Ordering number : EN6235A

LC75844M

ON Semiconductor®

http://onsemi.com

CMOS IC

1/4-Duty General-Purpose LCD Display Driver

Overview

The LC75844M is a 1/4 duty general-purpose LCD driver that can be used for frequency display in electronic tuners under the control of a microcontroller. The LC75844M can drive an LCD with up to 88 segments directly. The LC75844M can also control up to 4 general-purpose output ports. Since the LC75844M uses separate power supply systems for the LCD drive block and the logic block, the LCD driver block power-supply voltage can be set to any voltage in the range 2.7 to 6.0 volts, regardless of the logic block power-supply voltage.

Application

- Car, Home frequency display

Features

- Support for 1/4 duty 1/2 bias or 1/4 duty 1/3 bias drive of up to 88 segments under serial data control.
- Serial data input supports CCB format communication with the system controller.
- Serial data control of the power-saving mode based backup function and all the segments forced off function
- Serial data control of switching between the segment output port and the general-purpose output port functions
- High generality, since display data is displayed directly without decoder intervention.
- Independent V_{LCD} for the LCD driver block (V_{LCD} can be set to any voltage in the range 2.7 to 6.0 volts, regardless of the logic block power-supply voltage.)
- The $\overline{INH}$ pin can force the display to the off state.
- RC oscillator circuit

- CCB is ON Semiconductor® 's original format. All addresses are managed by ON Semiconductor® for this format.

Semiconductor Components Industries, LLC, 2013
July, 2013

80608HKIM B8-8317 / 92299TH(OT) No.6235-1/15

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	-0.3 to +7.0	V
	V_{LCD} max	V_{LCD}	-0.3 to +7.0	
Input voltage	$V_{IN}1$	CE, CL, DI, $\overline{INH}$	-0.3 to +7.0	V
	$V_{IN}2$	OSC	-0.3 to V_{DD}+0.3	
	$V_{IN}3$	$V_{LCD}1$, $V_{LCD}2$	-0.3 to V_{LCD}+0.3	
Output voltage	$V_{OUT}1$	OSC	-0.3 to V_{DD}+0.3	V
	$V_{OUT}2$	S1 to S22, COM1 to COM4, P1 to P4	-0.3 to V_{LCD}+0.3	
Output current	$I_{OUT}1$	S1 to S22	300	μA
	$I_{OUT}2$	COM1 to COM4	3	mA
	$I_{OUT}3$	P1 to P4	5	
Allowable power dissipation	Pd max	Ta = 85°C	100	mW
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-55 to +125	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating Ranges at Ta = -40 to +85°C, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	2.7		6.0	V
	V_{LCD}	V_{LCD}	2.7		6.0	
Input voltage	$V_{LCD}1$	$V_{LCD}1$		2/3V_{LCD}	V_{LCD}	V
	$V_{LCD}2$	$V_{LCD}2$		1/3V_{LCD}	V_{LCD}	
Input high-level voltage	V_{IH}	CE, CL, DI, $\overline{INH}$	0.8V_{DD}		6.0	V
Input low-level voltage	V_{IL}	CE, CL, DI, $\overline{INH}$	0		0.2V_{DD}	V
Recommended external resistor	Rosc	OSC		43		kΩ
Recommended external capacitor	Cosc	OSC		680		pF
Oscillation guaranteed range	fosc	OSC	25	50	100	kHz
Data setup time	tds	CL, DI [Figure 2]	160			ns
Data hold time	tdh	CL, DI [Figure 2]	160			ns
CE wait time	tcp	CE, CL [Figure 2]	160			ns
CE setup time	tcs	CE, CL [Figure 2]	160			ns
CE hold time	tch	CE, CL [Figure 2]	160			ns
High-level clock pulse width	tϕH	CL [Figure 2]	160			ns
Low-level clock pulse width	tϕL	CL [Figure 2]	160			ns
Rise time	tr	CE, CL, DI [Figure 2]		160		ns
Fall time	tf	CE, CL, DI [Figure 2]		160		ns
$\overline{INH}$ switching time	tc	$\overline{INH}$, CE [Figure 3]	10			μs

Electrical Characteristics at Allowable Operating Ranges

Parameter	Symbol	Pin	Conditions	Ratings			Unit
				min	typ	max	
Hysteresis width	V_H	CE, CL, DI, $\overline{INH}$			$0.1V_{DD}$		V
Input high-level current	I_{IH}	CE, CL, DI, $\overline{INH}$	V_I = 6.0V			5.0	μA
Input low-level current	I_{IL}	CE, CL, DI, $\overline{INH}$	V_I = 0V	-5.0			μA
Output high-level voltage	$V_{OH}1$	S1 to S22	I_O = -20μA	V_{LCD}-0.9			V
	$V_{OH}2$	COM1 to COM4	I_O = -100μA	V_{LCD}-0.9			
	$V_{OH}3$	P1 to P4	I_O = -1mA	V_{LCD}-0.9			
Output low-level voltage	$V_{OL}1$	S1 to S22	I_O = 20μA			0.9	V
	$V_{OL}2$	COM1 to COM4	I_O = 100μA			0.9	
	$V_{OL}3$	P1 to P4	I_O = 1mA			0.9	
Output middle-level voltage *1	$V_{MID}1$	COM1 to COM4	1/2 bias, I_O = ±100μA	$1/2V_{LCD}$ -0.9		$1/2V_{LCD}$ +0.9	V
	$V_{MID}2$	S1 to S22	1/3 bias, I_O = ±20μA	$2/3V_{LCD}$ -0.9		$2/3V_{LCD}$ +0.9	
	$V_{MID}3$	S1 to S22	1/3 bias, I_O = ±20μA	$1/3V_{LCD}$ -0.9		$1/3V_{LCD}$ +0.9	
	$V_{MID}4$	COM1 to COM4	1/3 bias, I_O = ±100μA	$2/3V_{LCD}$ -0.9		$2/3V_{LCD}$ +0.9	
	$V_{MID}5$	COM1 to COM4	1/3 bias, I_O = ±100μA	$1/3V_{LCD}$ -0.9		$1/3V_{LCD}$ +0.9	
Oscillator frequency	f_{OSC}	OSC	Rosc = 43kΩ Cosc = 680pF	40	50	60	kHz
Supply current	$I_{DD}1$	V_{DD}	Power saving mode			5	μA
	$I_{DD}2$	V_{DD}	V_{DD} = 6.0V, output open, fosc = 50kHz		230	460	
	$I_{LCD}1$	V_{LCD}	Power saving mode			5	
	$I_{LCD}2$	V_{LCD}	V_{LCD} = 6.0V, output open, 1/2 bias, fosc = 50kHz		100	200	
	$I_{LCD}3$	V_{LCD}	V_{LCD} = 6.0V, output open, 1/3 bias, fosc = 50kHz		60	120	

Note: *1 Excluding the bias voltage generation divider resistors built into $V_{LCD}1$, $V_{LCD}2$. (See Figure 1.)

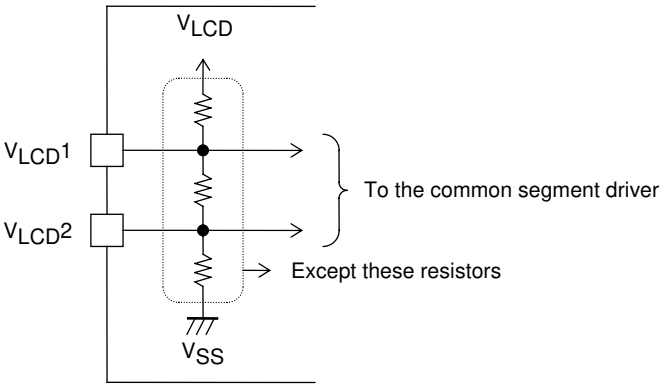
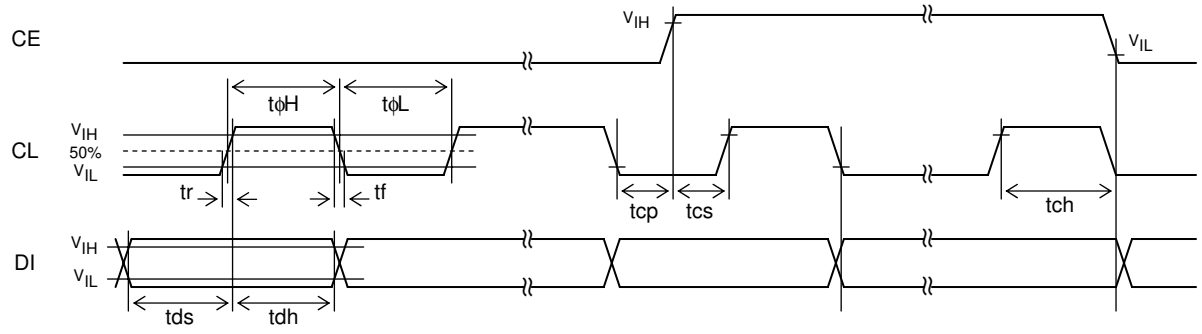


Figure 1

1. When CL is stopped at the low level



2. When CL is stopped at the high level

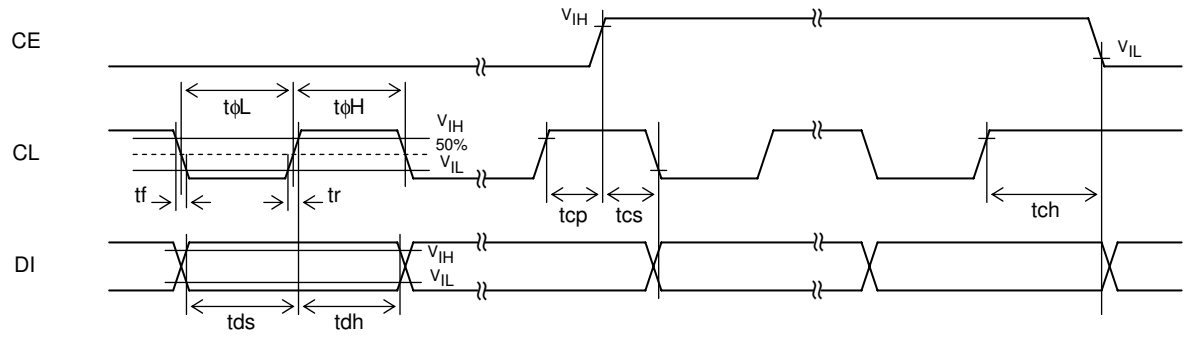
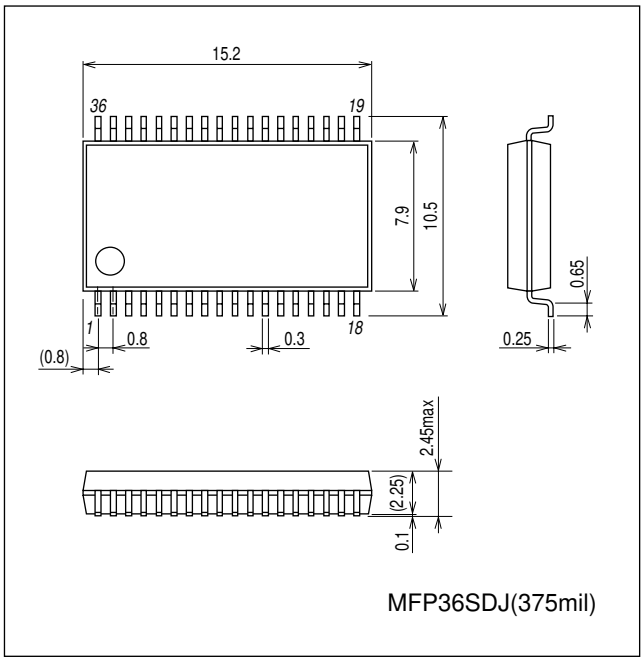


Figure 2

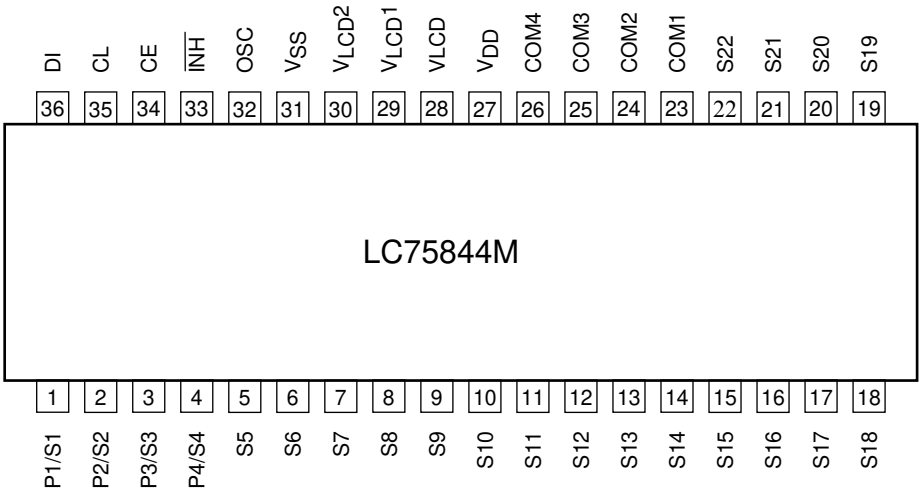
Package Dimensions

unit : mm (typ)

3263

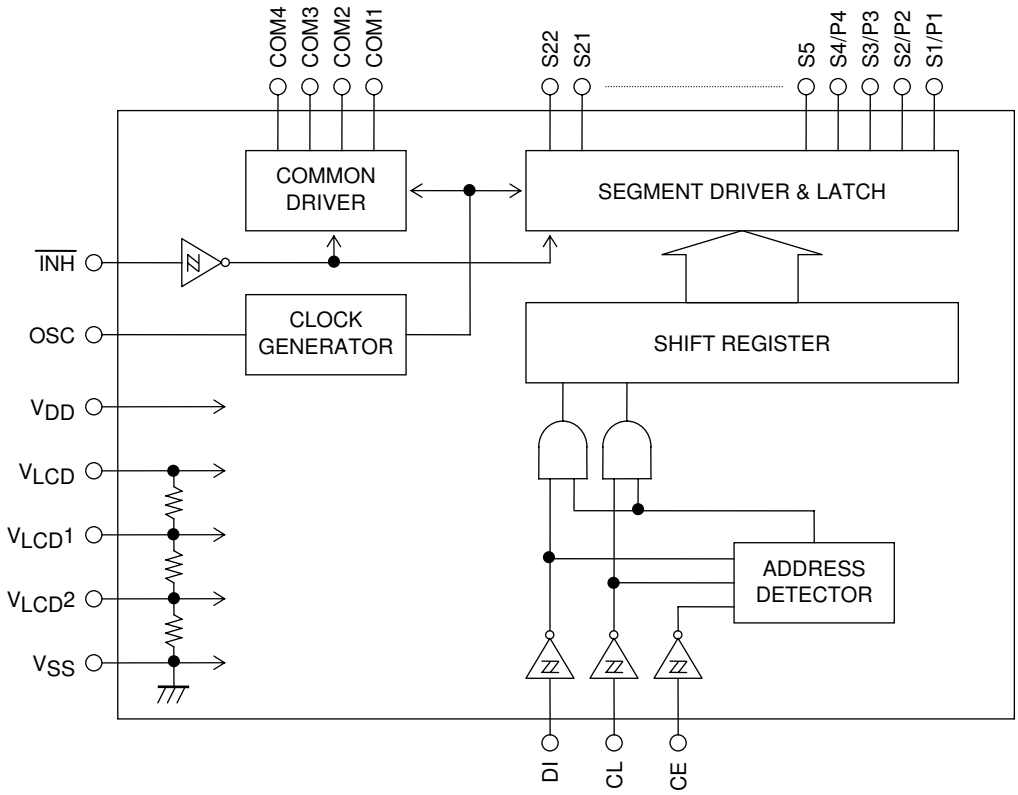


Pin Assignment



Top view

Block Diagram

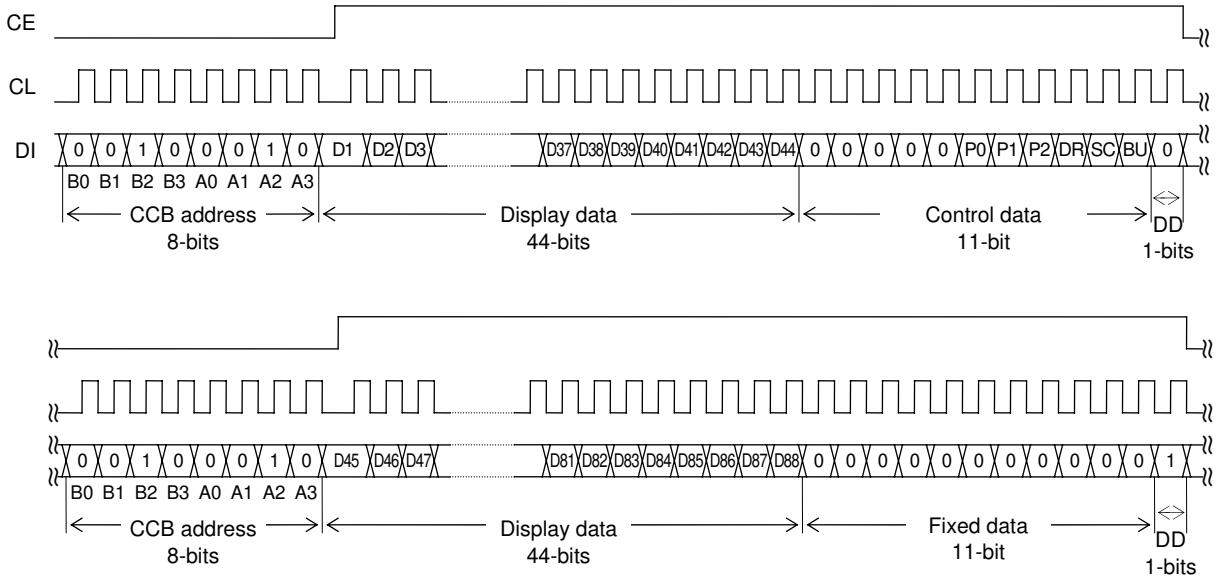


Pin Functions

Symbol	Pin No.	Function	Active	I/O	Handling when unused
S1/P1 to S4/P4 S5 to S22	1 to 4 5 to 22	Segment outputs for displaying the display data transferred by serial data input. The S1/P1 to S4/P4 pins can be used as general-purpose output ports under serial data control.	-	O	OPEN
COM1 to COM4	23 to 26	Common driver outputs The frame frequency (fo) is given by: fo=(fosc/512) Hz.	-	O	OPEN
OSC	32	Oscillator pin, which, together with externally connected resistor and capacitor, makes up an oscillator circuit.	-	I/O	V_{DD}
CE CL DI	34 35 36	Serial data transfer input pin to be connected to the controller. CE: Chip enable CL: Synchronization clock DI: Transfer data	H ↑ -	I I I	GND
$\overline{INH}$	33	Display off input pin • $\overline{INH}$="L" (V_{SS}) ... OFF S1/P1 to S4/P4="L" (V_{SS}) (Fixed to "L" after forced selection of segment output port.) S5 to S22="L" (V_{SS}) COM1 to COM4="L" (V_{SS}) • $\overline{INH}$="H" (V_{DD}) ... ON Note that the serial data can be transferred when OFF.	L	I	GND
$V_{LCD}1$	29	Used for applying the LCD driver 2/3 bias voltage externally. Must be connected to $V_{LCD}2$ when a 1/2 bias scheme is used.	-	I	OPEN
$V_{LCD}2$	30	Used for applying the LCD driver 1/3 bias voltage externally. Must be connected to $V_{LCD}1$ when a 1/2 bias scheme is used.	-	I	OPEN
V_{DD}	27	Logic block power supply pin to provide a voltage between 2.7V to 6.0V.	-	-	-
V_{LCD}	28	LCD driver power supply pin to provide a voltage between 2.7V to 6.0V.	-	-	-
V_{SS}	31	Power supply pin to connect to ground.	-	-	-

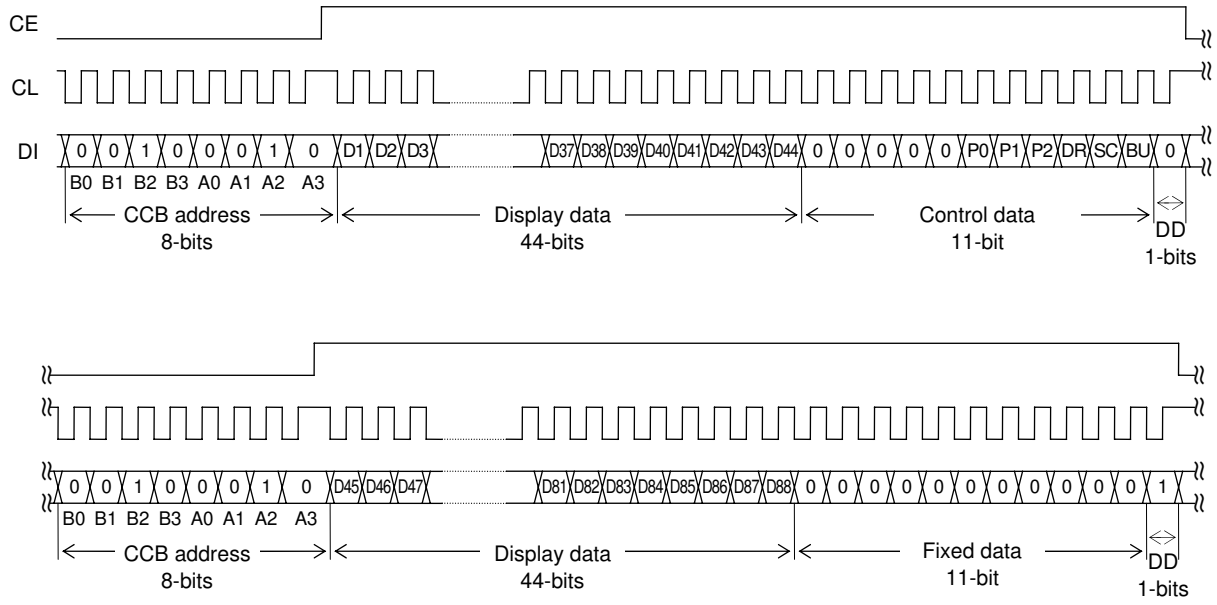
Serial Data Transfer Form

(1) When CL is stopped at the low level



Note) DD ····· Direction data

(2) When CL is stopped at the low level

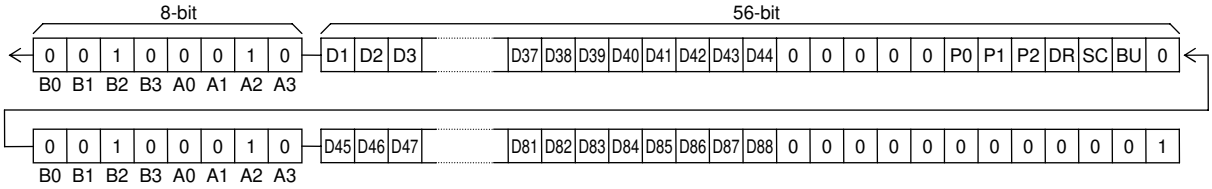


Note) DD ····· Direction data

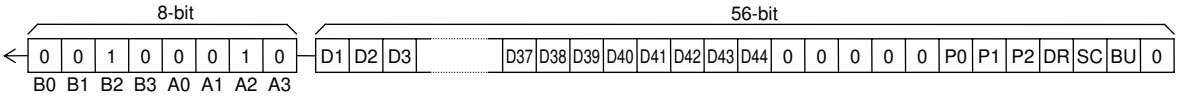
- CCB address ·· "44H"
- D1 to D88 ····· Display data
- P0 to P2····· Segment output port / general-purpose output port switching control data
- DR ····· 1/2 bias driver / 1/3 bias driver switching control data
- SC ····· Segment ON, OFF control data
- BU ····· Normal mode, power save mode control data

Example of Serial Data Transfer

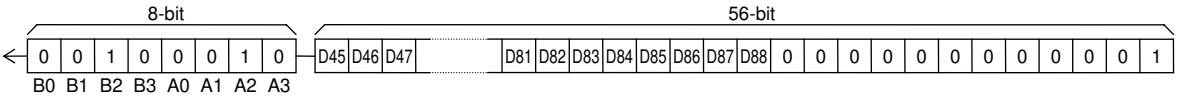
- When used with 45 segments or more
  Serial data must be transferred all 112-bit.



- When fewer than 45 segments are used, only 56-bits of serial data need to be sent. However, the display data D1 to D44 and the control data must be sent.



Note) When fewer than 45 segments are used, transfers such as that shown in the figure below cannot be used.



Control Data Description

(1) P0 to P2 ····· Segment output port/General-purpose output port switching control data
This control data switching output S1/P1 to S4/P4 segment output port and general-purpose output port.

Control data			Output pin state			
P0	P1	P2	S1/P1	S2/P2	S3/P3	S4/P4
0	0	0	S1	S2	S3	S4
0	0	1	P1	S2	S3	S4
0	1	0	P1	P2	S3	S4
0	1	1	P1	P2	P3	S4
1	0	0	P1	P2	P3	P4

Note) Sn (n=1 to 4): Segment output port
Pn (n=1 to 4): General-purpose output port

The following shows the correspondence between output pins and display data when the general-purpose output port is selected.

Output pin	Correspondence display data
S1/P1	D1
S2/P2	D5
S3/P3	D9
S4/P4	D13

For example, if output pin S4/P4 is for the general-purpose output port, output pin S4/P4 outputs high and low-level when display data D13="1" and D13= "0", respectively.

(2) DR ····· 1/2 bias drive, 1/3 bias driver switching control data
This control data switching LCD 1/2 bias driver and 1/3 bias driver.

DR	Driver method
0	1/3 bias driver
1	1/2 bias driver

(3) SC ····· Segment ON, OFF control data

This control data controls segment ON and OFF.

SC	Display state
0	ON
1	OFF

Note: that the OFF state with SC=[1] corresponds to the OFF state due to output of the display OFF waveform from the segment output pin.

(4) BU ····· Normal mode, Power save mode control data

This control data controls normal mode and power save mode.

BU	Mode
0	Normal mode
1	Power save mode (oscillation on the OSC pin stops and the common, segment output pins go low, However, output pins S1/P1 to S4/P4 can be used as the general-purpose output port by the use of control data P0 to P2.)

Display data and output pin correspondence

Output pin	COM1	COM2	COM3	COM4
S1/P1	D1	D2	D3	D4
S2/P2	D5	D6	D7	D8
S3/P3	D9	D10	D11	D12
S4/P4	D13	D14	D15	D16
S5	D17	D18	D19	D20
S6	D21	D22	D23	D24
S7	D25	D26	D27	D28
S8	D29	D30	D31	D32
S9	D33	D34	D35	D36
S10	D37	D38	D39	D40
S11	D41	D42	D43	D44

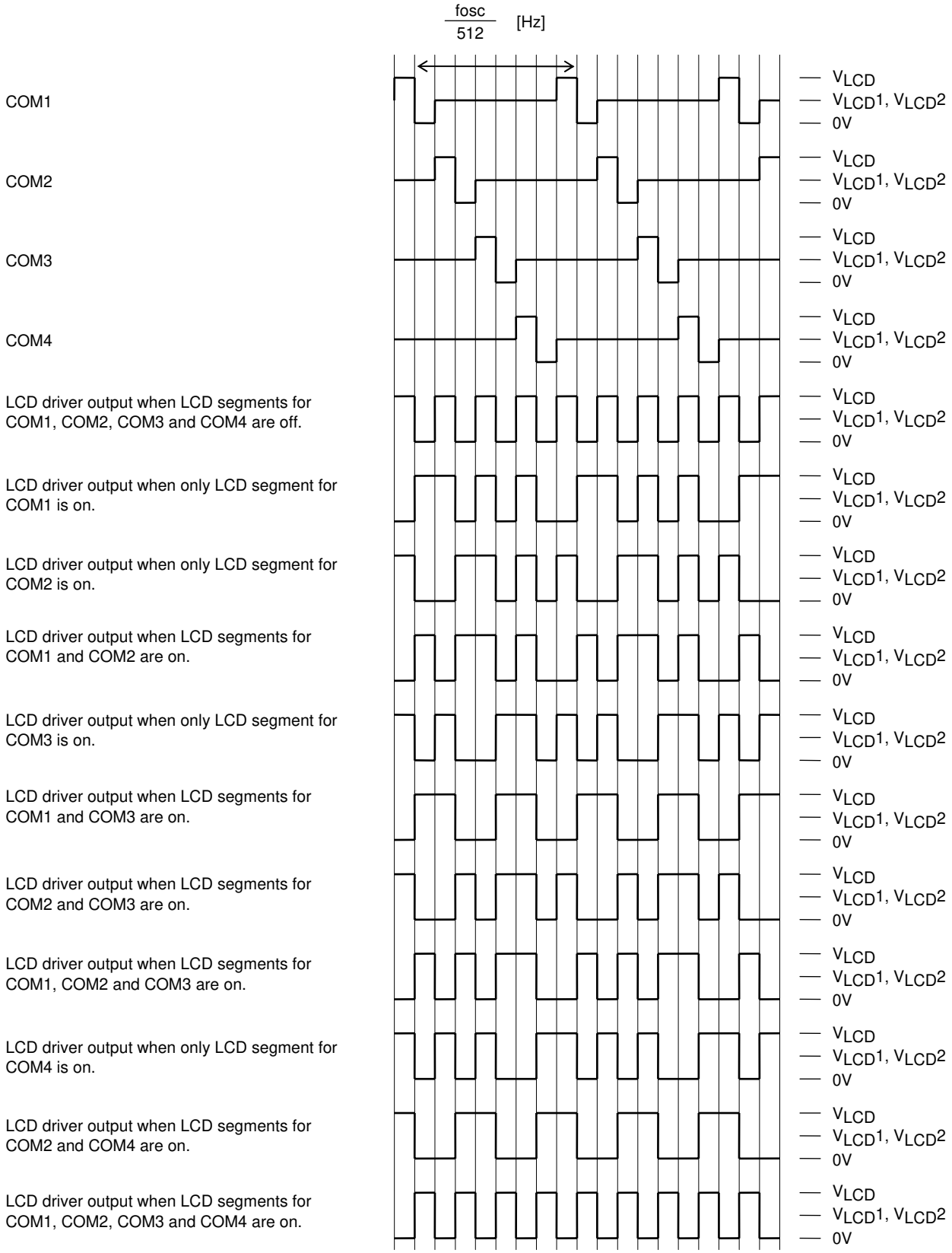
Output pin	COM1	COM2	COM3	COM4
S12	D45	D46	D47	D48
S13	D49	D50	D51	D52
S14	D53	D54	D55	D56
S15	D57	D58	D59	D60
S16	D61	D62	D63	D64
S17	D65	D66	D67	D68
S18	D69	D70	D71	D72
S19	D73	D74	D75	D76
S20	D77	D78	D79	D80
S21	D81	D82	D83	D84
S22	D85	D86	D87	D88

Note: Output pins S1/P1 to S4/P4 are for segment output port selection.

For example, the data to output pin correspondence for the output pin S11 is as follows.

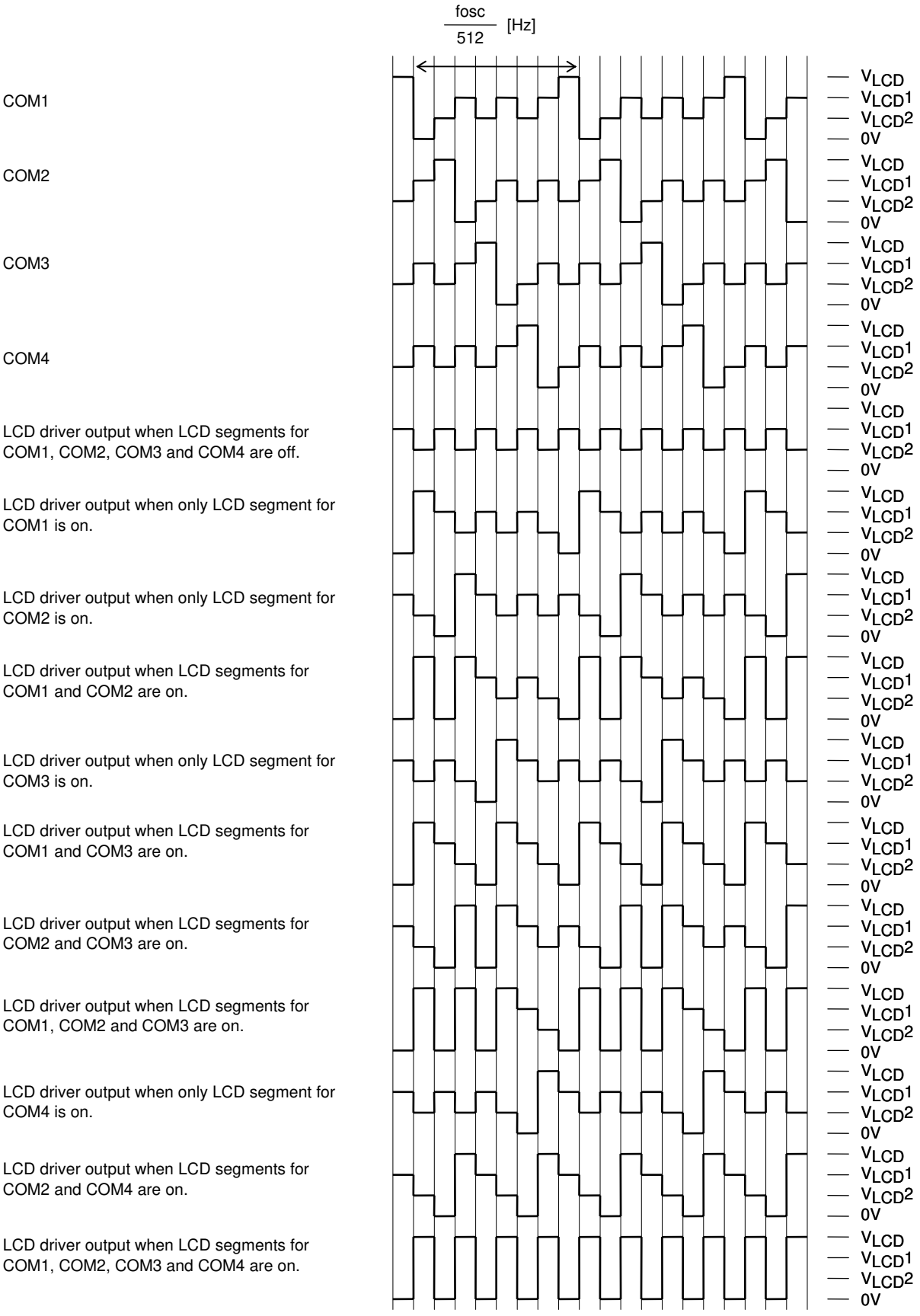
Display data				Output pin (S11) state
D41	D42	D43	D44	
0	0	0	0	LCD segments for COM1, COM2, COM3 and COM4 OFF
0	0	0	1	LCD segment for COM4 ON
0	0	1	0	LCD segment for COM3 ON
0	0	1	1	LCD segments for COM3 and COM4 ON
0	1	0	0	LCD segment for COM2 ON
0	1	0	1	LCD segments for COM2 and COM4 ON
0	1	1	0	LCD segments for COM2 and COM3 ON
0	1	1	1	LCD segments for COM2, COM3 and 4 ON
1	0	0	0	LCD segment for COM1 ON
1	0	0	1	LCD segments for COM1 and COM4 ON
1	0	1	0	LCD segments for COM1 and COM3 ON
1	0	1	1	LCD segments for COM1, 3 and COM4 ON
1	1	0	0	LCD segments for COM1 and COM2 ON
1	1	0	1	LCD segments for COM1, COM2 and COM4 ON
1	1	1	0	LCD segments for COM1, COM2 and COM3 ON
1	1	1	1	LCD segments for COM1, COM2, COM3 and COM4 ON

Output Waveforms (1/4-Duty 1/2-Bias ON System)



1/4 duty, 1/2 bias waveform

Output Waveforms (1/4-Duty 1/3-Bias ON System)



1/4 duty, 1/3 bias waveform

$\overline{\text{INH}}$ and Display Control

Since the IC internal data (D1 to D88, control data) is undefined immediately after applying power, hold $\overline{\text{INH}}$ low at same time as applying power to turn off the display (S1/P1 to S4/P4, S5 to S22, COM1 to COM4 ··· V_{SS} level), and serial transfer data from the microprocessor during the period that $\overline{\text{INH}}$ is low.
When the data transfer is complete, set $\overline{\text{INH}}$ high.
This procedure will avoid displaying meaningless patterns at startup. (See Figure 3)

Power Sequence

Be sure to observe the following sequence for power ON/OFF (See Figure 3)

- Power ON: Logic block power (V_{DD}) ON → LCD driver power (V_{LCD}) ON
- Power OFF: LCD driver power (V_{LCD}) OFF → Logic block power (V_{DD}) OFF

When the logic block power (V_{DD}) and LCD driver power (V_{LCD}) are common, both power supplies can be turned ON/OFF simultaneously.

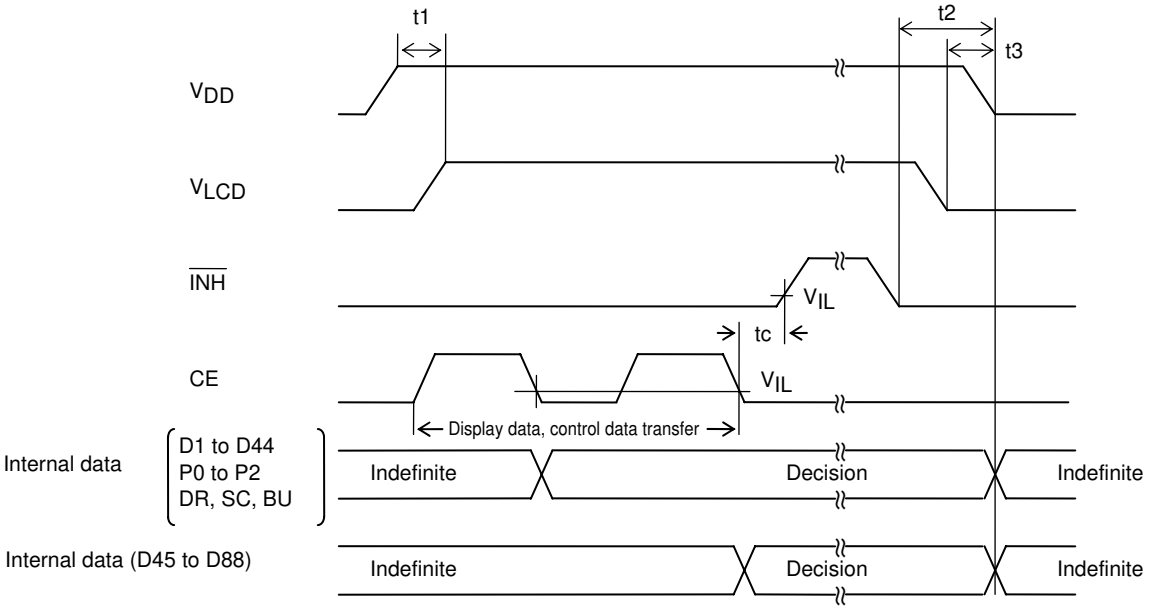


Figure 3

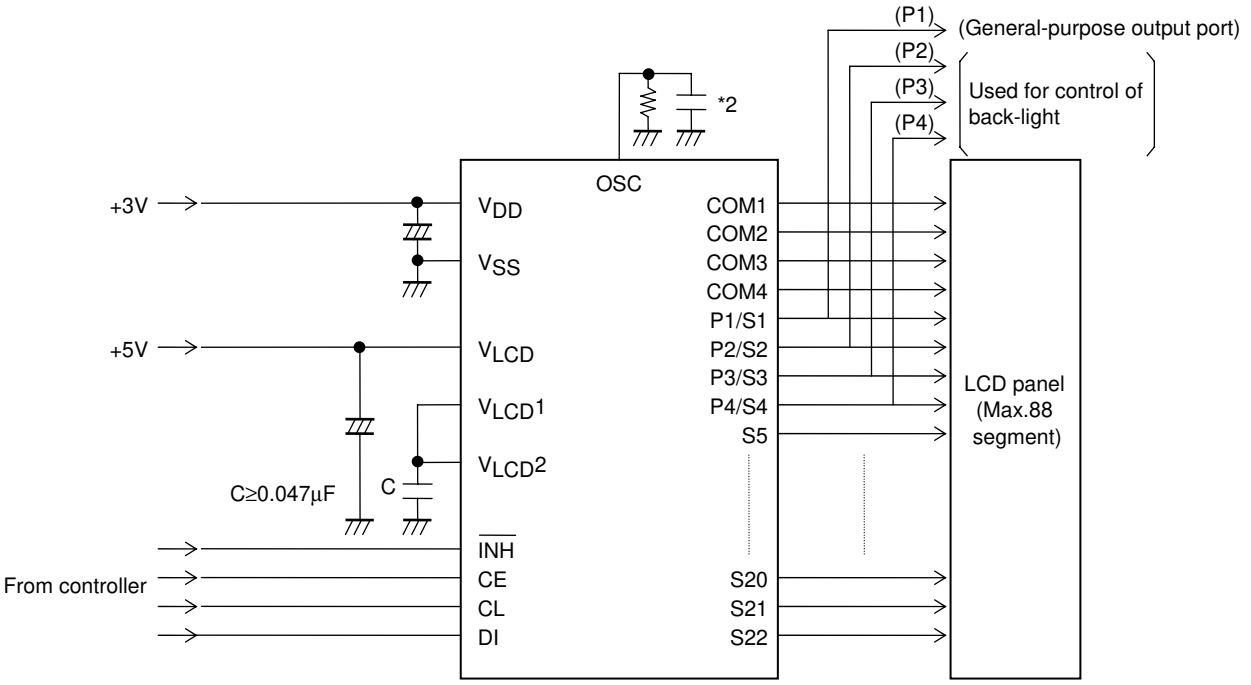
Note: •t1≥0
•t2>0
•t3≥0 (t2>t3)
•tc ····· 10μs min

Note on Controller-used Display Data Transfer

Since the LC75844M is such that display data (D1 to D88) is transferred in 4 times, it is recommended to transfer display data within 30 [ms] in terms of display quality.

Sample Application Circuit 1

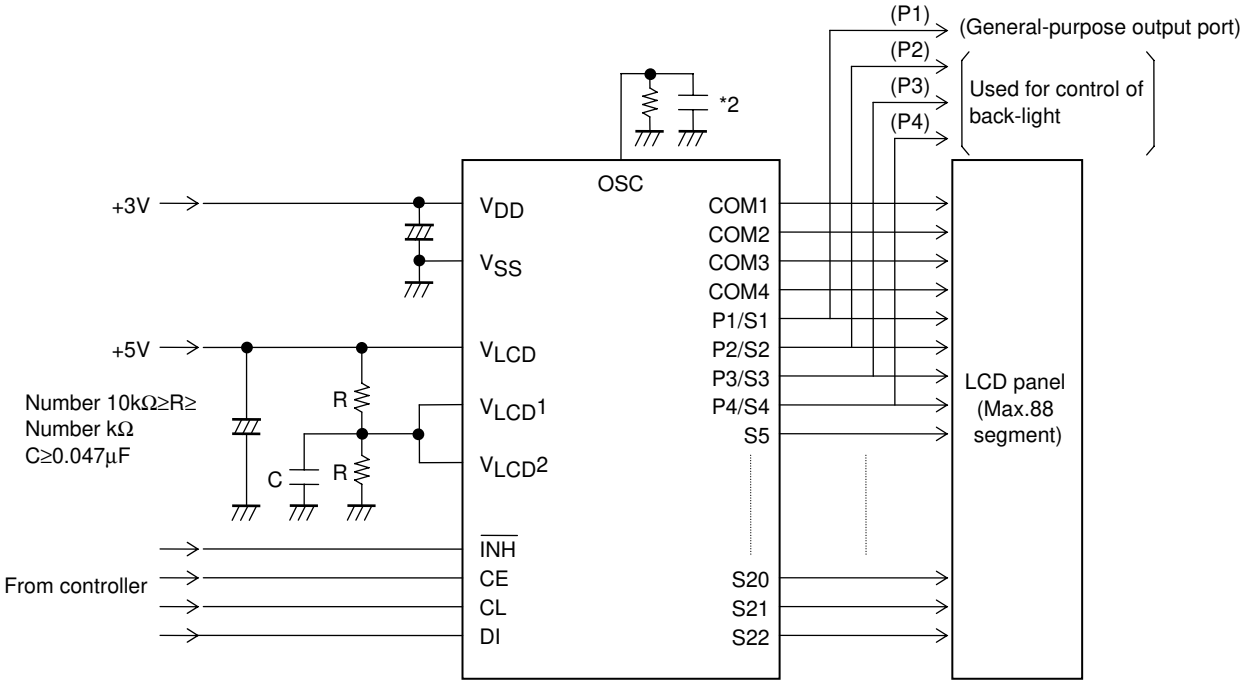
1/2 Bias (For normal panel)



*2 If a capacitor other than the external capacitor Cosc=680 [pF] recommended is to be used, it is recommended to used a capacitor of 220 to 2200 [pF].

Sample Application Circuit 2

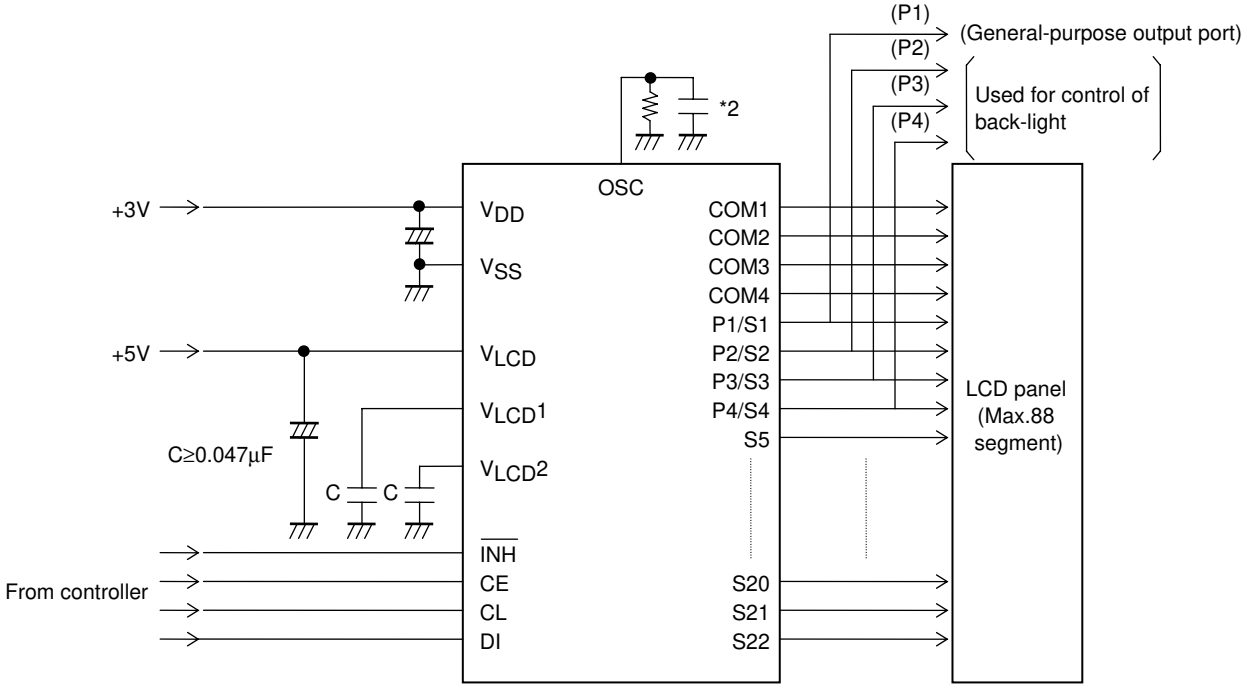
1/2 bias (For large panel)



*2 If a capacitor other than the external capacitor Cosc=680 [pF] recommended is to be used, it is recommended to used a capacitor of 220 to 2200 [pF].

Sample Application Circuit 3

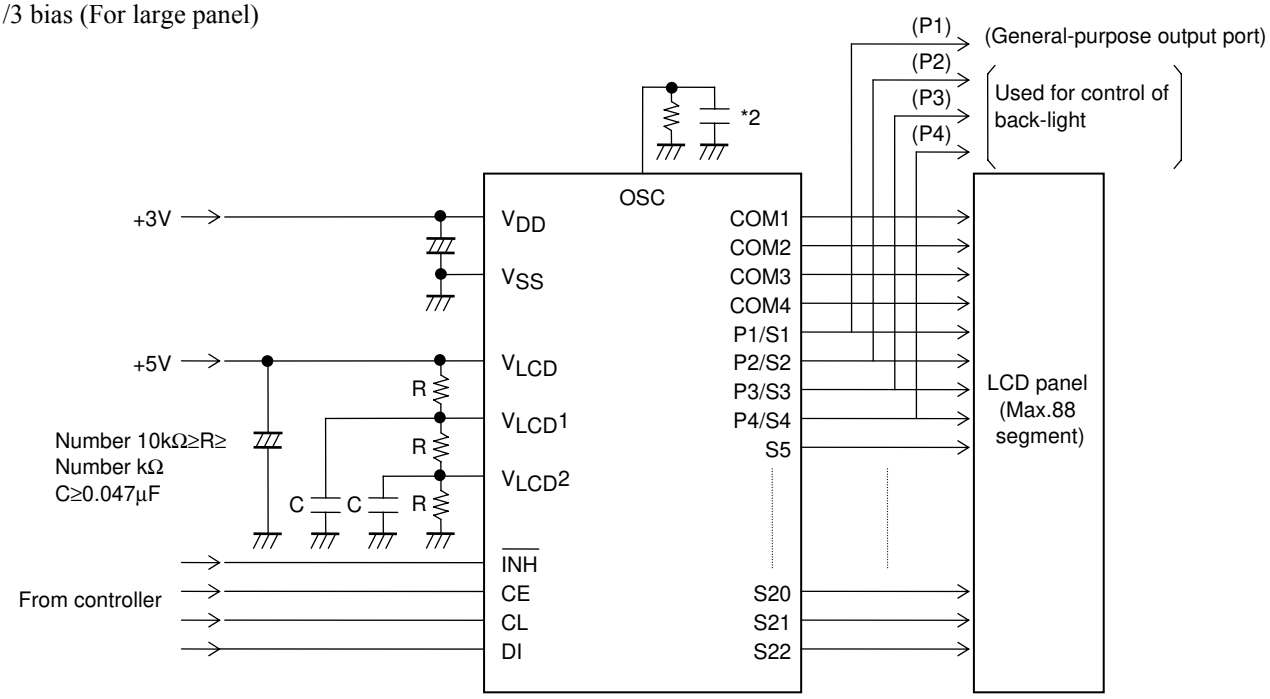
1/3 bias (For normal panel)



*2 If a capacitor other than the external capacitor Cosc=680 [pF] recommended is to be used, it is recommended to used a capacitor of 220 to 2200 [pF].

Sample Application Circuit 4

1/3 bias (For large panel)



*2 If a capacitor other than the external capacitor Cosc=680 [pF] recommended is to be used, it is recommended to used a capacitor of 220 to 2200 [pF].