REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes to table I, Common-mode rejection test. - drw	99-09-23	Raymond Monnin

REV																			
SHEET																			
REV	A	A																	
SHEET	15	16																	

REV STATUS OF SHEETS														
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
98-08-12

REVISION LEVEL
A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

MICROCIRCUIT, DIGITAL-LINEAR, SIGNAL CONDITIONING A/D CONVERTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-96762**

SHEET 1 OF 16

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:

5962	-	96762	01	Q	L	X
Federal stock class designator	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)
_____ Drawing number _____/						

1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	AD7710	Signal conditioning A/D converter

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

AV_{DD} to DV_{DD}	-0.3 V dc to +12 V dc
AV_{DD} to V_{SS}	-0.3 V dc to +12 V dc
AV_{DD} to AGND	-0.3 V dc to +12 V dc
AV_{DD} to DGND	-0.3 V dc to +12 V dc
DV_{DD} to AGND	-0.3 V dc to +6 V dc
DV_{DD} to DGND	-0.3 V dc to +6 V dc
V_{SS} to AGND	+0.3 V dc to -6 V dc
V_{SS} to DGND	+0.3 V dc to -6 V dc
Analog input voltage to AGND	V_{SS} - 0.3 V dc to AV_{DD} + 0.3 V dc
Reference input voltage to AGND	V_{SS} - 0.3 V dc to AV_{DD} + 0.3 V dc
REF OUT to AGND	-0.3 V dc to AV_{DD}
Digital input voltage to DGND	-0.3 V dc to AV_{DD} + 0.3 V dc
Digital output voltage to DGND	-0.3 V dc to DV_{DD} + 0.3 V dc
Storage temperature range	-65EC to +150EC
Lead temperature (soldering, 10 secs)	+265EC
Power dissipation to +75EC (P_D) 2/	450 mW

1.4 Recommended operating conditions.

Ambient operating temperature range	-55EC to +125EC

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Derate linearly above +75EC at 6 mW/EC.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 81 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C # T_A #+125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
No missing codes 2/		For filter notch # 60 Hz	1, 2, 3	01	24		Bits
		For filter notch = 100 Hz			22		
		For filter notch = 250 Hz			18		
		For filter notch = 500 Hz			15		
		For filter notch = 1 Khz			12		
Integral nonlinearity	INL	For filter notch # 60 Hz	1, 2, 3	01	-0.0015		%FSR
Bipolar negative full-scale error	BPFSE	Excluding reference 3/	1, 2, 3	01	-0.003	+0.003	%FSR
Analog Input Common-mode rejection	CMR	At DC, MCLKIN = 8 Mhz, AV_{DD} = +10.5 V, REF IN(+) = +1.25 V	1, 2, 3	01	90		dB
Common-mode voltage range	CMV	4/, 5/	1, 2, 3	01	V_{SS}	AV_{DD}	V
Normal - mode rejection 2/	NMR	For filter notches of 10, 25, 50 Hz, ±0.02 x f_{NOTCH}	1, 2, 3	01	100		dB
		For filter notches of 10, 30, 60 Hz, ±0.02 x f_{NOTCH}			100		
DC input leakage current	I_{IL}	2/	1, 2, 3	01		1	nA
Sampling capacitance	C_S	2/	4	01		20	pF
Analog input voltage range 6/, 7/	V_{IN}	Bipolar input range (B/U bit of control register = 0)	1, 2, 3	01		±V_{REF}	V
Reference input voltage	V_{REFIN}	REF IN(+) - REF IN(-) 8/	1, 2, 3	01	2.5	5	V
Reference output voltage	V_{REFO}		1, 2, 3	01	2.475	2.525	V
Line regulation (AV_{DD})		AV_{DD} = +5 V ±0.25 V	1, 2, 3	01		1	mV/V
Load regulation		Max load current 1 mA	1, 2, 3	01		1.5	mV/ mA
Input low voltage	V_{INL}	All inputs 5/	7, 8	01		0.8	V
Input high voltage 5/	V_{INH}	All inputs except MCLK IN	7, 8	01	2.0		V
		MCLK IN only			3.5		
Input current	I_{IN}		1, 2, 3	01	-10	+10	µA
Output low voltage	V_{OL}	I_{SINK} = 1.6 mA 5/	7, 8	01		0.4	V
Output high voltage	V_{OH}	I_{SOURCE} = 100 µA 5/	7, 8	01	DV_{DD-1}		V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ -55°C # T_A #+125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Floating state leakage current	I_{FL}		7, 8	01	-10	+10	µA
Transducer burn-out current	I_{BO}		1, 2, 3	01	3	6	µA
Compensation output current	I_{CO}		1, 2, 3	01	16	24	µA
Compensation current line regulation (AV_{DD})	I_{LINE}	AV_{DD} = +5 V ± 0.25 V	1, 2, 3	01		20	nA/V
Compensation current load regulation	I_{LOAD}		1, 2, 3	01		20	nA/V
Output compliance	V_{OC}	2/	1, 2, 3	01		AV_{DD}-2	V
Positive full-scale calibration	FSC 9/	GAIN is the selected PGA gain (between 1 and 128)	1, 2, 3	01		$\frac{(1.05 \times V_{REF})}{GAIN}$	V
Negative full-scale calibration						$-\frac{(1.05 \times V_{REF})}{GAIN}$	V
Offset calibration limits	OC 10/		1, 2, 3	01		$-\frac{(1.05 \times V_{REF})}{GAIN}$	V
Input span	IS 10/		1, 2, 3	01	$\frac{(0.8 \times V_{REF})}{GAIN}$	$\frac{(2.1 \times V_{REF})}{GAIN}$	V
AV_{DD} current	I_{AVDD}		1, 2, 3	01		4	mA
DV_{DD} current	I_{DVDD}		1, 2, 3	01		4.5	mA
V_{SS} current	I_{VSS}	V_{SS} = -5.25 V	1, 2, 3	01		1.5	mA
Master clock frequency	f_{CLKIN} 11/, 12/	Crystal oscillator or externally supplied for specified performance	9	01		10	MHz
SYNC pulse width	t_1	5/	9	01	1000		ns
DRDY to RES setup time	t_2	2/, 5/	9	01	0		ns
DRDY to RES hold time	t_3	5/	9, 10, 11	01	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ -55°C # T_A #+125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
A0 to RFS setup time	t_4	2/, 5/	9	01	2 X t_{CLKIN}		ns
RFS low to SCLK falling edge	t_6	2/, 5/	9, 10, 11	01		4 X t_{CLKIN} + 20	ns
Data access time (RFS low to data valid)	t_7	2/, 5/, 13/	9, 10, 11	01		4 X $t_{CLKIN + 20}$	ns
A0 to TFS setup time	t_{14}	2/, 5/	9	01	50		ns
A0 to TFS hold time	t_{15}	2/, 5/	9	01	0		ns
TFS to SCLK falling edge delay time	t_{16}	2/, 5/	9, 10, 11	01		4 X t_{CLKIN} +20	ns
TFS to SCLK falling edge hold time	t_{17}	5/	9	01	4 X t_{CLKIN}		ns
Data valid to SCLK setup	t_{18}	5/	9	01	0		ns
Serial clock input frequency	f_{SCLK}	5/	9	01		$f_{CLKIN/5}$	MHz
DRDY to RFS setup time	t_{20}	5/	9	01	0		ns
A0 to RFS setup time	t_{22}	2/, 5/	9, 10, 11	01	2 X t_{CLKIN}		ns
A0 to RFS hold time	t_{23}	2/, 5/	9, 10, 11	01	0		ns
Data access time (RFS low to data valid)	t_{24}	2/, 5/, 13/	9, 10, 11	01		4 X t_{CLKIN}	ns
SCLK low pulse width	t_{26}	5/	9	01	2 X t_{CLKIN}		ns
SCLK high pulse width	t_{27}	5/	9	01	2 X t_{CLKIN}		ns
RFS to data valid hold time	t_{31}	2/, 5/, 14/	9, 10, 11	01		5 X t_{CLKIN}/2 + 50	ns
A0 to TFS setup time	t_{32}	5/	9	01	0		ns
A0 to TFS hold time	t_{33}	5/	9	01	0		ns
SCLK falling edge to TFS hold time	t_{34}	2/, 5/	9, 10, 11	01	4 X t_{CLKIN}		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

1/ AV_{DD} = +5 V ±5%, DV_{DD} = +5 V ±5%, V_{SS} = 0 V/ -5 V, REF IN(+) = +2.5 V, REF IN(-) = AGND unless otherwise specified. MCLK IN = 10 Mhz.

2/ Measured only at initial design characterization and after design or process changes which may affect this parameter. these limits are guaranteed even though they are not tested.

3/ Applies after calibration at the temperature of interest.

4/ This common-mode voltage range is allowed provided that the input voltage on AIN(+) and AIN(-) does not exceed AV_{DD} + 30 mV and V_{SS} - 30 mV.

5/ This relationship is 100% tested on a pass/fail basis, with no parametric value returned.

6/ The analog inputs present a very high impedance dynamic load which varies with clock frequency and input sample rate. The maximum recommended source resistance depends on the selected gain.

7/ The analog input voltage range on the AIN1(+) and AIN2(+) inputs is given here with respect to the voltage on the AIN1(-) and AIN2(-) inputs. The absolute voltage on the analog inputs should not go more positive than AV_{DD} + 30 mV or go more negative than V_{SS} - 30 mV.

8/ The reference input voltage range may be restricted by the input voltage range requirement of the V_{BIAS} input.

9/ After calibration, if the analog input exceeds positive full scale, the converter will output all 1s. If the analog input is less than negative full scale the device will output all 0s.

10/ These calibration and span limits apply provided the absolute voltage on the analog inputs does not exceed AV_{DD} + 30 mV or go more negative than V_{SS} - 30 mV. The offset calibration limit applies to both the unipolar and bipolar zero point.

11/ Timing specification guaranteed by test vector coverage.

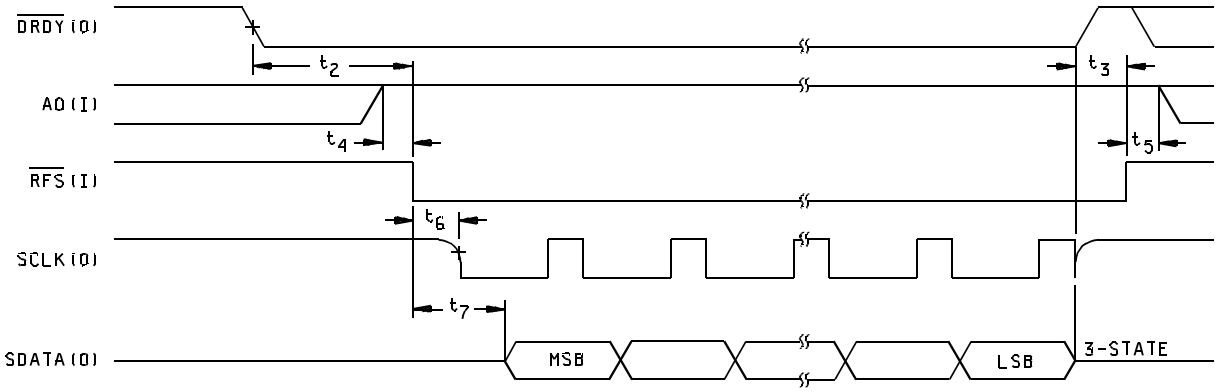
12/ CLK IN duty cycle range is 45% to 55%. CLK IN must be supplied when ever the device is not in STANDBY mode. If no clock is present in this case, the device can draw higher current than specified and possibly become uncalibrated.

13/ These numbers are measured with the load circuit of figure 3 and defined as the time required for the output to cross 0.8 V or 2.4 V.

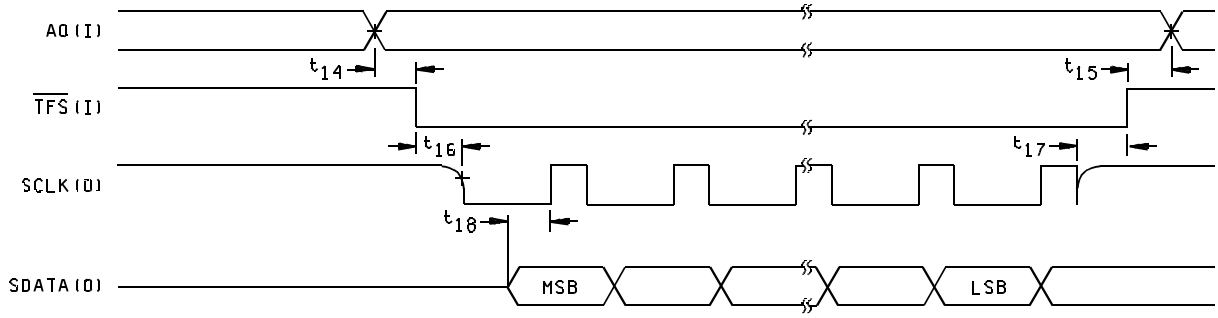
14/ These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of figure 3. The measured number is then extrapolated back to remove effects of charging or discharging the 100 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and, as such, are independent of external bus loading capacitances.

Device type	01
Case outline	L
Terminal number	Terminal symbols
1	SCLK
2	MCLK IN
3	MCLK OUT
4	A0
5	SYNC
6	MODE
7	AIN1(+)
8	AIN1(-)
9	AIN2(+)
10	AIN2(-)
11	V_{SS}
12	AV_{DD}
13	V_{BIAS}
14	REF IN(-)
15	REF IN(+)
16	REF OUT
17	I_{OUT}
18	AGND
19	TFS
20	RFS
21	DRDY
22	SDATA
23	DV_{DD}
24	DGND

FIGURE 1. Terminal connections.

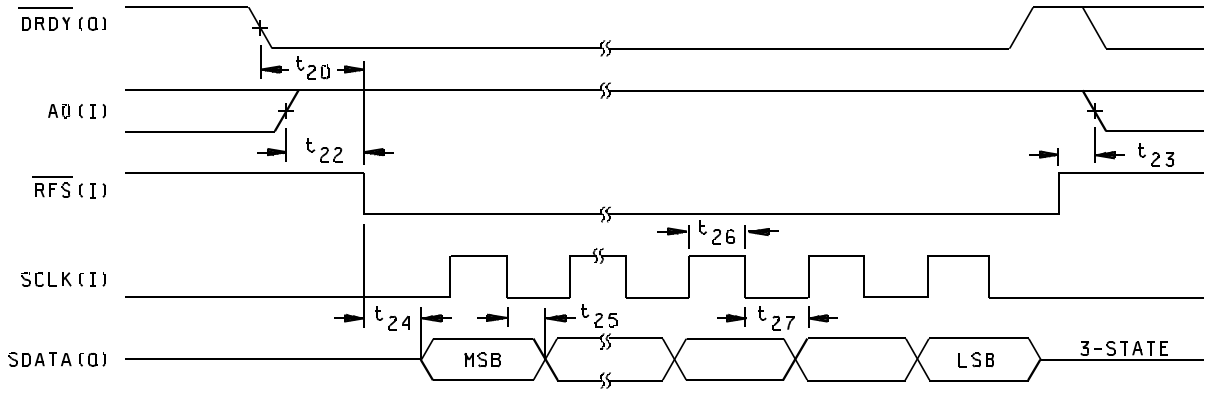


Self-clocking mode, output data read operation

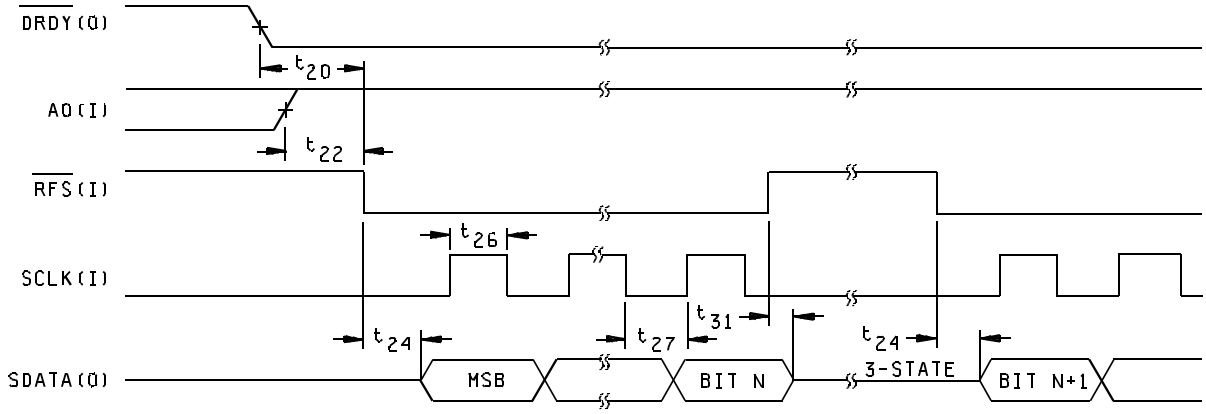


Self-clocking mode, control/calibration register write operation

FIGURE 2. Timing waveforms.

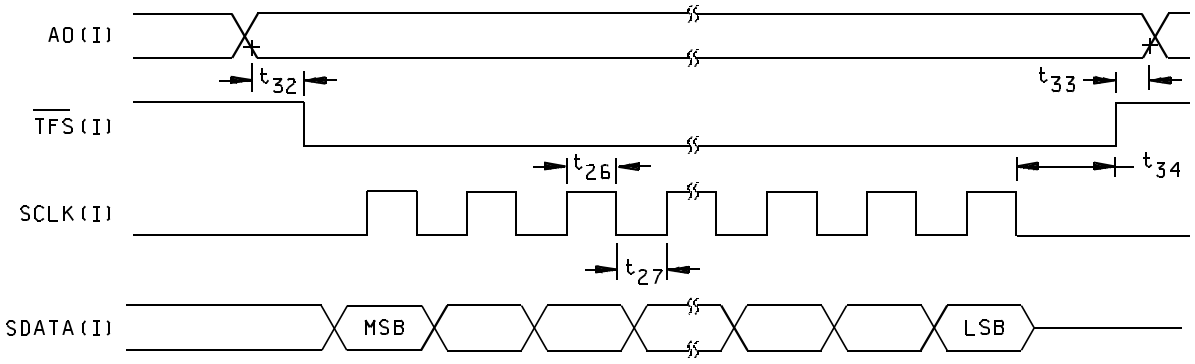


External-clocking mode, output data read operation

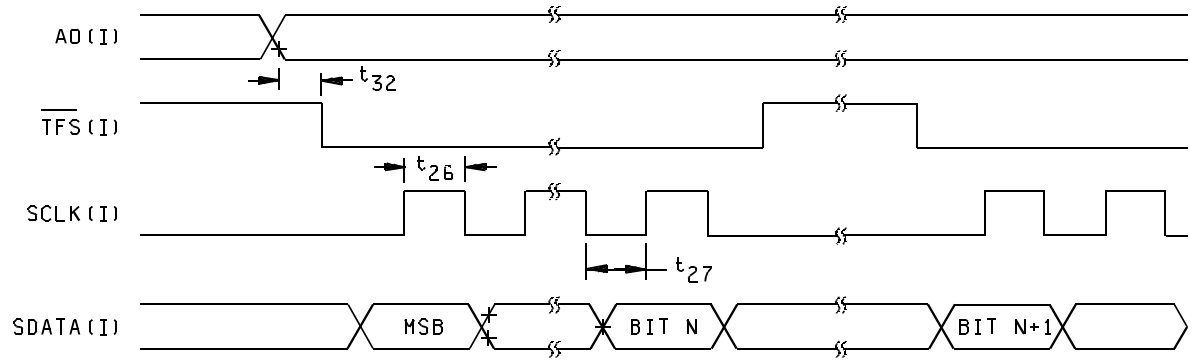


External-clocking mode, output data read operation (RFS returns high during read operation)

FIGURE 2. Timing waveforms - continued.

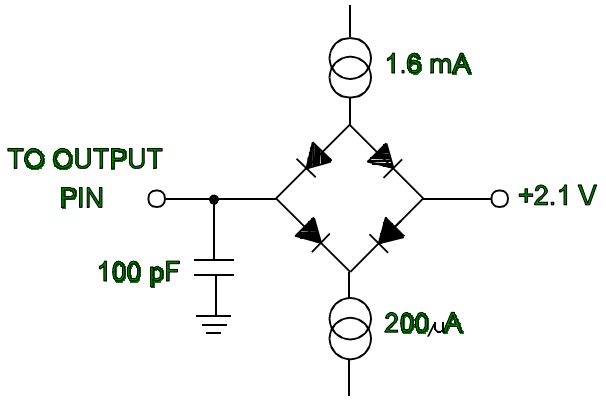


External-clocking mode, control/calibration register write operation



External-clocking mode, control/calibration register write operation ($\overline{TFS}$ returns high during write operation)

FIGURE 2. Timing waveforms - continued.



Load circuit for access time and bus relinquish time

FIGURE 3. Load circuit.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125EC, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Tests shall be as specified in table II herein.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 2, 3	1, 2, 3	1, 2, 3
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 4, 7, 8, 9, 10, 11	1/ 1, 2, 3, 4, 7, 8, 9, 10, 11	1/ 1, 2, 3, 4, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	- - -	- - -	- - -

1/ PDA applies to subgroup 1.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125EC, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25EC ±5EC, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply CenterColumbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 99-09-23

Approved sources of supply for SMD 5962-96762 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9676201QLA	24355	AD7710SQ/883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
24355	Analog Devices RT 1 Industrial Park PO Box 9106 Norwood, MA 02062 Point of contact: Bay F-1 Raheen IND. Estate Limerick, Ireland