

Skylake S-Line Applications: Setting VSA to SVID

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Intersil supports Intel Skylake™ S-Line applications with a variety of products. One product, the ISL95855, can support both the IA and GT core rails along with the System Agent (SA) rail in these Desktop applications. S-Line applications only require the SA rail to have a fixed VR at 1.05V. When using products like the ISL95855, one question which arises is how to communicate with the CPU since the SA rail is an SVID type VR. This technical brief will provide basic guidance on how to configure the Intel CPU to support an SVID type VR.

Skylake platforms support SPI flash devices which contain information used by the PCH in a Flash Descriptor. The Flash Descriptor is a data structure which is programmed to contain platform configuration data. Information is written during the manufacturing process and stored in the Flash Descriptor.

Within the Flash Descriptor structure map, the region of interest is the flash address UFCPUSBA +004h and default flash address 304h. Reference Intel Document Number: CDI/IBP# 550696. Refer to the 'Skylake-LP Client Platform: SPI Programming Guide' for more description of the SPI flash devices and the Flash Descriptor structure.

Section 9.181 on page 113 of the most recent revision of the Intel document (Revision 0.86.2, February 2015), provides the description of the configuration bits for flash address 304h. Bit 4 outlined in the table is for setting the SA core domain VR type. When this bit is set to "1", which indicates the SA core domain VR type is a fixed VR and does not require communication with the CPU. When this bit is set to "0", this indicates the SA core domain VR type is SVID and the CPU will communicate with the SA rail.

The issue resolved by configuring the CPU to support the SVID type VR for SA is clearing of the ALERT signal when platforms are first powered up. If the CPU is configured to support a fixed type VR, the ALERT signal will go low and never be cleared by the CPU. This is because the CPU has no way to communicate with the SVID type VR. Following the Intel SPI programming guide to set the configuration bit for the SA rail to recognize the VR as an SVID type resolves this issue.

[Table 1](#) outlines the Intersil controller classification pertaining to the VSA VR Type as a reference.

TABLE 1. VSA VR TYPE SELECTION BY PLATFORM

VSA VR TYPE CONTROLLER	S-LINE	H-LINE	U-LINE	Y-LINE
SVID ISL95829	Address 304h Bit 4 = 0	Address 304h Bit 4 = 0	Address 304h Bit 4 = 0	Address 304h Bit 4 = 0
SVID ISL95853/4	Address 304h Bit 4 = 0	Address 304h Bit 4 = 0	Address 304h Bit 4 = 0	Address 304h Bit 4 = 0
SVID ISL95855	Address 304h Bit 4 = 0	Address 304h Bit 4 = 0	Address 304h Bit 4 = 0	Address 304h Bit 4 = 0
SVID ISL95857	N/A	N/A	Address 304h Bit 4 = 0	Address 304h Bit 4 = 0
SVID ISL95859	N/A	N/A	Address 304h Bit 4 = 0	Address 304h Bit 4 = 0
Fixed VR ISL95870	Address 304h Bit 4 = 1	N/A	N/A	N/A

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