

December 1996

## Fast CMOS 8-Bit Identity Comparator

### Features

- Advanced 0.8 micron CMOS Technology
- CD74FCT521T is Pin Compatible with Bipolar FAST™ Series at a Higher Speed And Lower Power Consumption
- TTL Input and Output Levels
- Extremely Low Static Power
- Hysteresis on All Inputs

### Description

The CD74FCT521T is an 8-bit identity comparator. When two words of up to eight bits are compared, a bit-for-bit match of the two words provides a LOW output. The comparison can be extended over multiple words by the expansion input. The expansion input  $I_{A=B}$  also serves as an active LOW enable input.

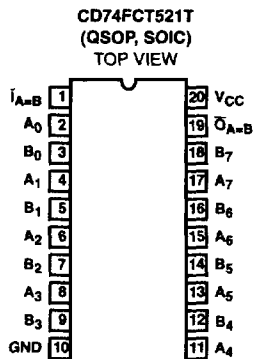
### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT521ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT521ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT521BTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT521BTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT521CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT521CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT521DTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT521DTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT521TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT521TQM	-40 to 85	20 Ld QSOP	M20.15-P

NOTE: QSOP is commonly known as SSOP.

When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

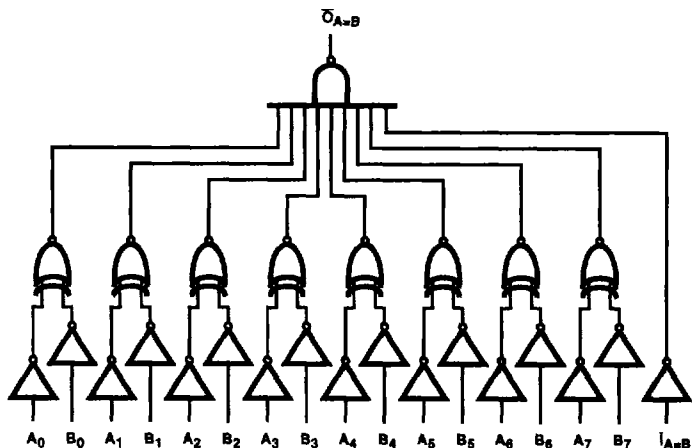
### Pinout



4

 OCTAL 5V FCT  
 5V FCT 25Ω

**Functional Block Diagram**



**TRUTH TABLE**

(NOTE 1) INPUTS		(NOTE 1) OUTPUTS
$\bar{I}_{A=B}$	A, B	$\bar{O}_{A=B}$
L	A = B (Note 2)	L
L	A $\neq$ B	H
H	A = B (Note 2)	H
H	A $\neq$ B	H

NOTE:

1. H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care
2.  $A_0 = B_0, A_1 = B_1, A_2 = B_2, \text{ etc.}$

**Pin Descriptions**

PIN NAME	DESCRIPTION
$\bar{I}_{A=B}$	Expansion or Enable Input (Active LOW)
$\bar{O}_{A=B}$	Identity Output (Active LOW)
$A_0 - A_7$	Word A Inputs
$B_0 - B_7$	Word B Inputs
GND	Ground
$V_{CC}$	Power

# CD74FCT521T

## Absolute Maximum Ratings

DC Input Voltage	-0.5V to 7.0V
DC Output Current	120mA

## Operating Conditions

Operating Temperature Range	-40°C to 85°C
Supply Voltage to Ground Potential	
Inputs and V <sub>CC</sub> Only	-0.5V to 7.0V
Supply Voltage to Ground Potential	
Outputs and D/O Only	-0.5V to 7.0V

## Thermal Information

Thermal Resistance (Typical, Note 3)	$\theta_{JA}$ (°C/W)
SOIC Package	87
QSOP Package	110
Maximum Junction Temperature	150°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C (Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

## Electrical Specifications

PARAMETER	SYMBOL	(NOTE 4) TEST CONDITIONS	MIN	(NOTE 5) TYP	MAX	UNITS
<b>DC ELECTRICAL SPECIFICATIONS</b> Over the Operating Range, $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ , $V_{CC} = 5.0\text{V} \pm 5\%$						
Output HIGH Voltage	$V_{OH}$	$V_{CC} = \text{Min}$ , $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -15.0\text{mA}$	2.4	3.0	- V
Output LOW Voltage	$V_{OL}$	$V_{CC} = \text{Min}$ , $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 48\text{mA}$	-	0.3	0.50 V
Input HIGH Voltage	$V_{IH}$	Guaranteed Logic HIGH Level		2.0	-	- V
Input LOW Voltage	$V_{IL}$	Guaranteed Logic LOW Level		-	-	0.8 V
Input HIGH Current	$I_{IH}$	$V_{CC} = \text{Max}$	$V_{IN} = V_{CC}$	-	-	1 $\mu\text{A}$
Input LOW Current	$I_{IL}$	$V_{CC} = \text{Max}$	$V_{IN} = \text{GND}$	-	-	-1 $\mu\text{A}$
Clamp Diode Voltage	$V_{IK}$	$V_{CC} = \text{Min}$ , $I_{IN} = -18\text{mA}$		-	-0.7	-1.2 V
Short Circuit Current	$I_{OS}$	$V_{CC} = \text{Max}$ (Note 6), $V_{OUT} = \text{GND}$		-60	-120	- mA
Power Down Disable	$I_{OFF}$	$V_{CC} = \text{GND}$ , $V_{OUT} = 4.5\text{V}$		-	-	100 $\mu\text{A}$
Input Hysteresis	$V_H$			-	200	- mV
<b>CAPACITANCE</b> $T_A = 25^\circ\text{C}$ , $f = 1\text{MHz}$						
Input Capacitance (Note 7)	$C_{IN}$	$V_{IN} = 0\text{V}$		-	6	10 pF
Output Capacitance (Note 7)	$C_{OUT}$	$V_{OUT} = 0\text{V}$		-	8	12 pF
<b>POWER SUPPLY SPECIFICATIONS</b>						
Quiescent Power Supply Current	$I_{CC}$	$V_{CC} = \text{Max}$	$V_{IN} = \text{GND}$ or $V_{CC}$	-	0.1	500 $\mu\text{A}$
Supply Current per Input at TTL HIGH	$\Delta I_{CC}$	$V_{CC} = \text{Max}$	$V_{IN} = 3.4\text{V}$ (Note 8)	-	0.5	2.0 mA
Supply Current per Input per MHz (Note 9)	$I_{CCD}$	$V_{CC} = \text{Max}$ , Outputs Open One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	-	0.15	0.25 mA/MHz
Total Power Supply Current (Note 11)	$I_C$	$V_{CC} = \text{Max}$ , Outputs Open $f_I = 10\text{MHz}$ 50% Duty Cycle One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	-	1.5	3.5 (Note 10) mA
			$V_{IN} = 3.4\text{V}$ $V_{IN} = \text{GND}$	-	1.8	4.5 (Note 10) mA

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OCTAL 5V FCT  
5V FCT 25Ω

## CD74FCT521T

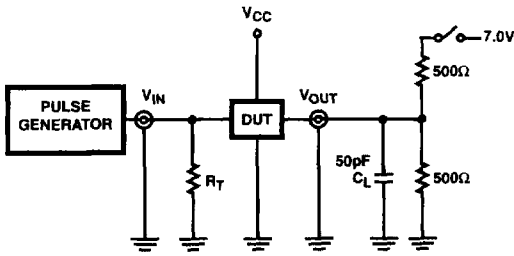
### Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 12) TEST CONDITIONS	T		AT		BT		CT		DT		UNITS
			(NOTE 13) MIN	MAX	(NOTE 13) MIN	MAX	(NOTE 13) MIN	MAX	(NOTE 13) MIN	MAX	(NOTE 13) MIN	MAX	
Propagation Delay $A_N$ or $B_N$ to $\bar{O}_{A=B}$	$t_{PLH}$ , $t_{PHL}$	$C_L = 50\text{pF}$ $R_L = 500\Omega$	1.5	10.0	1.5	7.2	1.5	5.5	1.5	4.5	1.5	4.2	ns
Propagation Delay $\bar{I}_{A=B}$ to $\bar{O}_{A=B}$	$t_{PLH}$ , $t_{PHL}$		1.5	9.0	1.5	6.0	1.5	4.6	1.5	4.1	1.5	3.8	ns

**NOTES:**

4. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type
5. Typical values are at  $V_{CC} = 5.0V$ ,  $25^\circ\text{C}$  ambient and maximum loading.
6. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
7. This parameter is determined by device characterization but is not production tested.
8. Per TTL driven input ( $V_{IN} = 3.4V$ ); all other inputs at  $V_{CC}$  or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
10. Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.
11.  $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$   
 $I_{CC}$  = Quiescent Current  
 $\Delta I_{CC}$  = Power Supply Current for a TTL High Input ( $V_{IN} = 3.4V$ )  
 $D_H$  = Duty Cycle for TTL Inputs High  
 $N_T$  = Number of TTL Inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)  
 $f_{CP}$  = Clock Frequency for Register Devices (Zero for Non-Register Devices)  
 $f_I$  = Input Frequency  
 $N_I$  = Number of Inputs at  $f_I$   
 All currents are in milliamperes and all frequencies are in megahertz.
12. See test circuit and wave forms.
13. Minimum limits are guaranteed but not tested on Propagation Delays.

**Test Circuits and Waveforms**



SWITCH POSITION	
TEST	SWITCH
$t_{PLZ}, t_{PZL}$	Closed
$t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}$	Open

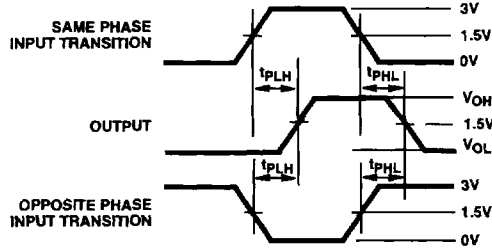
**DEFINITIONS:**

$C_L$  = Load capacitance, includes jig and probe capacitance.  
 $R_T$  = Termination resistance, should be equal to  $Z_{OUT}$  of the Pulse Generator.

**NOTE:**

14. Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $Z_{OUT} \leq 50\Omega$ ;  
 $t_f, t_r \leq 2.5\text{ns}$ .

**FIGURE 1. TEST CIRCUIT**



**FIGURE 2. PROPAGATION DELAY**