

FEATURES

Attenuation

Range: 31 dB

Step size: 1 dB

Insertion loss: 1.7 dB typical at 2.3 GHz to 3.0 GHz

Excellent attenuation accuracy: ± 0.3 dB

High Input linearity

0.1 dB compression (P0.1dB): 27 dBm typical at $V_{DD} = 5$ V

Third-order intercept (IP3): 50 dBm typical

High power handling: 27 dBm

Low phase shift: 27° at 1.5 GHz to 3.0 GHz

Single-supply operation: 3 V to 5 V

CMOS-/TTL-compatible parallel control

16-lead, 3 mm \times 3 mm LFCSP

ENHANCED PRODUCT FEATURES

Supports defense and aerospace applications
(AQEC standard)

Military temperature range: -55°C to $+125^\circ\text{C}$

Controlled manufacturing baseline

One assembly/test site

One fabrication site

Enhanced product change notification

Qualification data available on request

APPLICATIONS

Cellular infrastructure

Microwave radios and very small aperture terminals (VSATs)

Test equipment and sensors

IF and RF designs

GENERAL DESCRIPTION

The HMC470A-EP is a 5-bit digital step attenuator (DSA) with a 31 dB attenuation control range in 1 dB steps.

The HMC470A-EP offers excellent attenuation accuracy and high input linearity over the specified frequency range from 0.1 GHz to 3.0 GHz. However, this DSA features ACGx pins for external ac grounding capacitors to extend the operation below 100 MHz.

FUNCTIONAL BLOCK DIAGRAM

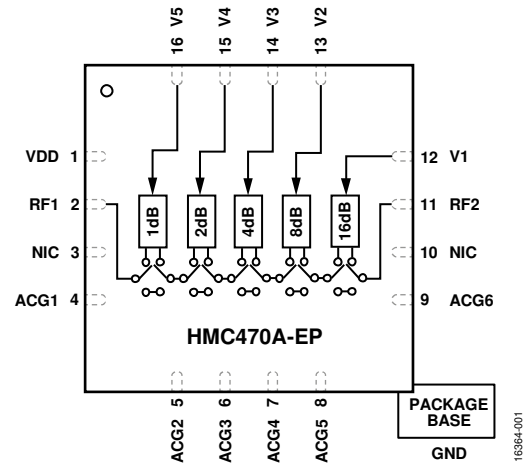


Figure 1.

The HMC470A-EP operates with a single positive supply voltage from 3 V to 5 V and provides CMOS-/TTL-compatible parallel control interface by incorporating an on-chip driver. The HMC470A-EP comes in a RoHS compliant, compact, 3 mm \times 3 mm LFCSP.

Additional application and technical information can be found in the [HMC470A](#) data sheet.

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REVISION HISTORY

10/2017—Revision 0: Initial Version

SPECIFICATIONS

$V_{DD} = 3\text{ V to }5\text{ V}$, V_1 to V_5 control pins voltage ($V_{CTL} = 0\text{ V or }V_{DD}$), $T_{CASE} = 25^\circ\text{C}$, $50\ \Omega$ system, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			0.1		3.0	GHz
INSERTION LOSS		0.1 GHz to 1.5 GHz		1.3	1.6	dB
		1.5 GHz to 2.3 GHz		1.5	1.8	dB
		2.3 GHz to 3.0 GHz		1.7	2.0	dB
ATTENUATION						
Control Range		Between minimum and maximum attenuation states, 0.1 GHz to 3.0 GHz		31		dB
Step Size		Between any successive attenuation states, 0.1 GHz to 3.0 GHz		1		dB
Step Error		Between any successive attenuation states, 0.1 GHz to 3.0 GHz		$\leq \pm 0.2$		dB
State Error		Referenced to insertion loss state				
		All attenuation states, 0.1 GHz to 2.3 GHz	$-(0.3 + 2\%$ of attenuation state)		$+(0.3 + 2\%$ of attenuation state)	dB
		1 dB to 15 dB attenuation states, 2.3 GHz to 3.0 GHz	$-(0.3 + 3\%$ of attenuation state)		$+(0.3 + 3\%$ of attenuation state)	dB
	16 dB to 31 dB attenuation states, 2.3 GHz to 3.0 GHz	$-(0.3 + 6\%$ of attenuation state)		$+(0.3 + 6\%$ of attenuation state)	dB	
RETURN LOSS		RF1 and RF2 pins, all attenuation states, 0.1 GHz to 3.0 GHz		14		dB
RELATIVE PHASE		Between minimum and maximum attenuation states				
		0.1 GHz to 1.5 GHz		12		Degrees
		1.5 GHz to 3.0 GHz		27		Degrees
SWITCHING CHARACTERISTICS		Between all attenuation states				
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		50		ns
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTL} to 90% of RF output		70		ns
INPUT LINEARITY ¹		All attenuation states, 250 MHz to 3.0 GHz				
0.1 dB Compression	P0.1dB	$V_{DD} = 3\text{ V}$		25		dBm
		$V_{DD} = 5\text{ V}$		27		dBm
Third-Order Intercept	IP3	10 dBm per tone, 1 MHz spacing		50		dBm
SUPPLY CURRENT	I_{DD}			1.7		mA
DIGITAL CONTROL INPUTS		V1 to V5 pins				
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		2.0		V_{DD}	V
Current						
Low	I_{INL}			1		μA
High	I_{INH}			40		μA

¹ Input linearity performance degrades at frequencies less than 250 MHz; see Figure 7 and Figure 9.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	7 V
Digital Control Input Voltage	-1 V to $V_{DD} + 1$ V
RF Input Power ¹ (All Attenuation States, f = 250 MHz to 3 GHz, $T_{CASE} = 85^{\circ}C$)	
$V_{DD} = 3$ V	25 dBm
$V_{DD} = 5$ V	27 dBm
Continuous Power Dissipation, P_{DISS} ²	
$T_{CASE} = 85^{\circ}C$	0.5 W
$T_{CASE} = 125^{\circ}C$	0.19 W
Temperature	
Junction, T_J	150°C
Storage Range	-65°C to +150°C
Reflow ³ (Moisture Sensitivity Level 3 (MSL3) Rating)	260°C
Electrostatic Discharge (ESD) Sensitivity Human Body Model (HBM)	250 V (Class 1A)

¹ For power derating at frequencies less than 250 MHz, see Figure 2.

² See Figure 3.

³ See the Ordering Guide for more information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

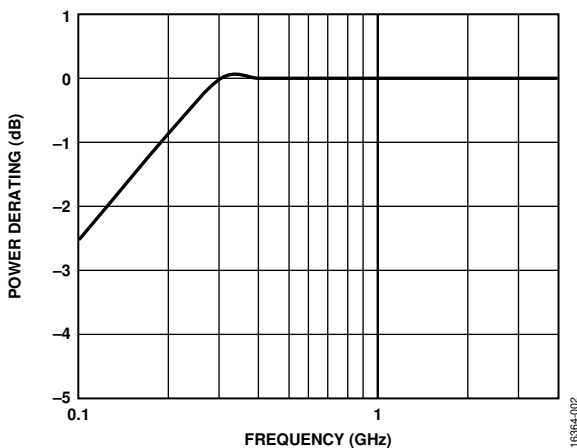


Figure 2. Power Derating at Frequencies Less Than 250 MHz

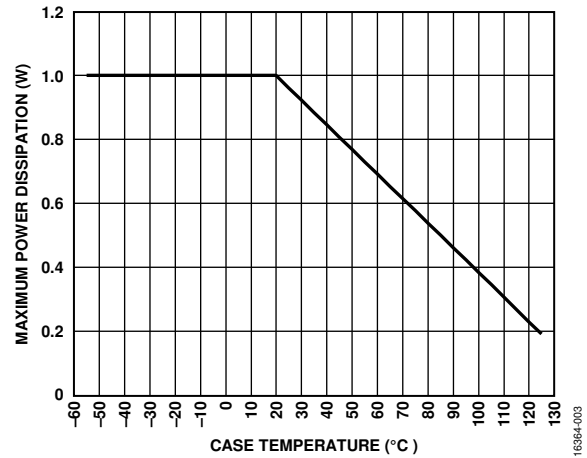


Figure 3. Maximum Power Dissipation vs. Case Temperature

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the junction to ambient air thermal resistance, and θ_{JC} is the junction to case thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-16-51 ¹	297	130 ²	°C/W

¹ Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with five thermal vias. See JEDEC JESD-51.

² The device is set to maximum attenuation state.

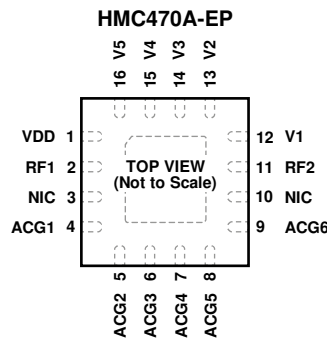
ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



- NOTES**
 1. NIC = THESE PINS ARE NOT INTERNALLY CONNECTED; HOWEVER, ALL DATA SHOWN HEREIN WAS MEASURED WHEN THESE PINS CONNECTED TO RF/DC GROUND OF EVALUATION BOARD.
 2. EXPOSED PAD. THE EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

16384-004

Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VDD	Power Supply. See Figure 6 for the interface schematic.
2	RF1	RF Input or Output of the Attenuator. The RF1 pin is dc-coupled to VDD and ac matched to 50 Ω. An external dc blocking capacitor is required. Select the capacitor value for the lowest frequency of operation. See Figure 5 for the interface schematic.
3, 10	NIC	Not Internally Connected. These pins are not internally connected; however, all data shown herein was measured when these pins were connected to the RF/dc ground of the evaluation board.
4 to 9	ACG1 to ACG6	AC Grounding Capacitor Pins. Leave these pins not connected when operating above 700 MHz. For frequencies less than 700 MHz, connect capacitors larger than 100 pF as close to the ACGx pins as possible. Select the capacitor value for the lowest frequency of operation.
11	RF2	RF Input or Output of the Attenuator. The RF2 pin is dc-coupled to VDD and ac matched to 50 Ω. An external dc blocking capacitor is required. Select the capacitor value for the lowest frequency of operation. See Figure 5 for the interface schematic.
12 to 16	V1 to V5	Parallel Control Voltage Inputs. These pins select the required attenuation (see Table 5). See Figure 6 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to ground for proper operation.

Table 5. P4 to P0 Truth Table

Digital Control Input ¹					Attenuation State (dB)
V1	V2	V3	V4	V5	
High	High	High	High	High	0 (reference)
High	High	High	High	Low	1
High	High	High	Low	High	2
High	High	Low	High	High	4
High	Low	High	High	High	8
Low	High	High	High	High	16
Low	Low	Low	Low	Low	31

¹ Any combination of the control voltage input states shown in Table 5 provides an attenuation equal to the sum of the bits selected.

INTERFACE SCHEMATICS

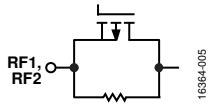


Figure 5. RF1, RF2 Interface Schematic

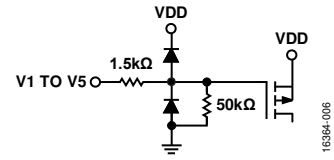


Figure 6. Digital Control Input Interface

TYPICAL PERFORMANCE CHARACTERISTICS

See the [HMC470A](#) data sheet for a full set of the Typical Performance Characteristics plots.

INPUT POWER COMPRESSION AND INSERTION LOSS

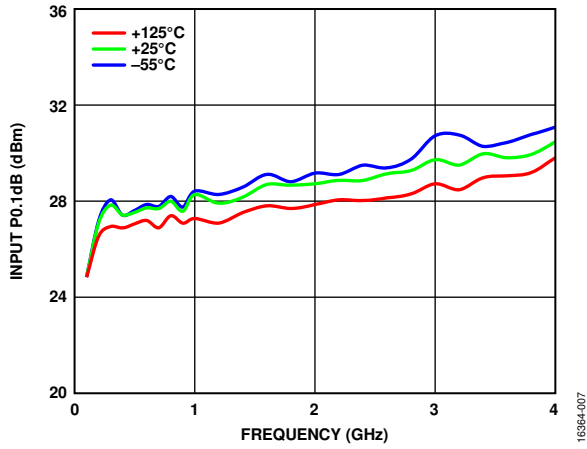


Figure 7. Input P0.1dB vs. Frequency at Minimum Attenuation State for Various Temperatures, $V_{DD} = 5\text{ V}$

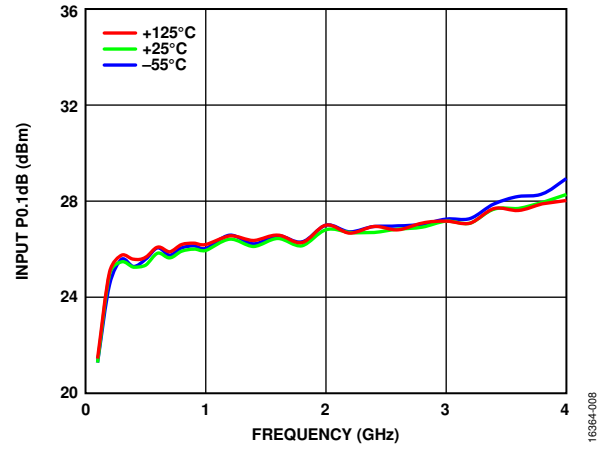


Figure 9. Input P0.1dB vs. Frequency at Minimum Attenuation State for Various Temperatures, $V_{DD} = 3\text{ V}$

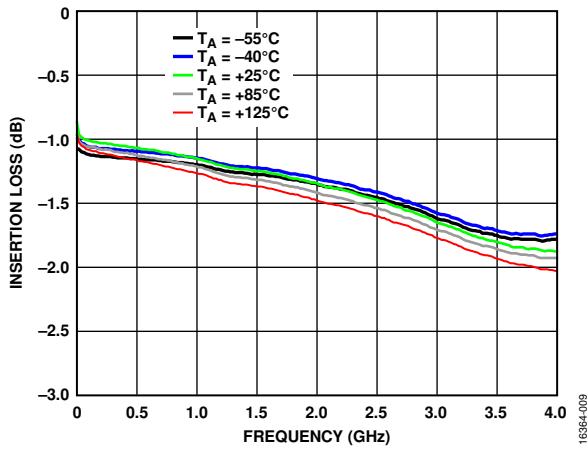
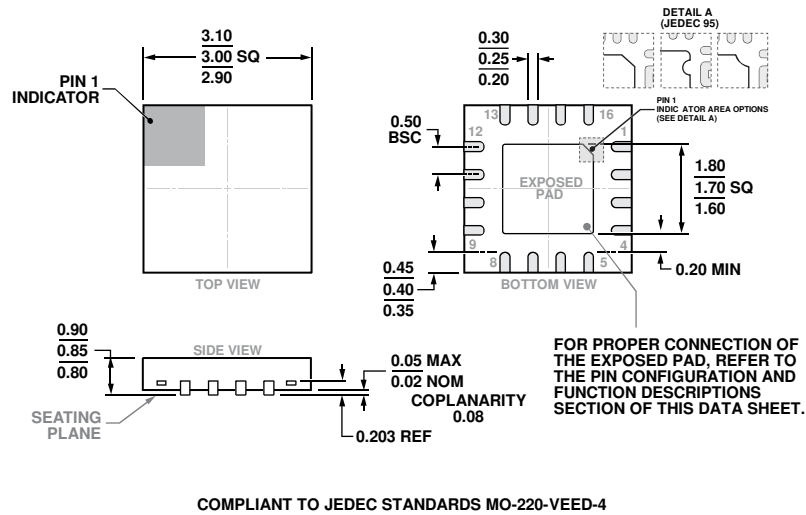


Figure 8. Insertion Loss vs. Frequency for Various Temperatures

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VEED-4

Figure 10. 16-Lead Lead Frame Chip Scale Package [LFCSP]
 3 mm × 3 mm Body and 0.85 mm Package Height
 (CP-16-51)

Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	MSL Rating ²	Package Description	Package Option	Branding
HMC470ATCPZ-EP-PT	-55°C to +125°C	MSL3	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-51	Y6U
HMC470ATCPZ-EP-RL7	-55°C to +125°C	MSL3	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-51	Y6U

¹ The HMC470ATCPZ-EP-PT and the HMC470ATCPZ-EP-RL7 models are RoHS Compliant.
² See the Absolute Maximum Ratings section.