Power Sequencing Controllers

The Intersil ISL6123, ISL6124, ISL6125, ISL6126, ISL6127, ISL6128 and ISL6130 are integrated four channel controlled-on/controlled-off power-supply sequencers with supply monitoring, fault protection and a “sequence completed” signal ($\overline{\text{RESET}}$). For larger systems, more than four supplies can be sequenced by simply connecting a wire between $\overline{\text{SYSRESET}}$ pins of cascaded IC's. The ISL6125 uses four open-drain outputs to control the on/off sequencing of four supplies, while the other sequencers use a patented, micropower 7x charge pump to drive four external low-cost NFET switch gates above the supply rail by 5.3V. These IC's can be biased from any supply 5V down to 1.5V. Individual product descriptions follow.

The four channel ISL6123 (ENABLE input), ISL6124 ($\overline{\text{ENABLE}}$ input) and ISL6125 ICs offer the designer 4 rail control when it is required that all four rails are in minimal compliance prior to turn on and that compliance must be maintained during operation. The ISL6123 and ISL6130 have a low power standby mode when disabled, suitable for battery powered applications.

The ISL6125 operates like the ISL6124 but instead of charge pump driven gate drive outputs it has open drain logic outputs for direct interface to other circuitry.

In contrast to the majority, for both the ISL6126 and ISL6130 each of the four channels operate independently so that the various GATEs will turn on once its individually associated input voltage requirements are met.

The ISL6127 is a pre-programmed A-B-C-D turn-on and D-C-B-A turn-off sequenced IC. Once all inputs are in compliance and $\overline{\text{ENABLE}}$ is asserted, the sequencing starts and each subsequent GATE will turn-on after the previous one completes turning-on.

The ISL6128 has two groups of two channels each with its independent I/O and is ideal for voltage sequencing into redundant capability loads as all four inputs need to be satisfied prior to turn on but a single group fault is ignored by the other group.

External resistors provide flexible voltage threshold programming of monitored rail voltages. Delay and sequencing are provided by external capacitors for both ramp-up and ramp-down.

Additional I/O is provided indicating and driving RESET state in various configurations.

For volume applications, other programmable options and features can be had. Contact the factory with your needs.

Features

- Enables Arbitrary Turn-on and Turn-off Sequencing of Up to Four Power Supplies (0.7V to 5V)
- Operates From 1.5V to 5V Supply Voltage
- Supplies V_{DD} +5.3V of Charge Pumped Gate Drive
- Adjustable Voltage Slew Rate for Each Rail
- Multiple Sequencers Can be Daisy-Chained to Sequence an Infinite Number of Independent Supplies
- Glitch Immunity
- Undervoltage Lockout for Each Supply
- 1µA Sleep State (ISL6123, ISL6130)
- Active High (ISL6123, ISL6130) or Low (ISL6124, ISL6125, ISL6126, ISL6127, ISL6128) $\overline{\text{ENABLE}}$ Input
- Open Drain Version Available (ISL6125)
- Voltage Determined Sequence (ISL6126, ISL6130)
- Pre-programmed Sequence Available (ISL6127)
- Dual Channel Groupings (ISL6128)
- QFN Package
- Pb-Free Available (RoHS compliant)

Applications

- Graphics Cards
- FPGA/ASIC/microprocessor/PowerPC Supply Sequencing
- Network Routers
- Telecommunications Systems

Ordering Information

PART NUMBER (Note 1)	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6123IR	ISL 6123IR	-40 to +85	24 Ld 4x4 QFN	L24.4x4
ISL6124IR	ISL 6124IR	-40 to +85	24 Ld 4x4 QFN	L24.4x4
ISL6125IR	ISL 6125IR	-40 to +85	24 Ld 4x4 QFN	L24.4x4
ISL6126IR	ISL 6126IR	-40 to +85	24 Ld 4x4 QFN	L24.4x4
ISL6127IR	ISL 6127IR	-40 to +85	24 Ld 4x4 QFN	L24.4x4
ISL6128IR	ISL 6128IR	-40 to +85	24 Ld 4x4 QFN	L24.4x4
ISL6123IRZA (Note 2)	61 23IRZ	-40 to +85	24 Ld 4x4 QFN (Pb-free)	L24.4x4
ISL6124IRZA (Note 2)	61 24IRZ	-40 to +85	24 Ld 4x4 QFN (Pb-free)	L24.4x4
ISL6125IRZA (Note 2)	61 25IRZ	-40 to +85	24 Ld 4x4 QFN (Pb-free)	L24.4x4
ISL6126IRZA (Note 2)	61 26IRZ	-40 to +85	24 Ld 4x4 QFN (Pb-free)	L24.4x4
ISL6127IRZA (Note 2)	61 27IRZ	-40 to +85	24 Ld 4x4 QFN (Pb-free)	L24.4x4
ISL6128IRZA (Note 2)	61 28IRZ	-40 to +85	24 Ld 4x4 QFN (Pb-free)	L24.4x4
ISL6130IRZA (Note 2)	61 30IRZ	-40 to +85	24 Ld 4x4 QFN (Pb-free)	L24.4x4
ISL612XSEQEVAL1Z	ISL612X Pb Free Evaluation Platform			
ISL6125EVAL1Z	ISL6125 Pb Free Evaluation Platform			

NOTES:

1. Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

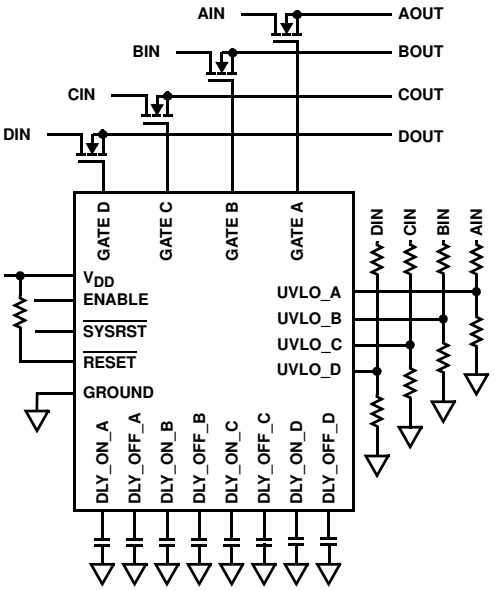


FIGURE 1. TYPICAL ISL6123 APPLICATION USAGE

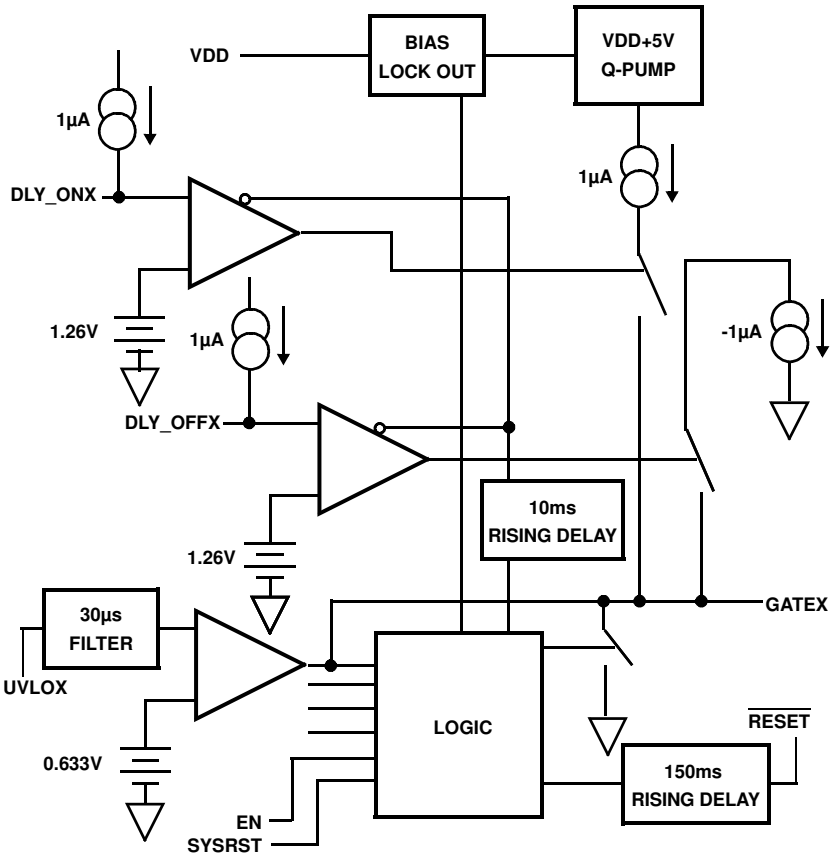
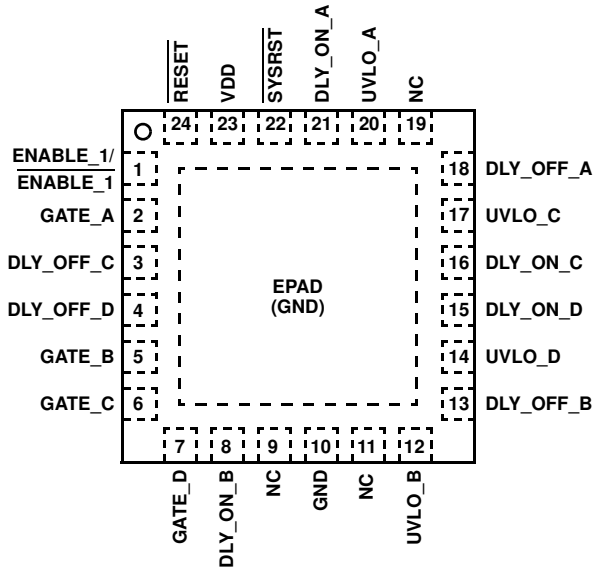


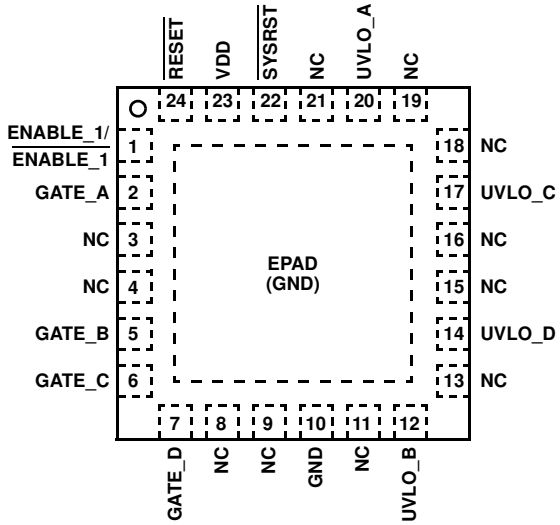
FIGURE 2. ISL6123 BLOCK DIAGRAM (1/4)

Pinouts

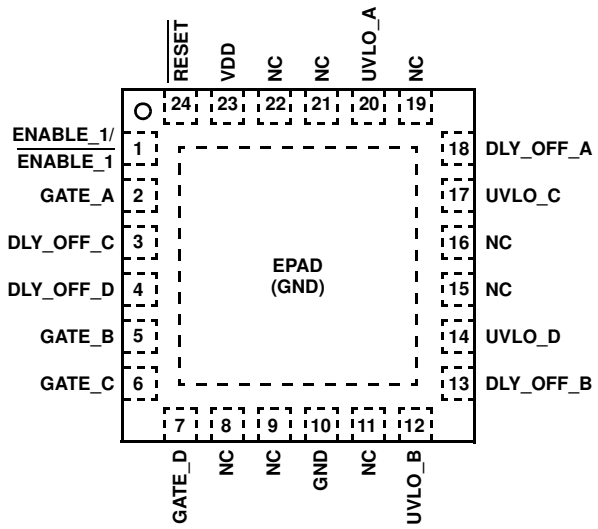
ISL6123, ISL6124, ISL6125
(24 LD QFN)
TOP VIEW



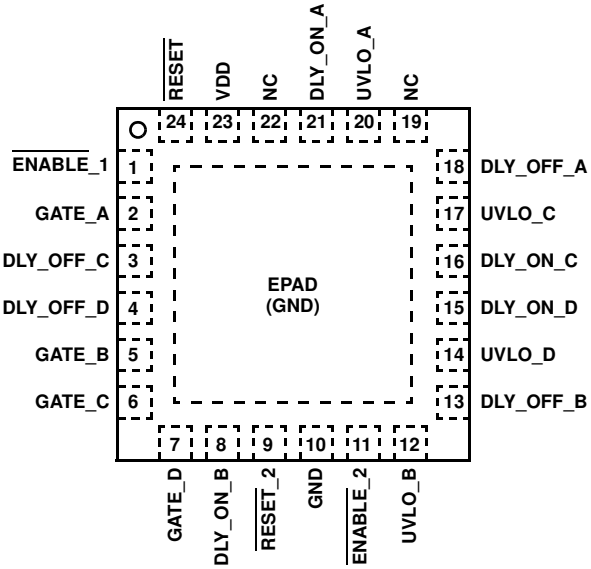
ISL6127
(24 LD QFN)
TOP VIEW



ISL6126, ISL6130
(24 LD QFN)
TOP VIEW



ISL6128
(24 LD QFN)
TOP VIEW



Pin Descriptions

PIN NAME	PIN NUMBER				DESCRIPTION
	ISL6123, ISL6124, ISL6125	ISL6126, ISL6130	ISL6127	ISL6128	
VDD	23	23	23	23	Chip Bias. Bias IC from nominal 1.5V to 5V
GND	10	10	10	10	Bias Return. IC ground
ENABLE_1/ $\overline{\text{ENABLE\_1}}$	1	1	1	1	Input to start on/off sequencing. Input to initiate the start of the programmed sequencing of supplies on or off. Enable functionality is disabled for 10ms after UVLO is satisfied. ISL6123 and ISL6130 have $\overline{\text{ENABLE}}$. ISL6124, ISL6125, ISL6126 and ISL6127 have $\overline{\text{ENABLE}}$. Only ISL6128 has 2 $\overline{\text{ENABLE}}$ inputs; 1 for each 2 channel grouping. $\overline{\text{ENABLE\_1}}$ for (A, B), and $\overline{\text{ENABLE\_2}}$ for (C, D).
ENABLE_2/ $\overline{\text{ENABLE\_2}}$	NC	NC	NC	11	
$\overline{\text{RESET}}$	24	24	24	24	$\overline{\text{RESET}}$ Output. $\overline{\text{RESET}}$ provides a low signal 150ms after all GATEs are fully enhanced. This delay is for stabilization of output voltages. $\overline{\text{RESET}}$ will assert low upon UVLO not being satisfied or ENABLE/$\overline{\text{ENABLE}}$ being deasserted. The RESET outputs are open drain N-channel FET and is guaranteed to be in the correct state for VDD down to 1V and is filtered to ignore fast transients on VDD and UVLO_X. $\overline{\text{RESET\_2}}$ only exists on ISL6128 for (C, D) group I/O.
$\overline{\text{RESET\_2}}$	NC	NC	NC	9	
UVLO_A	20	20	20	20	Undervoltage Lock Out/Monitoring Input. These inputs provide for a programmable UV lockout referenced to an internal 0.633V reference and are filtered to ignore short (<30µs) transients below programmed UVLO level.
UVLO_B	12	12	12	12	
UVLO_C	17	17	17	17	
UVLO_D	14	14	14	14	
DLY_ON_A	21	-	-	21	Gate On Delay Timer Output. Allows for programming the delay and sequence for VOUT turn-on using a capacitor to ground. Each capacitor is charged with 1µA, 10ms after turn-on initiated by ENABLE/$\overline{\text{ENABLE}}$ with an internal current source providing delay to the associated FETs GATE turn-on.
DLY_ON_B	8	-	-	8	
DLY_ON_C	16	-	-	16	
DLY_ON_D	15	-	-	15	
DLY_OFF_A	18	18	-	18	Gate Off Delay Timer Output. Allows for programming the delay and sequence for VOUT turn-off through ENABLE/$\overline{\text{ENABLE}}$ via a capacitor to ground. Each capacitor is charged with a 1µA internal current source to an internal reference voltage causing the corresponding gate to be pulled down turning-off the FET.
DLY_OFF_B	13	13	-	13	
DLY_OFF_C	3	3	-	3	
DLY_OFF_D	4	4	-	4	
GATE_A	2	2	2	2	FET Gate Drive Output. Drives the external FETs with a 1µA current source to soft-start ramp into the load. On the ISL6125 only, these are open drain outputs that can be pulled up to a maximum of VDD voltage.
GATE_B	5	5	5	5	
GATE_C	6	6	6	6	
GATE_D	7	7	7	7	
$\overline{\text{SYSRST}}$	22	-	22	-	System Reset I/O. As an input, allows for immediate and unconditional latch-off of all GATE outputs when driven low. This input can also be used to initiate the programmed sequence with ‘zero’ wait (no 10ms stabilization delay) from input signal on this pin being driven high to first GATE. As an output when there is a UV condition, this pin pulls low. If common to other $\overline{\text{SYSRST}}$ pins in a multiple IC configuration, it will cause immediate and unconditional latch-off of all other GATEs on all other ISL612X sequencers.
GND	EPAD	EPAD	EPAD	EPAD	Ground. Die Substrate
NC	9, 19	8, 9, 11, 15, 16, 19, 21, 22	3, 4, 8, 9, 11, 13, 15,16,18, 19, 21	19, 22	No Connect

ISL612X Variant Feature Matrix

PART NAME	EN/$\overline{EN}$	CMOS/ TTL	GATE DRIVE OR OPEN DRAIN OUTPUTS	REQUIRED CONDITIONS FOR INITIAL START-UP	NUMBER OF UVLO INPUTS MONITORED BY EACH $\overline{RESET}$	NUMBER OF CHANNELS THAT TURN-OFF WHEN 1 UVLO FAULTS	PRESET OR ADJUSTABLE SEQUENCE	NUMBER OF UVLO AND PAIRS OF I/O	FEATURES
ISL6123	EN	TTL	Gate Drive	4 UVLO 1 EN	4 UVLO	4 Gates	Time Adjustable On and Off	4 Monitors with 1 I/O	Auto Restart, Low Bias Current Sleep
ISL6124	EN	CMOS	Gate Drive	4 UVLO 1 EN	4 UVLO	4 Gates	Time Adjustable On and Off	4 Monitors with 1 I/O	Auto Restart
ISL6125	EN	CMO	Open Drain	4 UVLO 1 EN	4 UVLO	4 Open Drain	Time Adjustable On and Off	4 Monitors with 1 I/O	Auto Restart, Open Drain Sequenced Outputs
ISL6126	EN	CMOS	Gate Drive	1 UVLO 1 EN	4 UVLO	1 Gate	Voltage Determined ON Time Adjustable Off	4 Monitors with 1 I/O	Gates Independent On as UVLO Valid
ISL6127	EN	CMOS	Gate Drive	4 UVLO 1 EN	4 UVLO	4 Gates	Preset	4 Monitors with 1 I/O	Auto Restart
ISL6128	EN	CMOS	Gate Drive	4 UVLO 2 EN	2 UVLO	2 Gates	Preset	2 Monitors with 2 I/O	Dual Redundant Operation
ISL6130	EN	TTL	Gate Drive	1 UVLO 1 EN	4 UVLO	1 Gate	Voltage Determined ON Time Adjustable Off	4 Monitors with 1 I/O	Gates Independent On as UVLO Valid Low Bias Current Sleep

Absolute Maximum Ratings

V_{DD} . . . . . +6.0V
GATE . . . . . -0.3V to V_{DD}+6V
ISL6125 LOGIC OUT. . . . . -0.3V to V_{DD} + 0.3V
UVLO, ENABLE, $\overline{\text{ENABLE}}$, SYSRST . . . . . -0.3V to V_{DD} + 0.3V
$\overline{\text{RESET}}$, DLY_ON, DLYOFF . . . . . -0.3V to V_{DD} + 0.3V

Operating Conditions

V_{DD} Supply Voltage Range . . . . . +1.5V to +5.5V
Temperature Range (T_A) . . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical, Notes 3, 4)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
24 Ld 4x4 QFN Package	48	9

Maximum Junction Temperature . . . . . +125°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
4. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
5. All voltages are relative to GND, unless otherwise specified.

Electrical Specifications

V_{DD} = 1.5V to +5V, T_A = T_J = -40°C to +85°C, unless otherwise specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
UVLO						
Falling Undervoltage Lockout Threshold	$V_{UVLOvth}$	T_J = +25°C	619	633	647	mV
Undervoltage Lockout Threshold Tempco	$TC_{UVLOvth}$			40		nV/°C
Undervoltage Lockout Hysteresis	$V_{UVLOhys}$			10		mV
Undervoltage Lockout Threshold Range	RUVLOvth	Max $V_{UVLOvth}$- Min $V_{UVLOvth}$		7		mV
Undervoltage Lockout Delay	TUVLOdel	ENABLE satisfied		10		ms
Transient Filter Duration	t_{FIL}	V_{DD}, UVLO, ENABLE glitch filter		30		µs
DELAY ON/OFF						
Delay Charging Current	DLY_ichg	V_{DLY} = 0V	0.92	1	1.08	µA
Delay Charging Current Range	DLY_ichg_r	DLY_ichg(max) - DLY_ichg(min)		0.08		µA
Delay Charging Current Temperature Coefficient	TC_DLY_ichg			0.2		nA/°C
Delay Threshold Voltage	DLY_Vth		1.238	1.266	1.294	V
Delay Threshold Voltage Temperature Coefficient	TC_DLY_Vth			0.2		mV/°C
ENABLE/$\overline{\text{ENABLE}}$, $\overline{\text{RESET}}$ AND $\overline{\text{SYSRST}}$ I/O						
ENABLE Threshold	V_{ENh}			1.2		V
$\overline{\text{ENABLE}}$ Threshold	V_{ENh}			0.5 V_{DD}		V
ENABLE/$\overline{\text{ENABLE}}$ Hysteresis	V_{ENh} - V_{ENl}	Measured at V_{DD} = 1.5V		0.2		V
ENABLE/$\overline{\text{ENABLE}}$ Lockout Delay	t_{delEN_LO}	UVLO satisfied		10		ms
ENABLE/$\overline{\text{ENABLE}}$ Input Capacitance	Cin_en			5		pF
$\overline{\text{RESET}}$ Pull-up Voltage	Vpu_rst			V_{DD}		V
$\overline{\text{RESET}}$ Pull-Down Current	$I_{\overline{RST}pd1}$	V_{DD} = 1.5V, $\overline{\text{RST}}$ = 0.1V		5		mA
	$I_{\overline{RST}pd3}$	V_{DD} = 3.3V, $\overline{\text{RST}}$ = 0.1V		13		mA
	$I_{\overline{RST}pd5}$	V_{DD} = 5V, $\overline{\text{RST}}$ = 0.1V		17		mA
$\overline{\text{RESET}}$ Delay after GATE High	$T_{\overline{RST}del}$	GATE = V_{DD}+5V		160		ms

Electrical Specifications V_{DD} = 1.5V to +5V, $T_A = T_J$ = -40°C to +85°C, unless otherwise specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\overline{\text{RESET}}$ Output Low	$V_{\overline{RST}l}$	Measured at V_{DD} = 5V with 5k pull-up resistors			0.1	V
RESET Output Capacitance	C_{OUT_RST}			10		pF
$\overline{\text{SYSRST}}$ Pull-Up Voltage	Vpu_srst			V_{DD}		V
$\overline{\text{SYSRST}}$ Pull-Down Current	Ipu_1.5	V_{DD} = 1.5V		5		µA
	Ipu_5	V_{DD} = 5V		100		µA
$\overline{\text{SYSRST}}$ Low Output Voltage	Vol_srst	V_{DD} = 1.5V, I_{OUT} = 100µA		150		mV
$\overline{\text{SYSRST}}$ Output Capacitance	Cout_srst			10		pF
$\overline{\text{SYSRST}}$ Low to GATE Turn-Off	t_{delSYS_G}	GATE = 80% of V_{DD} + 5V		40		ns
GATE						
GATE Turn-On Current	I_{GATEon}	GATE = 0V	0.8	1.1	1.4	µA
GATE Turn-Off Current	$I_{GATEoff\_l}$	GATE = V_{DD}, Disabled	-1.4	-1.05	-0.8	µA
GATE Current Range	I_{GATE_range}	Within IC I_{GATE} max-min			0.35	µA
GATE Turn-On/Off Current Temperature Coefficient	TC_I_{GATE}			0.2		nA/°C
GATE Pull-Down High Current	$I_{GATEoff\_h}$	GATE = V_{DD}, UVLO = 0V		88		mA
GATE High Voltage	V_{GATEh}	V_{DD} < 2V, T_J = +25°C		V_{DD} + 4.9V		V
	V_{GATEh}	V_{DD} > 2V	V_{DD} + 5V	V_{DD} + 5.3V		V
GATE Low Voltage	V_{GATEl}	Gate Low Voltage, V_{DD} = 1V		0	0.1	V
BIAS						
IC Supply Current	I_{VDD_5V}	V_{DD} = 5V		0.20	0.5	mA
	$I_{VDD\_3.3V}$	V_{DD} = 3.3V		0.14		mA
	$I_{VDD\_1.5V}$	V_{DD} = 1.5V		0.10		mA
ISL6123, ISL6130 Stand By IC Supply Current	I_{VDD_sb}	V_{DD} = 5V, ENABLE = 0V			1	µA
V_{DD} Power-on Reset	$V_{DD\_}POR$				1	V

Descriptions and Operation

The ISL612X sequencer family consists of several four channel voltage sequencing controllers in various functional and personality configurations. All are designed for use in multiple-voltage systems requiring power sequencing of various supply voltages. Individual voltage rails are gated on and off by external N-Channel MOSFETs, the gates of which are driven by an internal charge pump to VDD + 5.3V (VQP) in a user programmed sequence.

With the four-channel ISL6123 the ENABLE must be asserted high and all four voltages to be sequenced must be above their respective user programmed Undervoltage Lock Out (UVLO) levels before programmed output turn on sequencing can begin. Sequencing and delay determination is accomplished by the choice of external capacitor values on the DLY_ON and DLY_OFF pins. Once all four UVLO inputs and ENABLE are satisfied for 10ms, the four DLY_ON capacitors are simultaneously charged with 1µA current sources to the DLY_Vth level of 1.27V. As each DLY_ON pin reaches the DLY_Vth level its associated GATE will then turn-on with a 1µA source current to the VQP voltage of V_{DD} + 5.3V. Thus, all four GATEs will sequentially turn-on. Once at DLY_Vth the DLY_ON pins will discharge to be ready when next needed. After the entire turn on sequence has been completed and all GATEs have reached the charge pumped voltage (VQP), a 160ms delay is started to ensure stability after which the $\overline{\text{RESET}}$ output will be released to go high. Subsequent to turn-on, if any input falls below its UVLO point for longer than the glitch filter period (~30µs) this is considered a fault. $\overline{\text{RESET}}$ and $\overline{\text{SYSRST}}$ are pulled low and all GATEs are simultaneously also pulled low. In this mode the GATEs are pulled low with 88mA. Normal shutdown mode is entered when no UVLO is violated and the ENABLE is deasserted. When ENABLE is deasserted, $\overline{\text{RESET}}$ is

asserted and pulled low. Next, all four shutdown ramp capacitors on the DLY_OFF pins are charged with a 1µA source and when any ramp-capacitor reaches DLY_Vth, a latch is set and a current is sunk on the respective GATE pin to turn off its external MOSFET. When the GATE voltage is approximately 0.6V, the GATE is pulled down the rest of the way at a higher current level. Each individual external FET is thus turned off removing the voltages from the load in the programmed sequence.

The ISL6123 and ISL6124 have the same functionality except for the ENABLE active polarity with the ISL6124 having an $\overline{\text{ENABLE}}$ input. Additionally, the ISL6123 and ISL6130 also have an ultra low power sleep state when ENABLE is low.

The ISL6125 has the same personality as the ISL6124 but instead of charged pump driven GATE outputs it has open drain outputs that can be pulled up to a maximum of VDD.

The ISL6126 and ISL6130 are different in that their sequence on is not time determined but voltage determined. Each of the four channels operates independently so that once the IC is biased and any one of the UVLO inputs is greater than the 0.63V internal reference, the enable input is also satisfied and the GATE for the associated UVLO input will turn-on. In turn, the other UVLO inputs need to be satisfied for the associated GATEs to turn-on. 150ms after all GATEs are fully on (GATE voltage = VQP), the $\overline{\text{RESET}}$ is released to go high. The UVLO inputs can be driven by either a previously turned on output rail offering a voltage determined sequence or by logic signal inputs. Any subsequent UVLO level < its programmed level will pull the associated GATE and $\overline{\text{RESET}}$ output low (if previously released), but will not latch-off the other GATEs. Predetermined turn-off is accomplished by deasserting enable, this will cause $\overline{\text{RESET}}$ to latch low and all four GATE outputs to follow the programmed turn off sequence similar to ISL6124.

The ISL6127 is a four-channel sequencer pre-programmed for A-B-C-D turn-on and D-C-B-A turn-off. After all four UVLO and ENABLE inputs are satisfied for ~10ms, the sequencing starts and the next GATE in the sequence starts to ramp-up once the previous GATE has reached ~VQP-1V. 160ms after the last GATE is at VQP, the $\overline{\text{RESET}}$ output will be deasserted. Once any UVLO is unsatisfied, $\overline{\text{RESET}}$ is pulled low, SYSRST is pulled low and all GATEs are simultaneously turned off. When $\overline{\text{ENABLE}}$ is signaled high the D GATE will start to pull low and once below 0.6V the next GATE will then start to pull low and so on until all GATEs are at 0V. Unloaded, this turn off sequence will complete in <1ms. This variant offers a lower cost and size implementation as the external delay capacitors are not used. Since the delay capacitors are not used, this IC cannot delay the start of subsequent GATEs, thus necessary stabilization or system house keeping need to be considered.

The ISL6128 is a four-channel device that groups the four channels into two groups of two channels each, as A, B and C, D, each group having its own $\overline{\text{ENABLE}}$ and $\overline{\text{RESET}}$ I/IO pins. This requires all four UVLO and both $\overline{\text{ENABLE}}$s to be satisfied for sequencing to start. The A, B group will first turn on 10ms after the second $\overline{\text{ENABLE}}$ is pulled low with A then B turning on followed by C then D. Once the preceding GATE = VQP the next DLY_ON pin starts to charge its capacitor thus turning on all four GATEs. Approximately 160ms after D GATE = VQP the $\overline{\text{RESET}}$ output is released to go high. Once any UVLO is unsatisfied, only the related group's $\overline{\text{RESET}}$ and two GATEs are pulled low. The related EN input has to be cycled for the faulted group to be turned-on again. Normal shutdown is invoked by either signaling both $\overline{\text{ENABLE}}$ inputs high which will cause all the two related GATEs to shutdown in reverse order from turn-on. DLY_X capacitors adjust the delay between GATES during turn on and off but not the order.

During bias up the $\overline{\text{RESET}}$ output is guaranteed to be in the correct state with VDD lower than 1V.

The SYSRST pin follows the VDD upon power-up with a weak internal pull-up and is both an input and output connection providing two functions. As an input, if it is pulled low, all GATEs will be unconditionally shut off and $\overline{\text{RESET}}$ pulls low, (see Figure 7). This input can also be used as a no wait enabling input, if all inputs (ENABLE and UVLO) are satisfied, it does not wait through the ~10ms enable delay to initiate DLY_ON capacitor charging when released to go high. As an output, it is useful when implementing multiple sequencers in a design needing simultaneous shutdown as with a kill switch across all sequencers. Once any UVLO is unsatisfied longer than tFIL the related $\overline{\text{SYSRST}}$ will pull low and pull all other $\overline{\text{SYSRST}}$ inputs low that are on a common connection thus unconditionally shutting down all outputs across multiple sequencers.

Except for the ISL6128 after a fault, restart of the turn-on sequence is automatic once all requirements are met. This allows for no interaction between the sequencer and a controller IC if desired. The ENABLE and $\overline{\text{RESET}}$ I/O do allow for a higher level of feedback and control if desired. The ISL6128 requires that the related $\overline{\text{ENABLE}}$ be cycled for restart of its associated group GATEs. If no capacitors are connected between DLY_ON or DLY_OFF pins and ground then all such related GATEs start to turn on immediately after the 10ms (TUVLOdel) ENABLE stabilization time out has expired and the GATEs start to immediately turn off when ENABLE is asserted.

If some of the rails are to be sequenced together in order to eliminate the effect of capacitor variance on the timing and to reduce cost, a common capacitor can be connected to two or more DLY_ON or DLY_OFF pins. In this case multiply the capacitor value by the number of common DLY_X pins to retain the desired timing.

Table 1 illustrates the nominal time delay from the start of

charging to the 1.27V reference for various capacitor values on the DLY_X pins. This table does not include the 10ms of enable lock out delay during a start-up sequence but represents the time from the end of the enable lock out delay to the start of GATE transition. There is no enable lock out delay for a sequence off, so this table illustrates the delay to GATE transition from a disable signal.

TABLE 1.

NOMINAL DELAY TO SEQUENCING THRESHOLD	
DLY PIN CAPACITANCE	**TIME(s)**
Open	0.00006
100pF	0.00013
1000pF	0.0013
0.01µF	0.013
0.1µF	0.13
1µF	1.3

TABLE 1.

NOMINAL DELAY TO SEQUENCING THRESHOLD	
DLY PIN CAPACITANCE	**TIME(s)**
10µF	13

NOTE: Nom. T_{DEL_SEQ} = Capacitor (µF)*1.3MΩ.

Figure 3 illustrates the turn-on and Figure 4 illustrates the nominal turnoff timing diagram of the ISL6123 and ISL6124 product.

The ISL6125 is similar to the ISL6124 except that instead of charge pumped GATE outputs, there are sequenced open drain outputs that can be pulled up to a maximum of VDD.

Note the delay and flexible sequencing possibilities. Multiple series, parallel or adjustable capacitors can be used to easily fine tune timing between that offered by standard value capacitors.

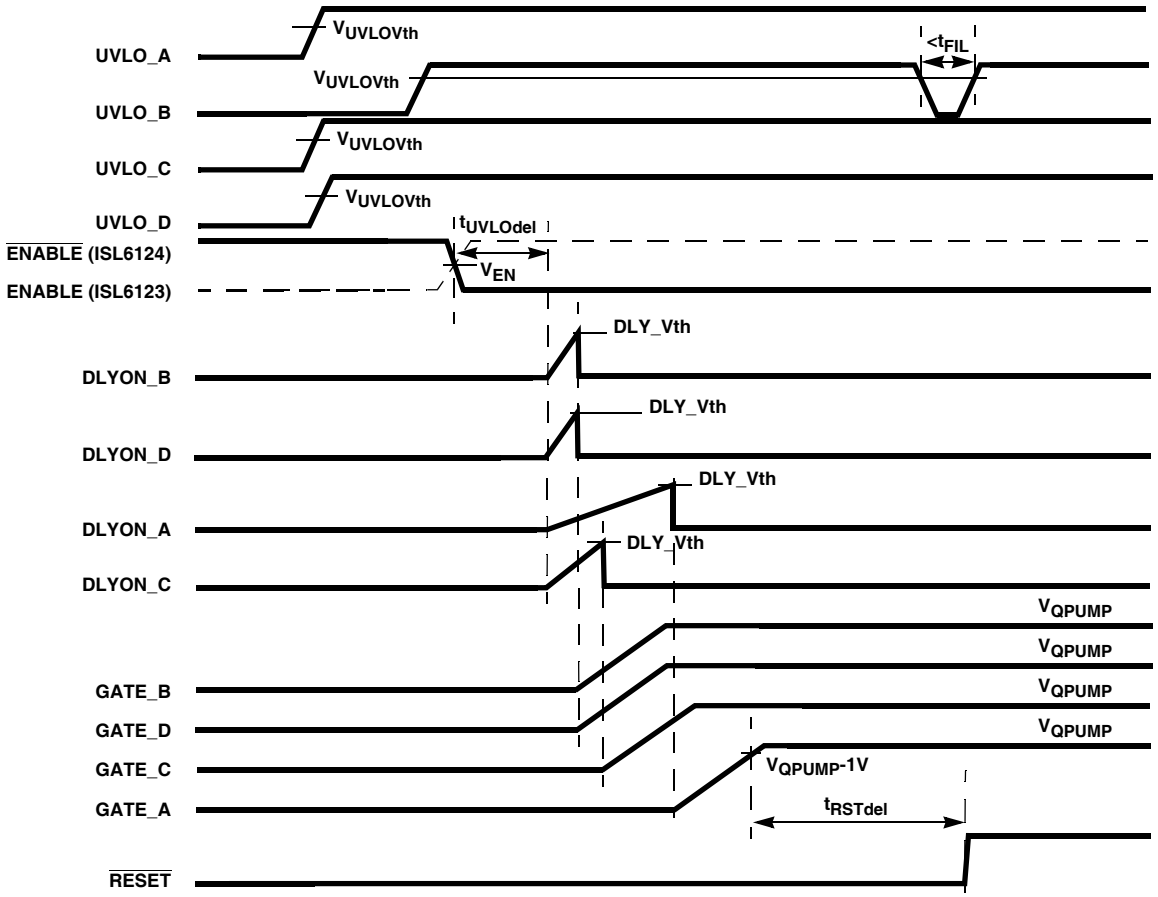


FIGURE 3. ISL6123, ISL6124 TURN-ON AND GLITCH RESPONSE TIMING DIAGRAM

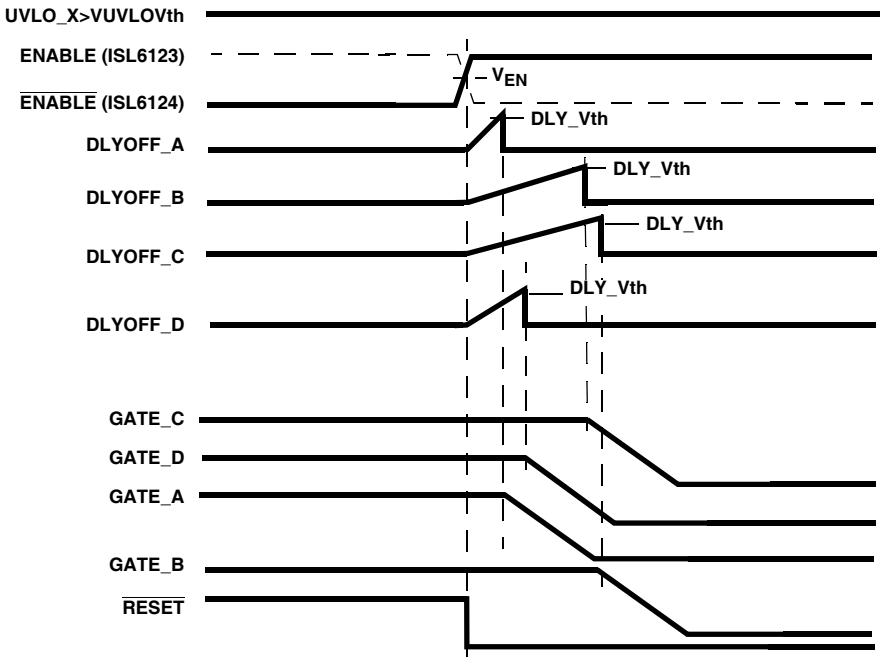


FIGURE 4. ISL6123, ISL6124 TURN-OFF TIMING DIAGRAM

Typical Performance Curves

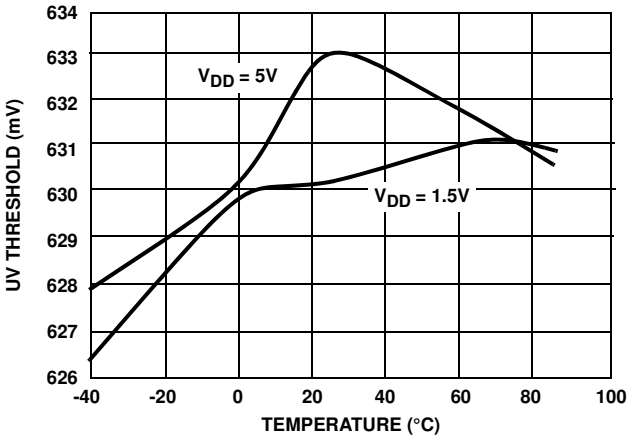


FIGURE 5. UVLO THRESHOLD VOLTAGE

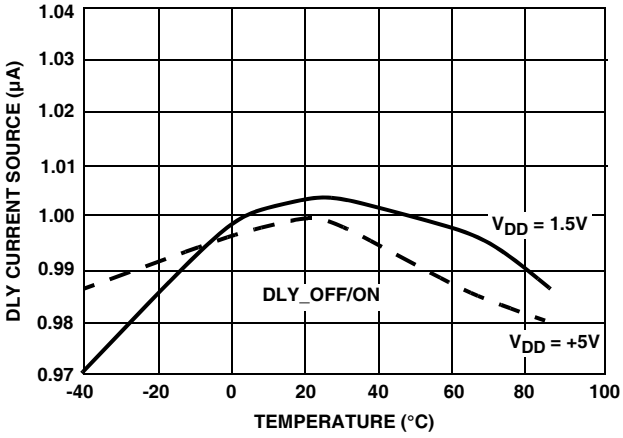


FIGURE 6. DLY CHARGE CURRENT

Typical Performance Curves (Continued)

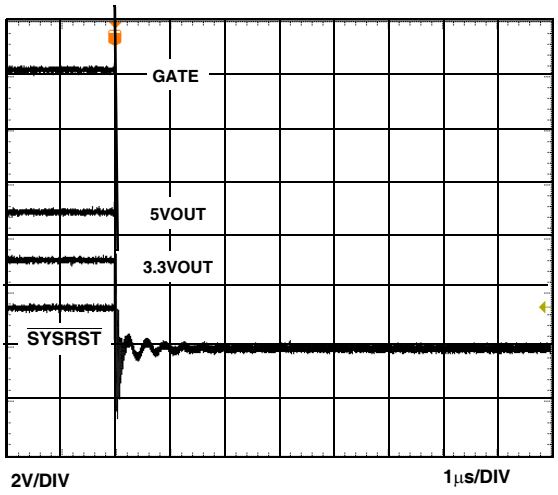


FIGURE 7. $\overline{\text{SYSRST}}$ LOW TO OUTPUT LATCH OFF

Using the ISL612XSEQEVAL1Z Platform

The ISL612XSEQEVAL1Z platform is the primary evaluation board for this family. The board has two complete, separate and electrically identical circuits. See Figure 16 for its schematic and photograph. Additionally, there is an ISL6125 specific evaluation platform, ISL6125EVAL1Z, due to its unique open drain outputs for ease of evaluation. See Figure 17 for its schematic and photograph.

In the top right hand corner of the board is a SMD layout with ISL6123 illustrating the full functionality and small implementation size for an application having the highest component count.

The majority of the board is given over to a socket and discrete through-hole components circuit for ease of evaluation flexibility through IC variant swapping and modification of UVLO levels and sequencing order by passive component substitution.

The board is shipped with the ISL6123 installed in both locations and with two each of the other released variant types loose packed. As this sequencer family has a common function pinout there are no major modifications to the board necessary to evaluate the other ICs.

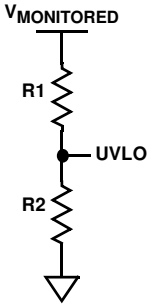
To the left, right and above the socket are four test point strips (TP1, TP2, TP3, TP4). These give access to the labeled IC I/O pins during evaluation. Remember that significant current or capacitive loading of particular I/O pins will affect functionality and performance.

Attention to orientation and placement of variant ICs in the socket must be paid to prevent IC damage or faulty evaluation.

The default configuration of the ISL612XSEQEVAL1Z circuitries was built around the following design assumptions:

1. Using the ISL6123IR or ISL6124IR
2. The four supplies being sequenced are 5V (IN_A), 3.3V (IN_B), 2.5V (IN_C) and 1.5V (IN_D), the UVLO levels are ~80% of nominal voltages. Resistors chosen such that the total resistance of each divider is ~10k using standard value resistors to approximate 80% of nominal = 0.63V on UVLO input.

   Resistor choice is such that I x R2 = 0.633V at the desired UV (undervoltage) level as the monitored voltage decreases. Total resistance in the divider is a factor for the designer to consider for accuracy of UV level and efficiency vs electrical noise immunity trade-offs.



   Vmon/0.633mV = R1+R2/R2 when Vmon = desired UV level as Vmon decreases.

   For example, a 5V supply with a desired UV level at 4V would mean R1+R2/R2 = 6.319. Ideally, any R1 and R2 combination that met this ratio would work, but with only standard value resistors available, small deviations will occur.

3. The desired order turn-on sequence is first both 5V and 3.3V supplies together and then the 2.5V supply about 75ms later and lastly, the 1.5V supply about 45ms later.
4. The desired turn-off sequence is first both 1.5V and 3.3V supplies at the same time then the 2.5V supply about 50ms later and lastly, the 5V supply about 72ms after that.

All scope shots are taken from ISL612XSEQEVAL1Z board. Figures 8 and 9 illustrate the desired turn-on and turn-off sequences respectively. The sequencing order and delay

between voltages sequencing is set by external capacitance values, so other than illustrated can be accomplished.

Figures 10 and 11 illustrate the timing relationships between the EN input, $\overline{\text{RESET}}$, DLY and GATE outputs and the VOUT voltage for a single channel being turned on and off respectively. $\overline{\text{RESET}}$ is not shown in Figure 10 as it asserts 160ms after the last GATE goes high.

All IC family variants share similar function for DLY_X capacitor charging, GATE and $\overline{\text{RESET}}$ operation. Figures 12 through 15 illustrate the principal feature and functional differences for each of the ISL6125, ISL6126, ISL6127 and ISL6128 variants.

Figure 12 features the ISL6125 open drain outputs being sequenced on and off along with $\overline{\text{RESET}}$ relationship, which is similar to all other family variants.

Figure 13 illustrates the independent input feature of the ISL6126 which allows once the $\overline{\text{EN}}$ is low for each UVLO to be individually satisfied and for its associated GATE to turn-on.

Only when the last variable VIN is satisfied as shown does the $\overline{\text{RESET}}$ release to signal all input voltages are valid.

Figure 14 shows the ISL6127 pre-programmed ABCD on DCBA off order of sequencing with minimal non-adjustable delay between each.

Figure 15 demonstrates the independence of the redundant two rail sequencer. It shows that either one of the two groups can be turned off and the ABCD order of restart with capacitor programmable delay once both EN inputs are pulled low.

Using the ISL6125EVAL1Z Platform

The ISL6125EVAL1Z is the ISL6125 specific evaluation board providing for easy evaluation of the ISL6125 with its unique open drain outputs. The UVLO levels, sequence and delays are programmed exactly like the other ISL612X ICs but the ISL6125 has sequenced open drain outputs rather than charge pumped driven GATE outputs. See Figure 17 for its schematic and photograph.

Typical Performance Waveforms

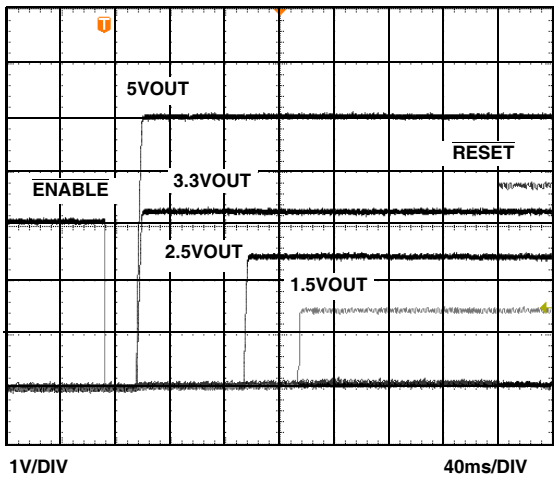


FIGURE 8. ISL6124 SEQUENCED TURN-ON

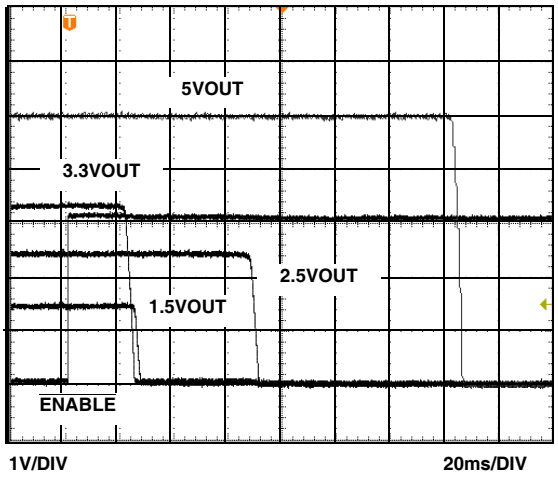


FIGURE 9. ISL6124 SEQUENCED TURN-OFF

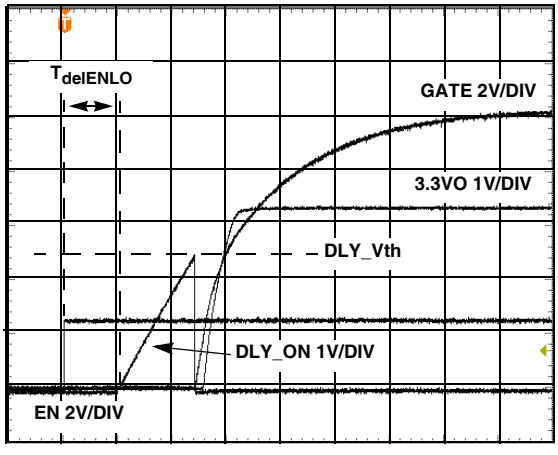


FIGURE 10. ISL6123 SINGLE CHANNEL TURN-ON

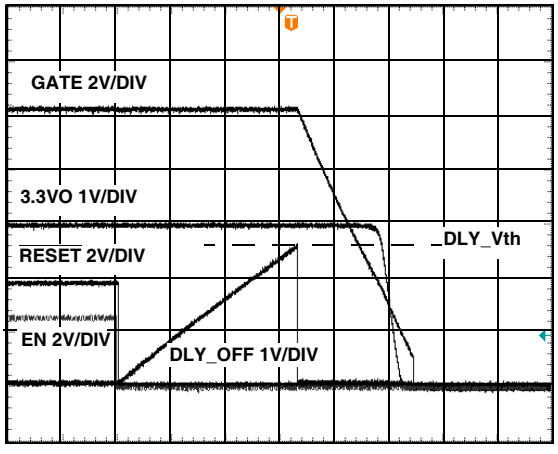


FIGURE 11. ISL6123 SINGLE CHANNEL TURN-OFF

Typical Performance Waveforms (Continued)

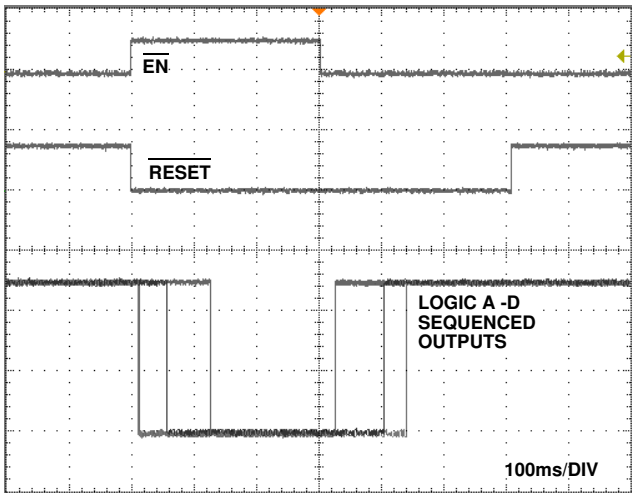


FIGURE 12. ISL6125 LOGIC OUTPUTS SEQUENCED ON AND OFF AND RESET RELATIONSHIP

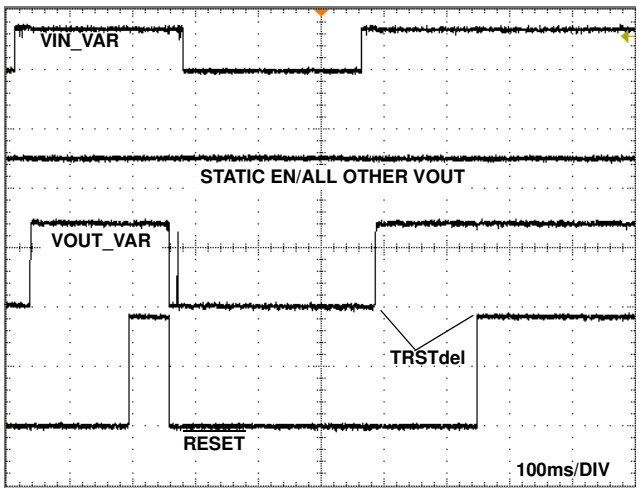


FIGURE 13. ISL6126 UVLO INPUT/OUTPUT INDEPENDENCE AND RESET RELATIONSHIP

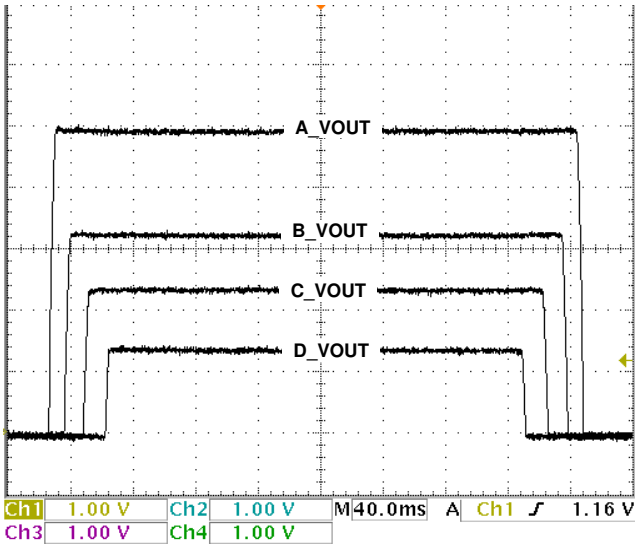


FIGURE 14. ISL6127 PREPROGRAMMED ABCD TURN-ON AND DCBA TURN-OFF

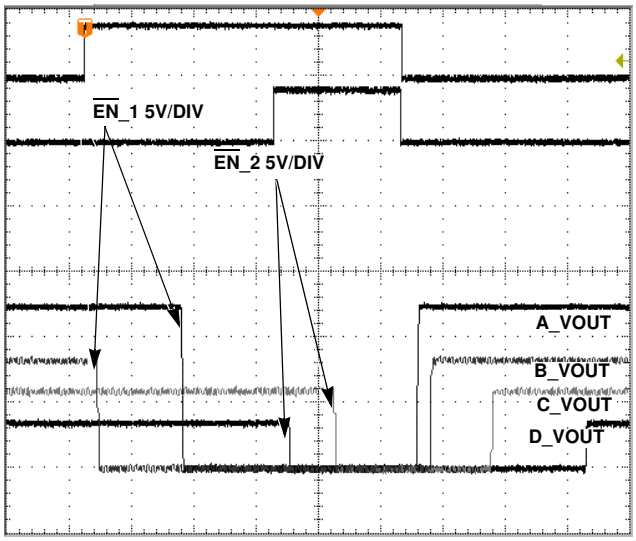
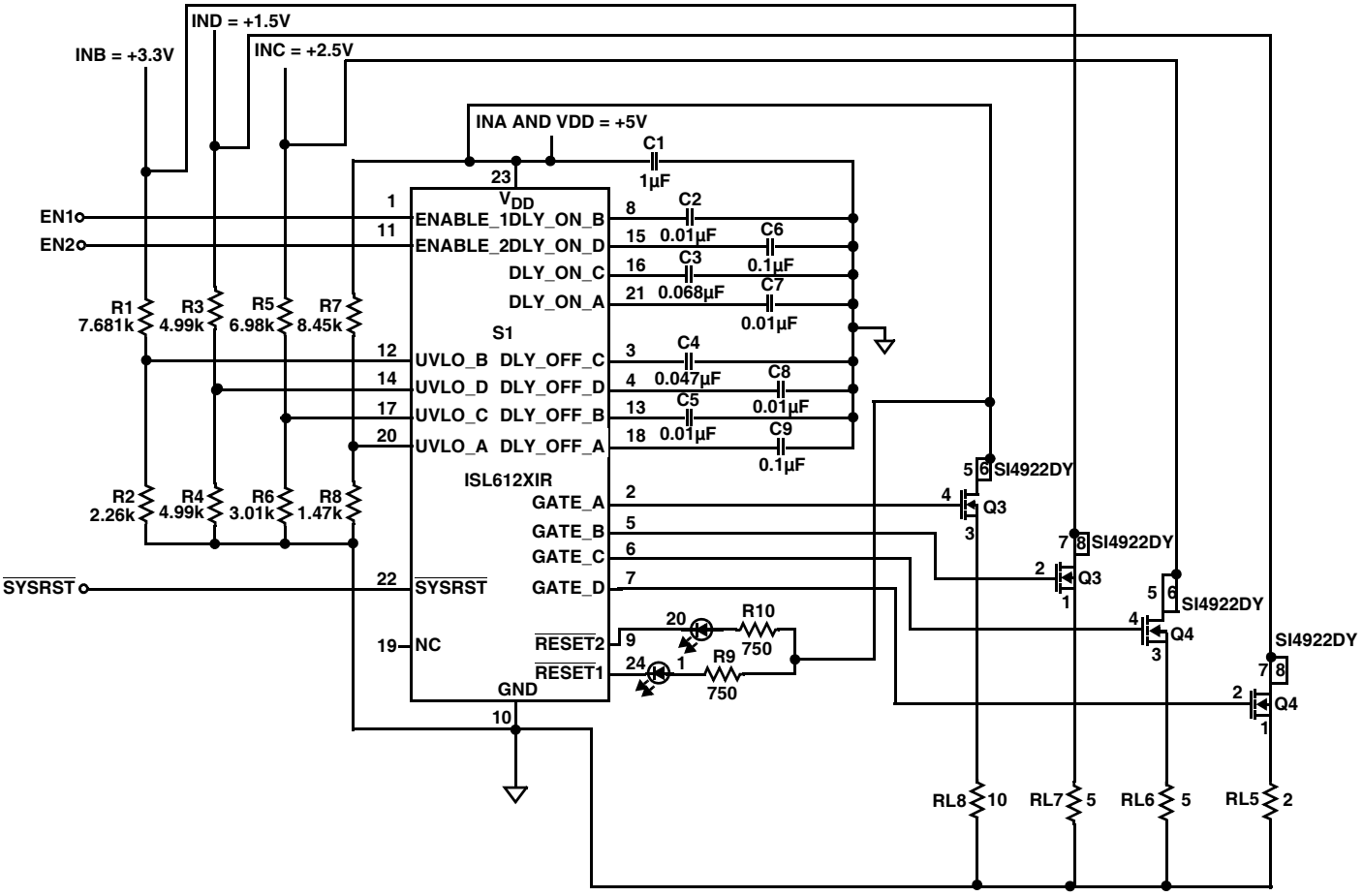


FIGURE 15. ISL6128 GROUP INDEPENDENT TURN-OFF AND DELAY ADJUSTABLE PRE PROGRAMMED TURN-ON



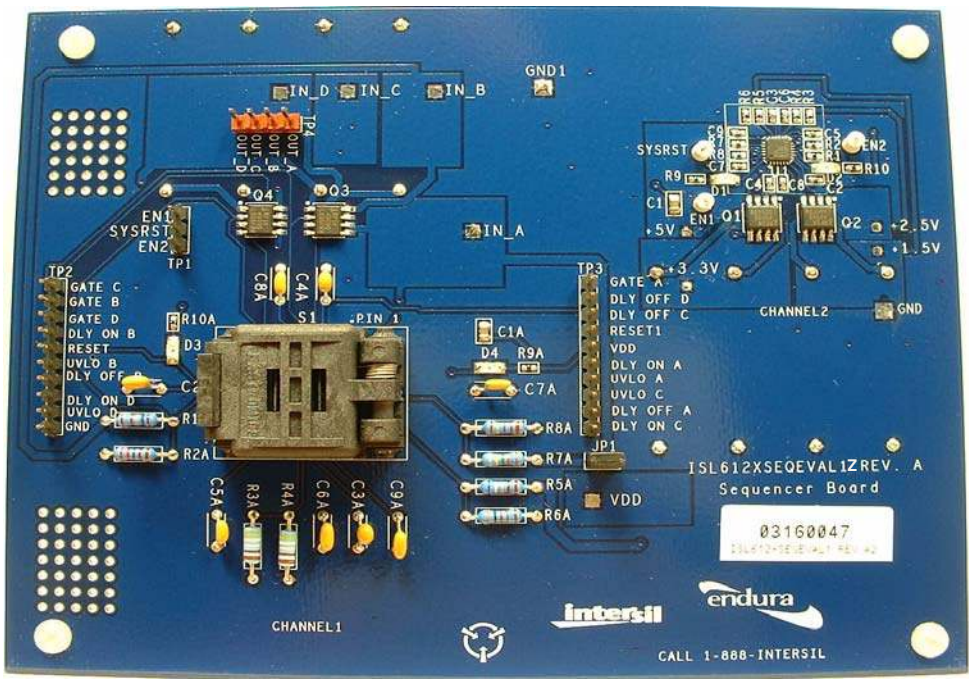
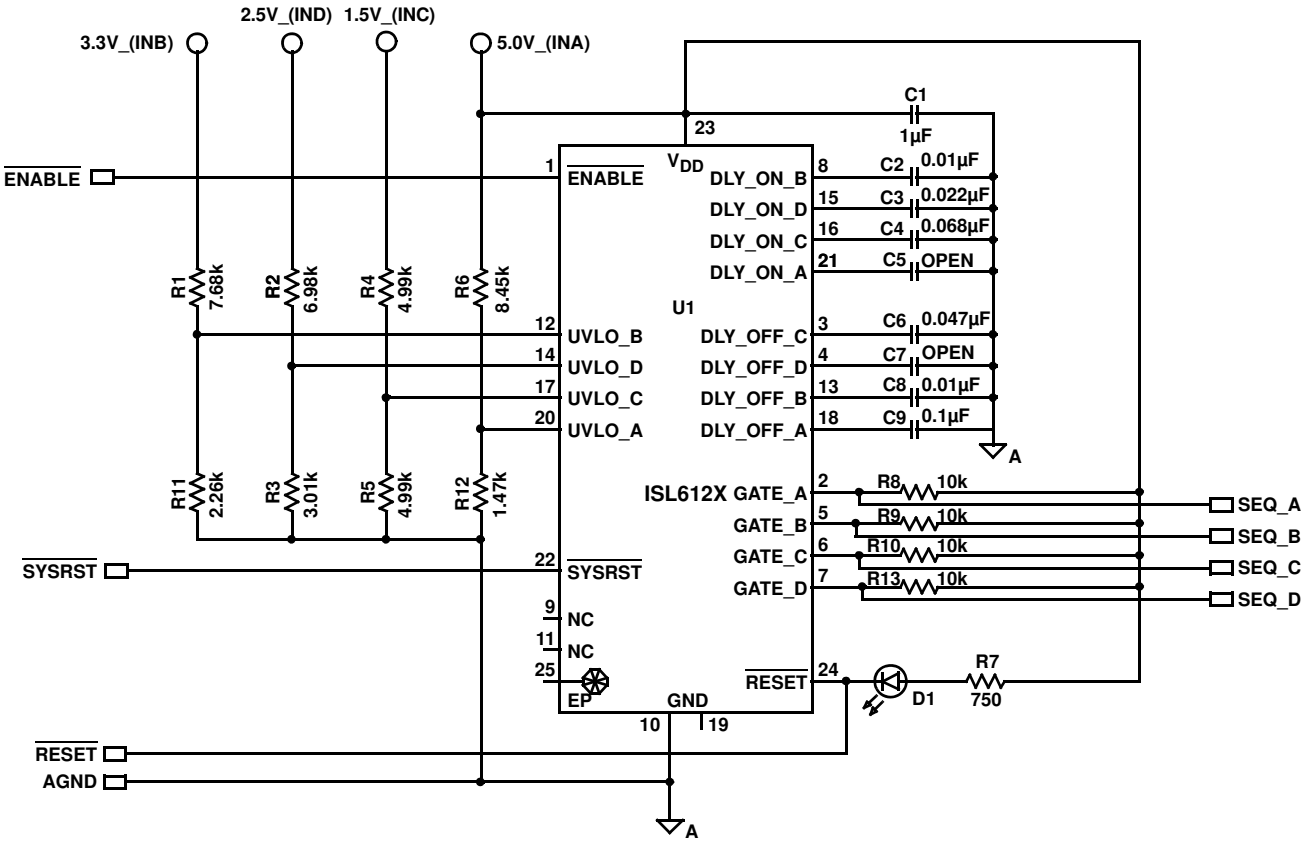


FIGURE 16. EVAL BOARD CHANNEL 1 SCHEMATIC AND ISL612XSEQEVAL1Z PHOTOGRAPH



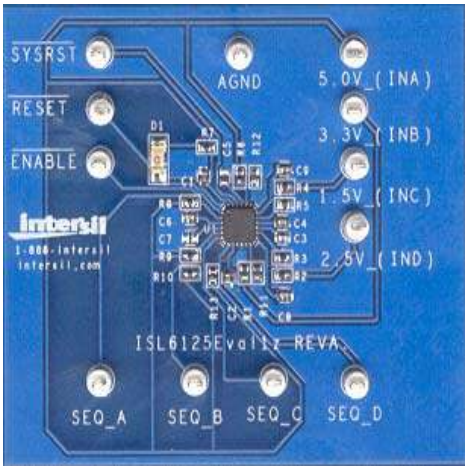


FIGURE 17. ISL6125EVAL1Z SCHEMATIC AND PHOTOGRAPH

TABLE 2. ISL612XSEQEVAL1Z BOARD CHANNEL 1 COMPONENT LISTING

COMPONENT DESIGNATOR	COMPONENT FUNCTION	COMPONENT DESCRIPTION
S1	ISL612X, 4 Supply Sequencer Socket	Intersil, ISL612X4 Supply Sequencer Socket
Q3, Q4	Voltage Rail Switches	SI4922DY or equivalent, Dual 8A, 30V, 0.018Ω, N-Channel MOSFET
R7	5V to UVLO_A Resistor for Divider String	8.45kΩ 1%, 0402
R8	UVLO_A to GND Resistor for Divider String	1.47kΩ 1%, 0402
R1	3.3V to UVLO_B Resistor for Divider String	7.68kΩ 1%, 0402
R2	UVLO_B to GND Resistor for Divider String	2.26kΩ 1%, 0402
R5	2.5V to UVLO_C Resistor for Divider String	6.98kΩ 1%, 0402
R6	UVLO_C to GND Resistor for Divider String	3.01kΩ 1%, 0402
R3	1.5V to UVLO_D Resistor for Divider String	4.99kΩ 1%, 0402
R4	UVLO_D to GND Resistor for Divider String	4.99kΩ 1%, 0402
R9	$\overline{\text{RESET}}$1 LED Current Limiting Resistor	750Ω 10%, 0805
R10	$\overline{\text{RESET}}$2 LED Current Limiting Resistor	750Ω 10%, 0805
C7	5V turn-on Delay Capacitor (13ms)	0.01µF 10%, 6.3V, 0402
C9	5V turn-off Delay Capacitor (130ms)	0.1µF 10%, 6.3V, 0402
C2	3.3V turn-on Delay Capacitor (13ms)	0.01µF 10%, 6.3V, 0402
C5	3.3V turn-off Delay Capacitor (3ms)	0.01µF 10%, 6.3V, 0402
C3	2.5V turn-on Delay Capacitor (88ms)	0.068µF 10%, 6.3V, 0402
C4	2.5V turn-off Delay Capacitor (61ms)	0.047µF 10%, 6.3V, 0402
C6	1.5V turn-on Delay Capacitor (130ms)	0.1µF 10%, 6.3V, 0402
C8	1.5V turn-off Delay Capacitor (13ms)	0.01µF 10%, 6.3V, 0402
C1	Decoupling Capacitor	0.1µF, 0805
D1	$\overline{\text{RESET}}$1 Indicating LED	0805, SMD LEDs Red
D2	$\overline{\text{RESET}}$2 Indicating LED	0805, SMD LEDs Red
RL8	5V Load Resistor	10Ω 20%, 3W Carbon
RL7	3.3V Load Resistor	5Ω 20%, 3W Carbon
RL6	2.5V Load Resistor	5Ω 20%, 3W Carbon
RL5	1.5V Load Resistor	2Ω 20%, 3W Carbon

TABLE 3. ISL6125EVAL1Z COMPONENT LISTING

COMPONENT DESIGNATOR	COMPONENT FUNCTION	COMPONENT DESCRIPTION
U1	ISL6125, Four Supply Sequencer	Intersil, ISL6125, Four Supply Sequencer with Open Drain Outputs
R6	5V to UVLO_A Resistor for Divider String	8.45kΩ 1%, 0402
R12	UVLO_A to GND Resistor for Divider String	1.47kΩ 1%, 0402
R1	3.3V to UVLO_B Resistor for Divider String	7.68kΩ 1%, 0402
R11	UVLO_B to GND Resistor for Divider String	2.26kΩ 1%, 0402
R2	2.5V to UVLO_D Resistor for Divider String	6.98kΩ 1%, 0402
R3	UVLO_D to GND Resistor for Divider String	3.01kΩ 1%, 0402
R4	1.5V to UVLO_C Resistor for Divider String	4.99kΩ 1%, 0402
R5	UVLO_D to GND Resistor for Divider String	4.99kΩ 1%, 0402
R9	RESET LED Current Limiting Resistor	750Ω 10%, 0805
C5	5V turn-on Delay Capacitor A	DNP, 0402
C9	5V turn-off Delay Capacitor A (135ms)	0.1µF 10%, 6.3V, 0402
C2	3.3V turn-on Delay Capacitor B (13.7ms)	0.01µF 10%, 6.3V, 0402
C8	3.3V turn-off Delay Capacitor B (13.7ms)	0.01µF 10%, 6.3V, 0402
C3	2.5V turn-on Delay Capacitor D (28ms)	0.022µF 10%, 6.3V, 0402
C7	2.5V turn-off Delay Capacitor D	DNP, 0402
C4	1.5V turn-on Delay Capacitor C (98ms)	0.068µF 10%, 6.3V, 0402
C6	1.5V turn-off Delay Capacitor C (59ms)	0.047µF 10%, 6.3V, 0402
C1	Decoupling Capacitor	0.1µF, 0805
D1	$\overline{\text{RESET}}$1 Indicating LED	0805, SMD LED
R8	SEQ_OUTPUT_A Pull-Up Resistor	10kΩ, 0402
R9	SEQ_OUTPUT_B Pull-Up Resistor	10kΩ, 0402
R10	SEQ_OUTPUT_C Pull-Up Resistor	10kΩ, 0402
R13	SEQ_OUTPUT_D Pull-Up Resistor	10kΩ, 0402

Application Implementations

Multiple Sequencer Implementations

In order to control the sequencing of more than 4 voltages, several of the ISL6123, ISL6124, ISL6125 or ISL6127 devices can be variously configured together to accomplish this. There may be concerns of a particular implementation that would make a particular configuration preferable over another. The fundamental questions to answer to determine which configuration is best suited for your applications are:

1. What level of voltage assurance is needed prior to sequencing on and can the voltage supplies be grouped into high and low criticality?
2. Is there a critical maximum time window all supplies must be present at load or is there a first and a second group preference possibly with some work done in between the two groups of voltages being present?

Three configurations are described and illustrated here.

In applications where the integrity of critical voltages must be assured prior to sequencing, additional monitoring of the critical supplies is needed. If the compliance of the voltage is critical for either undervoltage and/or overvoltage, voltage supervisors can be employed to provide this additional assurance across multiple sequencers. Figure 18 is a block diagram of this voltage compliant, high assurance, low risk configuration showing the ISL6131 or ISL6132 supervisor and a mix of FET switched outputs and logic output sequencers (ISL6124 and ISL6125 ICs).

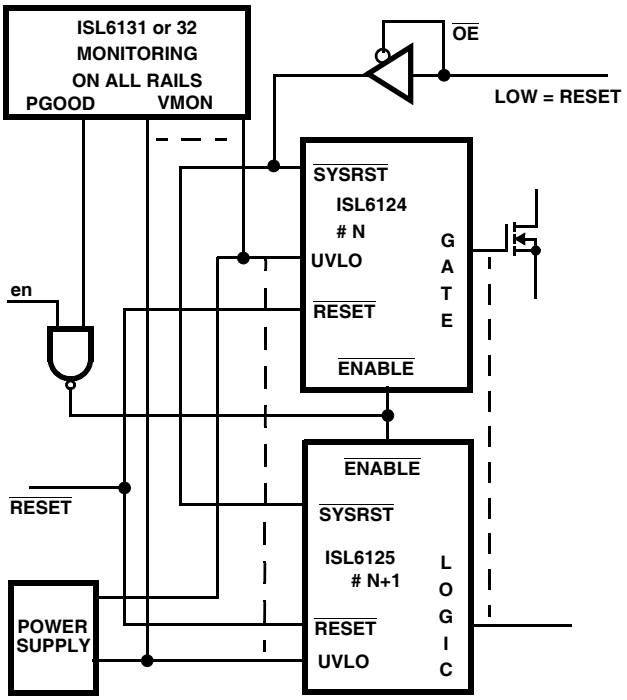


FIGURE 18. ISL612X AND ISL613X VOLTAGE COMPLIANT SEQUENCING BLOCK DIAGRAM

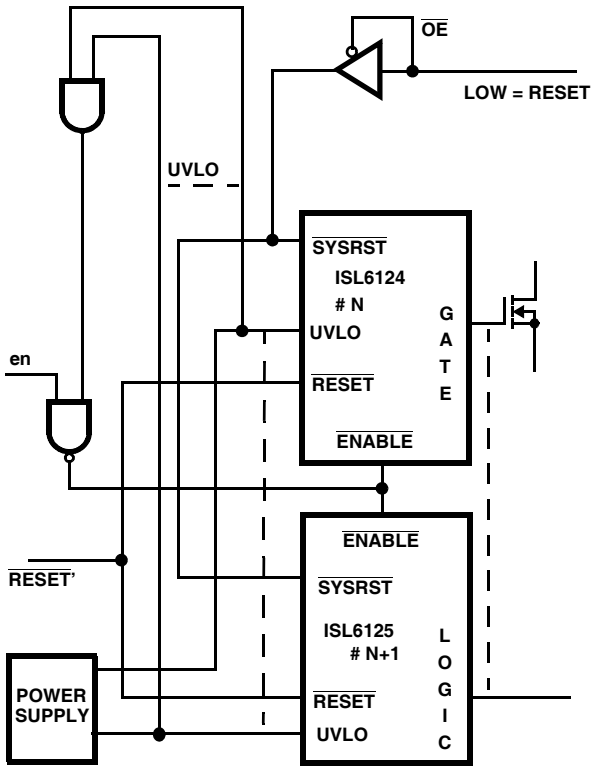


FIGURE 19. MULTIPLE ISL612X USING LOGIC GATES FOR VOLTAGE PRESENCE DETECT

If the mere presence of some voltage potential is adequate prior to sequencing on, then a small number of standard logic AND gates can be used to accomplish this. The block diagram in Figure 19 illustrates this voltage presence configuration.

In either case, the sequencing is straight forward across multiple sequencers as all DLY_ON capacitors will simultaneously start charging ~10ms after the common ENABLE input signal is delivered. This allows the choice of capacitors to be related to each other no different than using a single sequencer. When the common enabling signal is de-asserted these configurations will then execute the turn-off sequence across all sequencers as programmed by the DLY_OFF capacitor values.

In both cases, with all the $\overline{\text{SYSRST}}$ pins bussed together, once the on sequence is complete, simultaneous shutdown upon any UVLO input failure is assured as $\overline{\text{SYSRST}}$ output will momentarily pull low turning off all GATE and LOGIC outputs.

There may be applications that require or allow groups of supplies being brought up in sequence and supplies within each group to be sequenced. Figure 20 illustrates such a configuration that allows the first group of supplies to turn-on before the second group starts. This arrangement does not necessarily preclude adding the assurance of all supplies prior to turn-on sequencing as previously shown but it will prevent the turn-on sequence from completing if there is one unsatisfied UVLO input in a group. Using this configuration involves waiting through the $T_{UVLOdel}$ and $T_{\overline{RST}del}$ (total of ~160ms) for each sequencer IC in the chain for the final $\overline{\text{RESET}}$ to release. Once ENABLE on the first sequencer is de-asserted all the $\overline{\text{RESET}}$ outputs will quickly pull low and thus allow the sequenced turn-off of this configuration to ripple through several banks as quickly as the user programmed sequence (as chosen by the DLY_OFF) capacitors allow. Once again with common bussed $\overline{\text{SYSRTS}}$ pins, simultaneous shut down of all GATEs and LOGIC down upon an unsatisfied UVLO input is assured once all FETs or LOGIC output are on. If a GATE drive option IC is used to drive both FETs and logic signals, then care to ensure the charged pump GATE does not overdrive and damage the logic input must be taken. A simple resistor divider can be used to lower the GATE voltage to a suitable voltage for the logic input as shown in Figure 20.

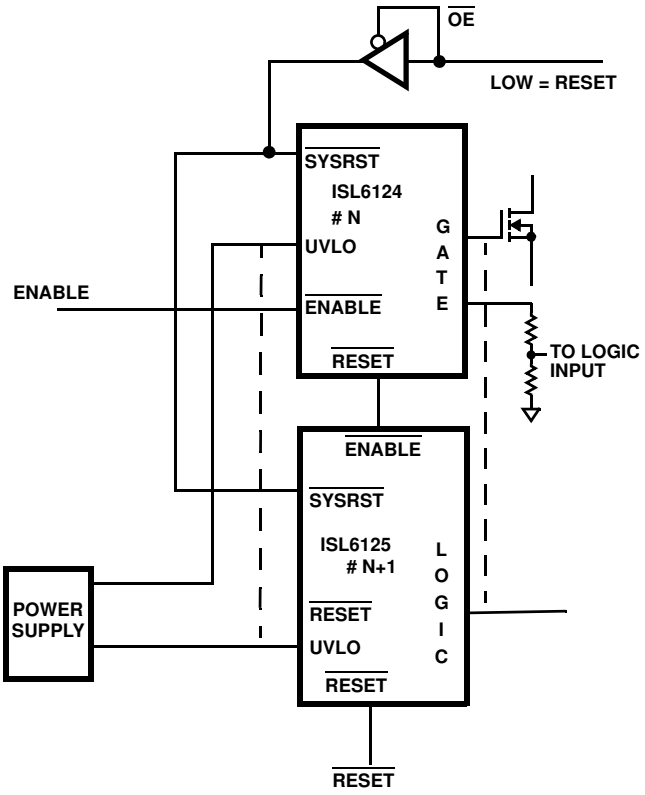


FIGURE 20. MULTIPLE ISL612X SERIAL CONFIGURATION

Voltage Tracking

In some applications the various voltages may have to track each other as they ramp up and down, whereas others may just need sequencing. In these cases, tracking can be accomplished and has been demonstrated over a wide range of load current (1A to 10A) and load capacitance (10µF to 3300µF) with the ISL612X family. Figure 21 and Figure 22 illustrate output voltage ramping tracking performance. Note that differences are less than 0.5V. With the relevant GATE pins tied together in a star pattern so that the resistance between any two GATE pins is equivalent (1k to 10k), which results in a sharing of the GATE ramping voltage and with the same or similar enough FETs this behavior is observed.

It is suggested that this circuit implementation be prototyped and evaluated for the particular expected loads prior to committing to manufacturing build.

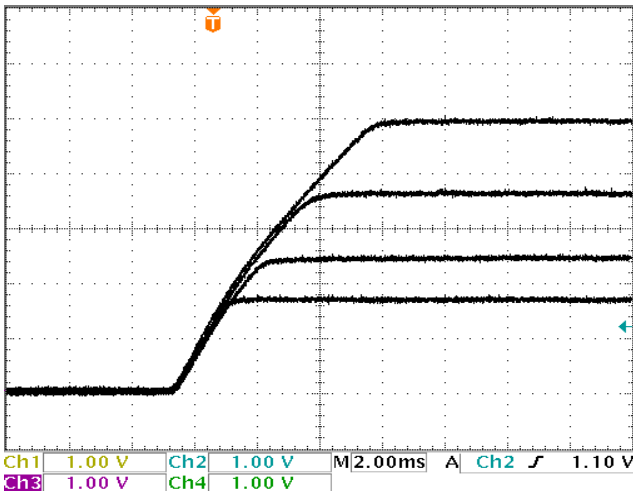


FIGURE 21. OUTPUT VOLTAGE ON LOW TO HIGH TRACKING

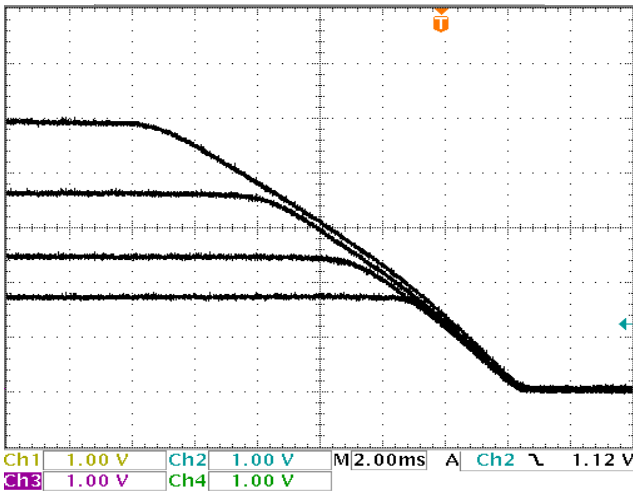


FIGURE 22. OUTPUT VOLTAGE HIGH TO LOW TRACKING

Negative Voltage Sequencing

The ISL612X family can use the charged pump GATE output to drive FETs that would control and sequence negative voltages down to a nominal -5V with minimal additional external circuitry. Figure 23 shows turn-on of 5V bipolar supplies together, then the +2.5V and turn-off of both positive supplies being turned off together after the -5V. Figure 24 shows the minimal additional external circuitry to accomplish this. The 5V zener diode is used to level shift the GATE drive down 5V to prevent premature turn-on when GATE = 0V. Once GATE drive voltage > Vz, then FET Vgs > 5V, ensuring full turn-on once GATE gets to VDD+5.3V. Turn-on and turn-off ramp rate can be adjusted with FET gate series resistor value. Sequencing of the -V rail is accomplished as normal via the DLY_X capacitor value although adjustments in prototyping should be factored in to fine tune for actual circuit requirements.

Figures 25 and 26 illustrate a high accuracy -V detection circuit using the ISL6131 and a low cost low accuracy -V detect circuit respectively.

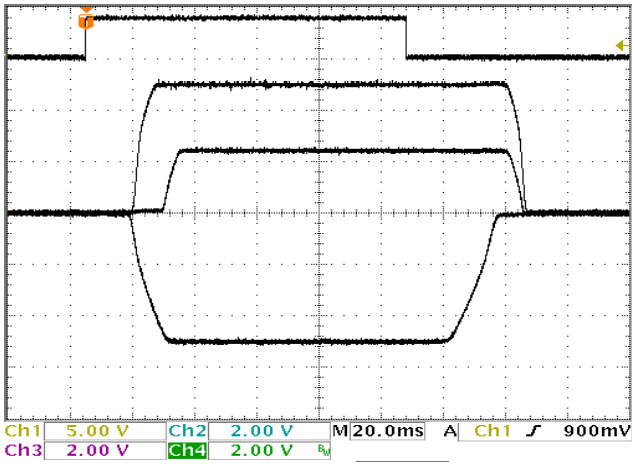
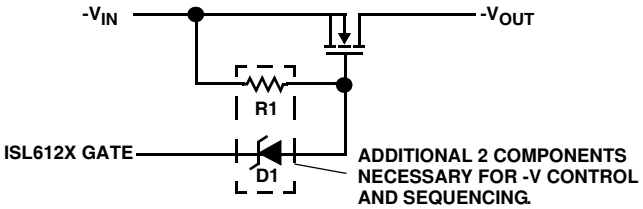
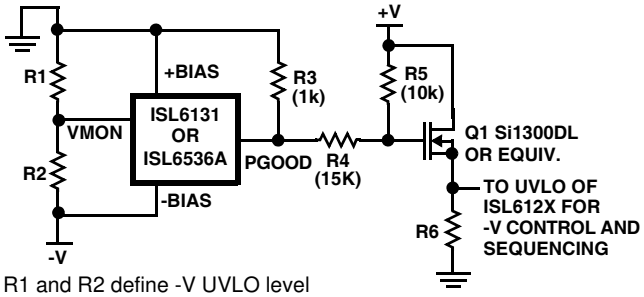


FIGURE 23. ±VOLTAGE SEQUENCING



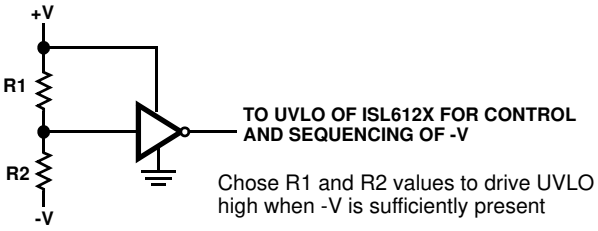
D1 necessary to prevent premature turn-on. R1 is used to hold FET Vgs = 0V until D1 Vz is overcome. R1 value can be changed to adjust -V ramp rates. Choose a R1 value between 4MΩ and 10MΩ initially and fine tune resistor value for the particular need.

FIGURE 24. -VOLTAGE FET DRIVE CIRCUIT



R1 and R2 define -V UVLO level
R3 ensures supervisor (ISL6131 or ISL6536A) PGOOD pull-up
R4 and R5 provide Q1 gate bias between 0V and +V
to 0V (resistor values suitable for -V = -5V and +V = +3.3V)

FIGURE 25. HGH ACCURACY -V LOCK OUT



Chose R1 and R2 values to drive UVLO high when -V is sufficiently present

FIGURE 26. LOW ACCURACY -V PRESENCE DETECTION

Application Considerations

Timing Error Sources

In any system there are variance contributors, for the ISL612X family the timing errors are mainly contributed by three sources.

Capacitor Timing Mismatch Error

Obviously, the absolute capacitor value is an error source, thus lower percentage tolerance capacitors help to reduce this error source. Figure 27 illustrates a difference of 0.57ms between two DLY_X outputs ramping to DLY_X threshold voltage, these 5% capacitors were from a common source. In applications where two or more GATEs or LOGIC outputs must have concurrent transitions, it is recommended that a common GATE drive be used to eliminate this timing error.

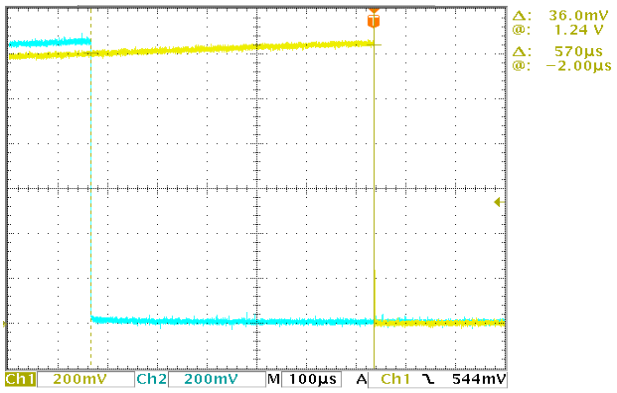


FIGURE 27. CAPACITOR TIMING MISMATCH

DLY_X Threshold Voltage and Charging Current Mismatch

The two other error sources come from the IC itself and are the differences in the DLY_X threshold voltage, (DLY_Vth) when the GATE charging latch is set and the DLY_X charging current, (DLY_ichg) across the four individual I/Os. Both of these parameters are bounded by specification and Figure 28 illustrates that with a common capacitor the typical error contributed by these factors is insignificant as both DLY_X traces overlay each other.

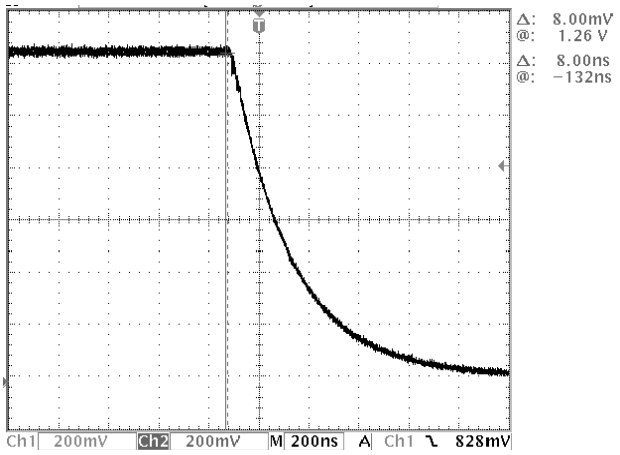
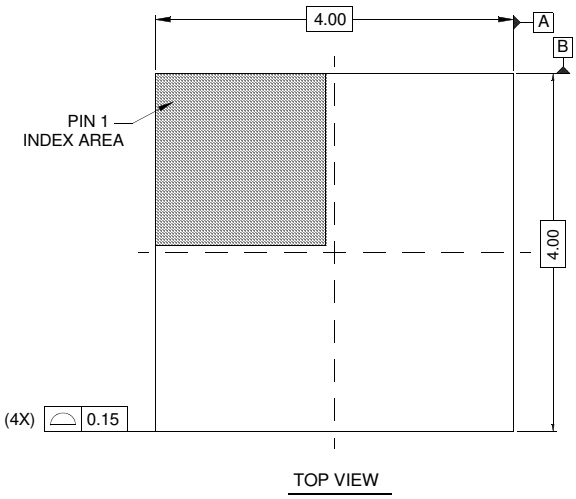


FIGURE 28. DLY_VTH AND DLY_ICHG TIMING MISMATCH

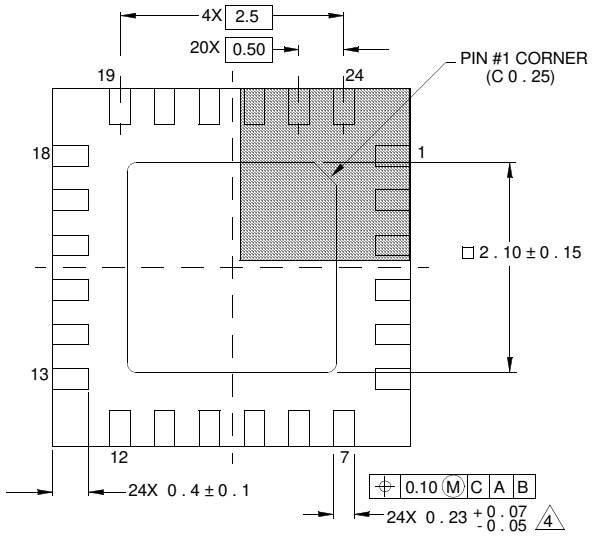
Package Outline Drawing

L24.4x4

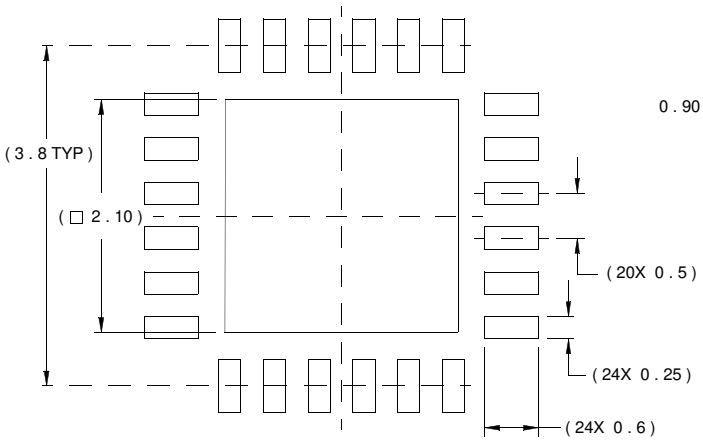
24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 4, 10/06



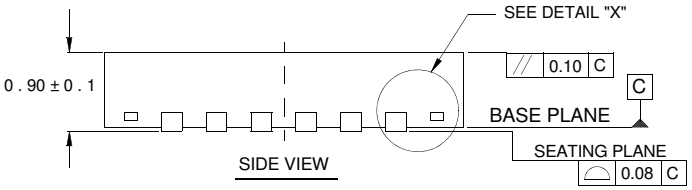
TOP VIEW



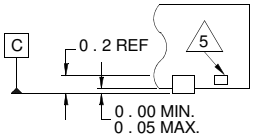
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.