

ISL28133

Single Micropower, Chopper Stabilized, RRIO Operational Amplifier

FN6560  
Rev.7.1  
Apr 22, 2021

The **ISL28133** is a single micropower, chopper stabilized operational amplifier that is optimized for single supply operation from 1.8V to 5.5V. Its low supply current of 18µA and wide input range enable make it an excellent general purpose op amp for a range of applications. The ISL28133 is ideal for handheld devices that operate off 2 AA or single Li-ion batteries.

The ISL28133 is available in the 5 Ld SOT-23 and 5 Ld SC70 packages. All devices operate over the extended temperature range of -40°C to +125°C.

**Features**

- Low input offset voltage ..... 8µV, Max.
- Low offset TC ..... 0.075µV/°C, Max
- Input bias current ..... 300pA, Max.
- Quiescent current ..... 18µA, Typ.
- Wide supply range ..... 1.8V to 5.5V
- Low noise (0.01Hz to 10Hz) ..... 1.1µV<sub>p-p</sub>, Typ.
- Rail-to-rail inputs and output
- Operating temperature range.....-40°C to +125°C

**Applications**

- Bidirectional current sense
- Temperature measurement
- Medical equipment
- Electronic weigh scales

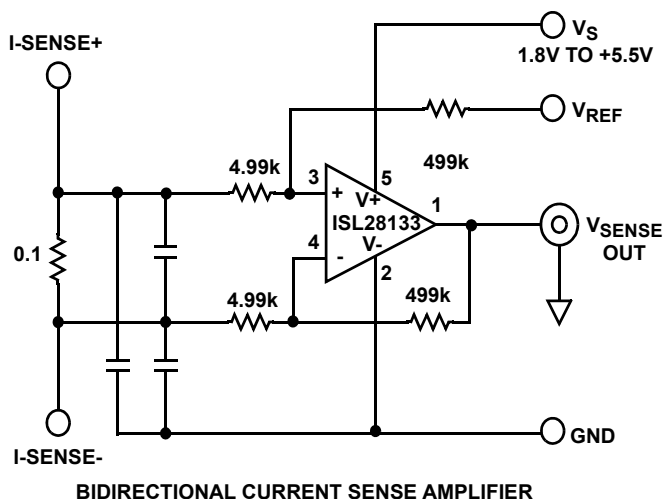


FIGURE 1. TYPICAL APPLICATION CIRCUIT

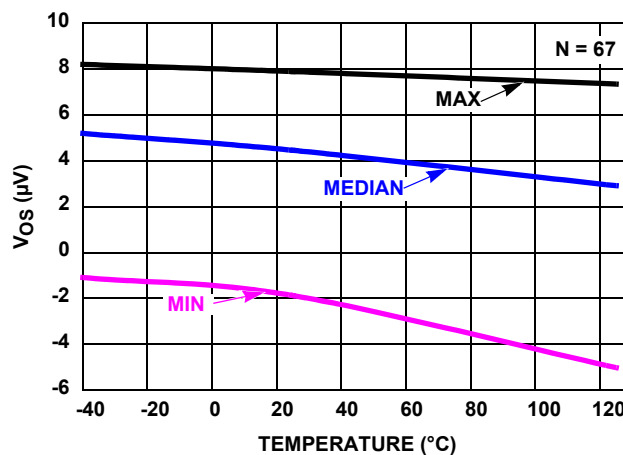
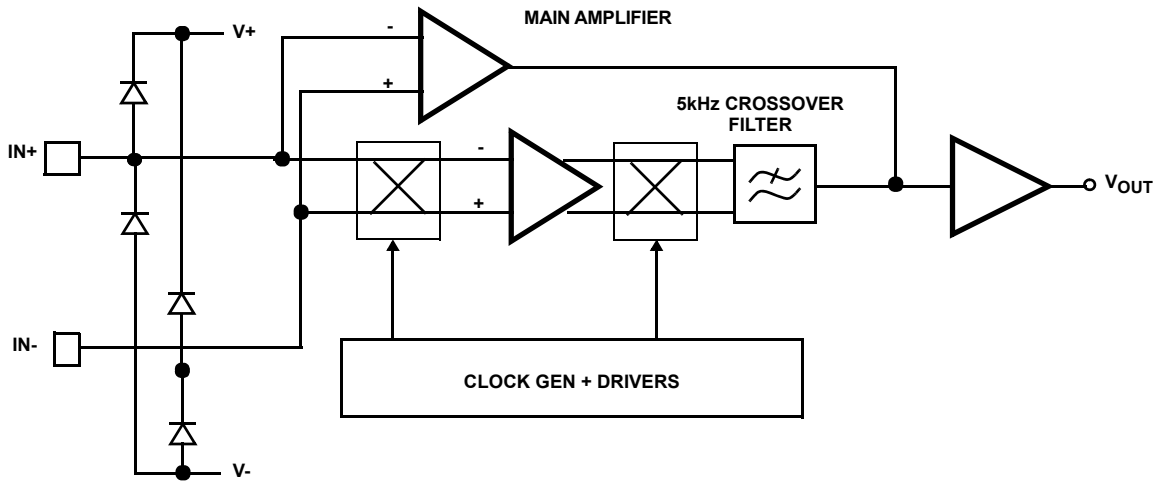


FIGURE 2. VOS vs TEMPERATURE

## Block Diagram



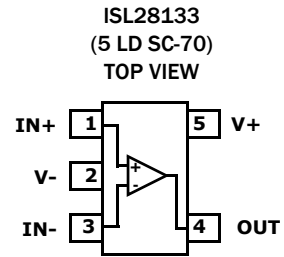
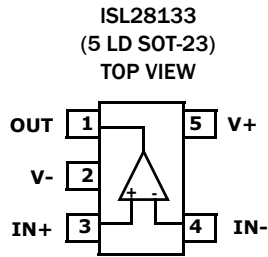
## Ordering Information

PART NUMBER	PART MARKING	PACKAGE DESCRIPTION (RoHS Compliant)	PKG. DWG. #	CARRIER TYPE (Note 1)
ISL28133FHZ-T7 (Note 2)	BCFA (Note 5)	5 Ld SOT-23	P5.064A	Reel, 3k
ISL28133FHZ-T7A (Note 2)				Reel, 250
ISL28133FEZ-T7 (Note 2)	BHA (Note 5)	5 Ld SC70	P5.049	Reel, 3k
ISL28133ISENSEV1Z	Evaluation Board			
ISL28133EVAL1Z	Evaluation Board			
ISL28133CSENSEV1Z	Evaluation Board			

### NOTES:

- See [TB347](#) for details on reel specifications.
- These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
- These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
- For Moisture Sensitivity Level (MSL), please see the device information page for the [ISL28133](#). For more information on MSL please see techbrief [TB363](#).
- The part marking is located on the bottom of the part.

## Pin Configurations



TOP VIEW

## Pin Descriptions

ISL28133 (5 Ld SOT23)	ISL28133 (5 Ld SC-70)	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
3	1	IN+	Non-inverting input	<p>Circuit 1</p>
2	2	V-	Negative supply	
4	3	IN-	Inverting input	(See Circuit 1)
1	4	OUT	Output	<p>Circuit 2</p>
5	5	V+	Positive supply	

## Absolute Maximum Ratings

Max Supply Voltage $V_+$ to $V_-$ .....	6.5V
Max Voltage $V_{IN}$ to GND .....	-0.5V to 6.5V
Max Input Differential Voltage .....	6.5V
Max Input Current .....	20mA
Max Voltage $V_{OUT}$ to GND (10s) .....	6.5V
ESD Rating	
Human Body Model .....	3000V
Machine Model .....	200V
Charged Device Model .....	1500V

## Thermal Information

Thermal Resistance (Typical)	$\theta_{JA}$ ( $^{\circ}\text{C}/\text{W}$ )	$\theta_{JC}$ ( $^{\circ}\text{C}/\text{W}$ )
5 Ld SOT-23 (Note 6, 7) .....	225	110
5 Ld SC-70 (Note 6) .....	206	N/A
Maximum Storage Temperature Range .....	-65 $^{\circ}\text{C}$ to +150 $^{\circ}\text{C}$	
Pb-Free Reflow Profile .....	see <a href="#">TB493</a>	

## Operating Conditions

Temperature Range .....	-40 $^{\circ}\text{C}$ to +125 $^{\circ}\text{C}$
Maximum Junction Temperature .....	140 $^{\circ}\text{C}$

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

### NOTES:

- $\theta_{JA}$  is measured with the component mounted on a high effective thermal conductivity test board in free air. See [TB379](#) for details.
- For  $\theta_{JC}$ , the "case temp" location is taken at the package top center.

**Electrical Specifications**  $V_+ = 5\text{V}$ ,  $V_- = 0\text{V}$ ,  $V_{CM} = 2.5\text{V}$ ,  $T_A = +25^{\circ}\text{C}$ ,  $R_L = \text{Open}$ , unless otherwise specified. **Boldface limits apply over the operating temperature range, -40 $^{\circ}\text{C}$  to +125 $^{\circ}\text{C}$ .**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
<b>DC SPECIFICATIONS</b>						
$V_{OS}$	Input Offset Voltage		-8	$\pm 2$	8	$\mu\text{V}$
			<b>-15.5</b>		<b>15.5</b>	$\mu\text{V}$
$TCV_{OS}$	Input Offset Voltage Temperature Coefficient			0.02	<b>0.075</b>	$\mu\text{V}/^{\circ}\text{C}$
$I_{OS}$	Input Offset Current			-60		pA
$I_B$	Input Bias Current		-300	$\pm 30$	300	pA
			<b>-600</b>		<b>600</b>	pA
Common Mode Input Voltage Range		$V_+ = 5.0\text{V}$ , $V_- = \text{GND}$	-0.1		5.1	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = -0.1\text{V}$ to 5.0V	118	125		dB
			<b>115</b>			dB
PSRR	Power Supply Rejection Ratio	$V_S = 2\text{V}$ to 5.5V	110	138		dB
			<b>110</b>			dB
$V_{OH}$	Output Voltage Swing, High	$R_L = 10\text{k}\Omega$	<b>4.965</b>	4.981		V
$V_{OL}$	Output Voltage Swing, Low	$R_L = 10\text{k}\Omega$		18	<b>35</b>	mV
$A_{OL}$	Open Loop Gain	$R_L = 1\text{M}\Omega$		174		dB
$V_+$	Supply Voltage	(Note 9)	1.8		5.5	V
$I_S$	Supply Current	$R_L = \text{OPEN}$		18	25	$\mu\text{A}$
					<b>35</b>	$\mu\text{A}$
$I_{SC+}$	Output Source Short Circuit Current	$R_L = \text{Short to ground or } V_+$	13	17	26	mA
$I_{SC-}$	Output Sink Short Circuit Current		-26	-19	-13	mA
<b>AC SPECIFICATIONS</b>						
GBWP	Gain Bandwidth Product $f = 50\text{kHz}$	$A_V = 100$ , $R_F = 100\text{k}\Omega$ , $R_G = 1\text{k}\Omega$ , $R_L = 10\text{k}\Omega$ to $V_{CM}$		400		kHz
$e_{N\text{ V}_{P-P}}$	Peak-to-Peak Input Noise Voltage	$f = 0.01\text{Hz}$ to 10Hz		1.1		$\mu\text{V}_{P-P}$
$e_N$	Input Noise Voltage Density	$f = 1\text{kHz}$		65		$\text{nV}/\sqrt{\text{Hz}}$

**Electrical Specifications**  $V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, T_A = +25^\circ C, R_L = \text{Open}$ , unless otherwise specified. **Boldface limits apply over the operating temperature range,  $-40^\circ C$  to  $+125^\circ C$ . (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
$i_N$	Input Noise Current Density	$f = 1\text{kHz}$		72		$fA/\sqrt{\text{Hz}}$
		$f = 10\text{Hz}$		79		$fA/\sqrt{\text{Hz}}$
$C_{in}$	Differential Input Capacitance	$f = 1\text{MHz}$		1.6		pF
	Common Mode Input Capacitance			1.12		pF
<b>TRANSIENT RESPONSE</b>						
SR	Positive Slew Rate	$V_{OUT} = 1V \text{ to } 4V, R_L = 10k\Omega$		0.2		$V/\mu s$
	Negative Slew Rate			0.1		$V/\mu s$
$t_r, t_f$ , Small Signal	Rise Time, $t_r$ 10% to 90%	$A_V = +1, V_{OUT} = 0.1V_{P-P}, R_F = 0\Omega, R_L = 10k\Omega, C_L = 1.2pF$		1.1		$\mu s$
	Fall Time, $t_f$ 10% to 90%			1.1		$\mu s$
$t_r, t_f$ Large Signal	Rise Time, $t_r$ 10% to 90%	$A_V = +1, V_{OUT} = 2V_{P-P}, R_F = 0\Omega, R_L = 10k\Omega, C_L = 1.2pF$		8		$\mu s$
	Fall Time, $t_f$ 10% to 90%			10		$\mu s$
$t_s$	Settling Time to 0.1%, $2V_{P-P}$ Step	$A_V = +1, R_F = 0\Omega, R_L = 10k\Omega, C_L = 1.2pF$		35		$\mu s$

NOTES:

- 8. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
- 9. Parts are 100% tested with a minimum operating voltage of 1.8V to a VOS limit of  $\pm 15\mu V$ .

**Typical Performance Curves**  $V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = \text{Open}$ .

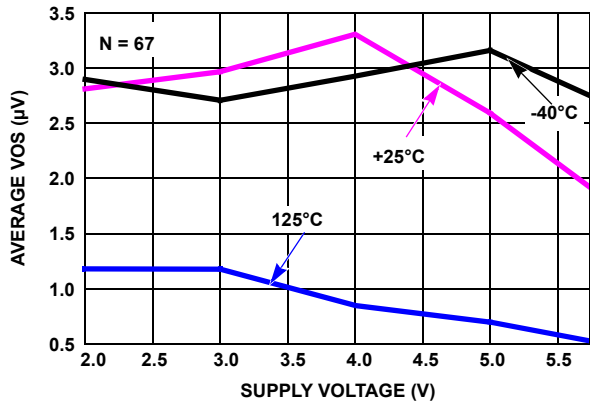


FIGURE 3. AVERAGE INPUT OFFSET VOLTAGE vs SUPPLY VOLTAGE

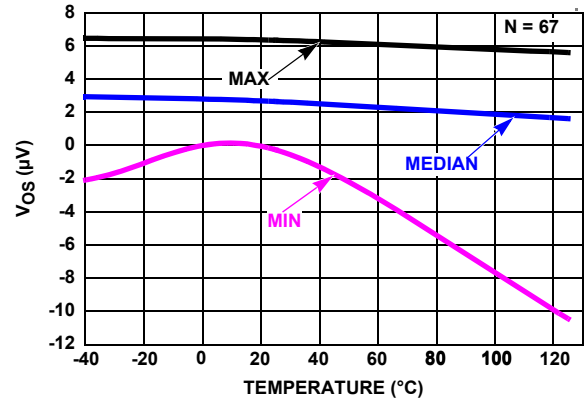


FIGURE 4.  $V_{OS}$  vs TEMPERATURE,  $V_S = \pm 1.0V, V_{IN} = 0V, R_L = \text{INF}$

**Typical Performance Curves**  $V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = \text{Open. (Continued)}$

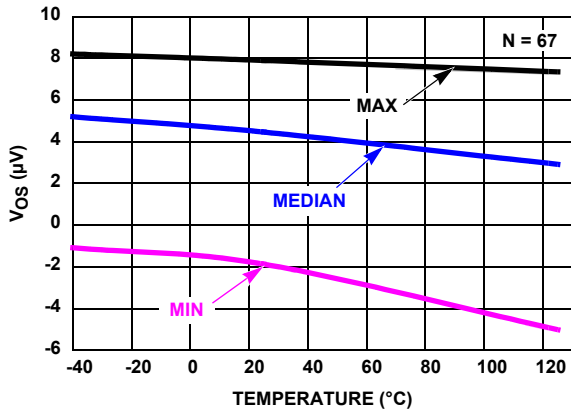


FIGURE 5.  $V_{OS}$  vs TEMPERATURE,  $V_S = \pm 2.5V, V_{IN} = 0V, R_L = \text{INF}$

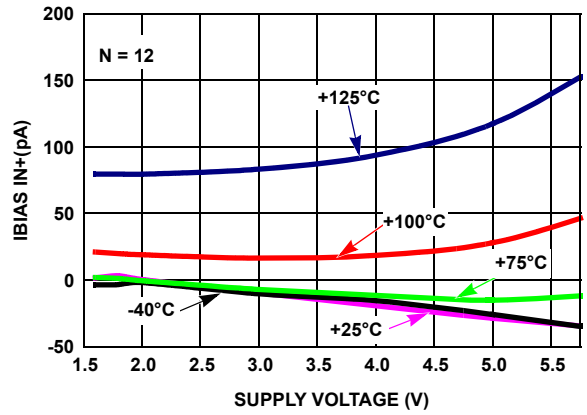


FIGURE 6.  $I_{B+}$  vs SUPPLY VOLTAGE vs TEMPERATURE

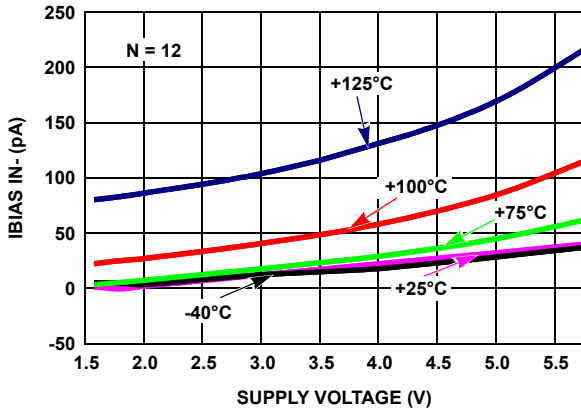


FIGURE 7.  $I_{B-}$  vs SUPPLY VOLTAGE vs TEMPERATURE

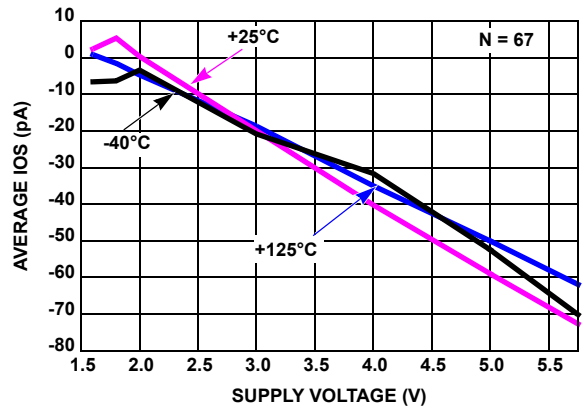


FIGURE 8.  $I_{OS}$  vs SUPPLY VOLTAGE vs TEMPERATURE

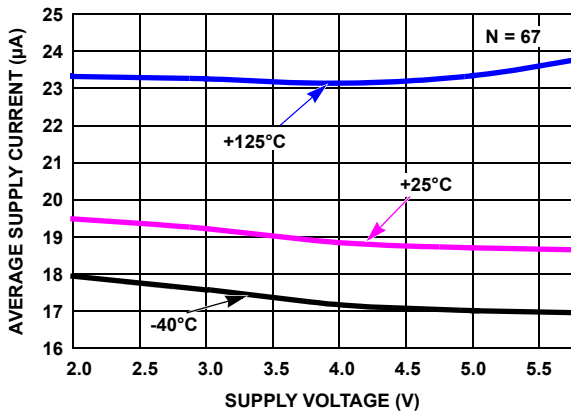


FIGURE 9. AVERAGE SUPPLY CURRENT vs SUPPLY VOLTAGE

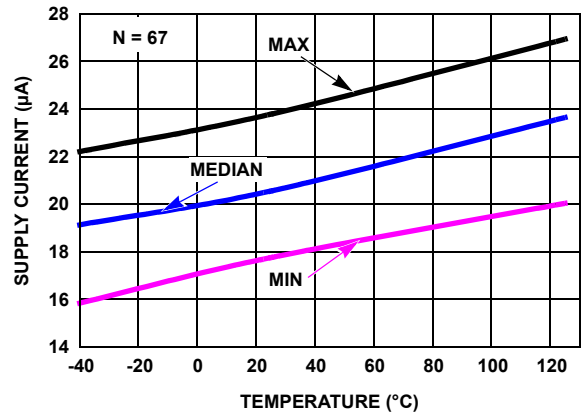
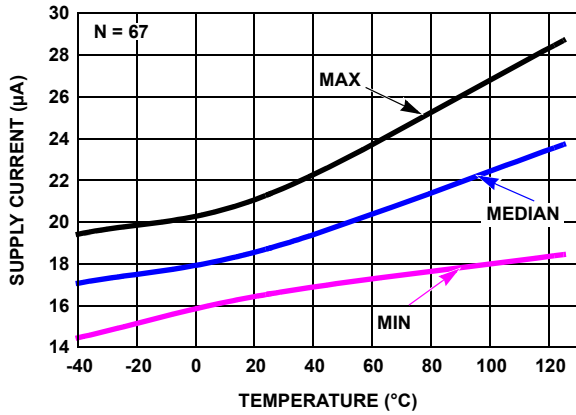
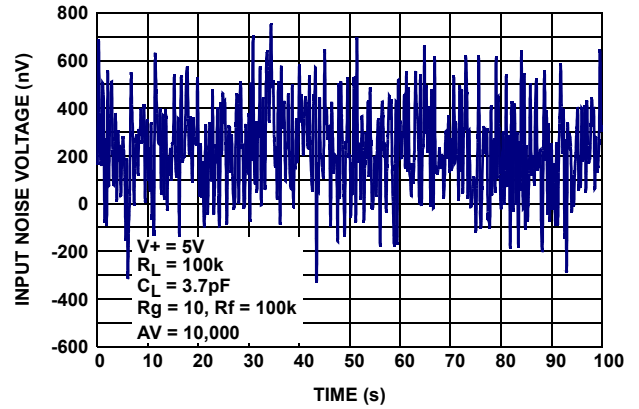


FIGURE 10. MIN/MAX SUPPLY CURRENT vs TEMPERATURE,  $V_S = \pm 0.8V, V_{IN} = 0V, R_L = \text{INF}$

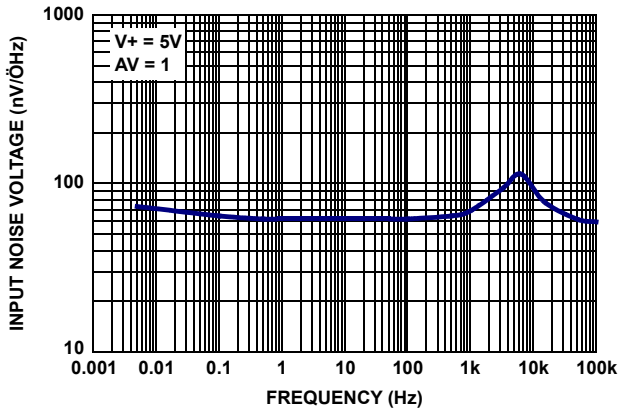
**Typical Performance Curves**  $V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = \text{Open. (Continued)}$



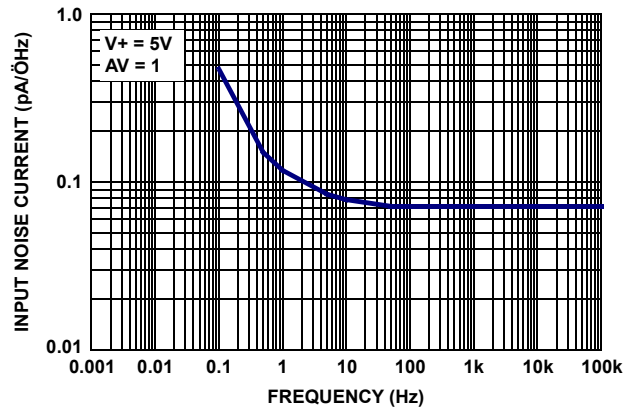
**FIGURE 11. MIN/MAX SUPPLY CURRENT vs TEMPERATURE,**  
 $V_S = \pm 2.5V, V_{IN} = 0V, R_L = \text{INF}$



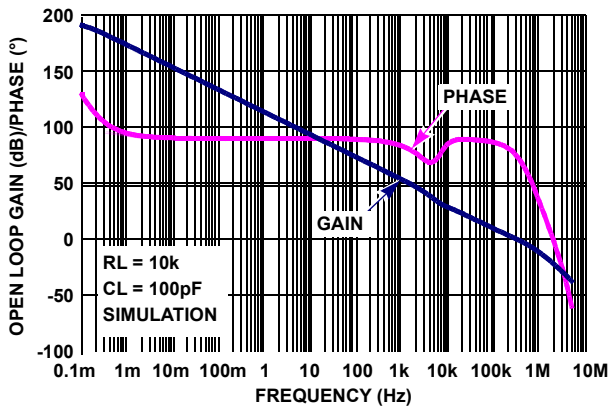
**FIGURE 12. INPUT NOISE VOLTAGE 0.01Hz TO 10Hz**



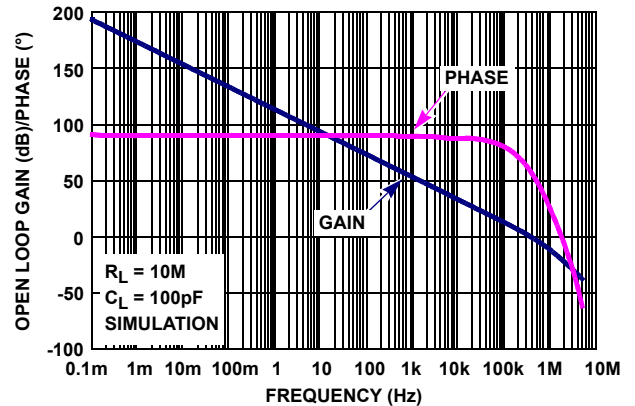
**FIGURE 13. INPUT NOISE VOLTAGE DENSITY vs FREQUENCY**



**FIGURE 14. INPUT NOISE CURRENT DENSITY vs FREQUENCY**



**FIGURE 15. FREQUENCY RESPONSE vs OPEN LOOP GAIN,  $R_L = 10k$**



**FIGURE 16. FREQUENCY RESPONSE vs OPEN LOOP GAIN,  $R_L = 10M$**

**Typical Performance Curves**  $V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = \text{Open}$ . (Continued)

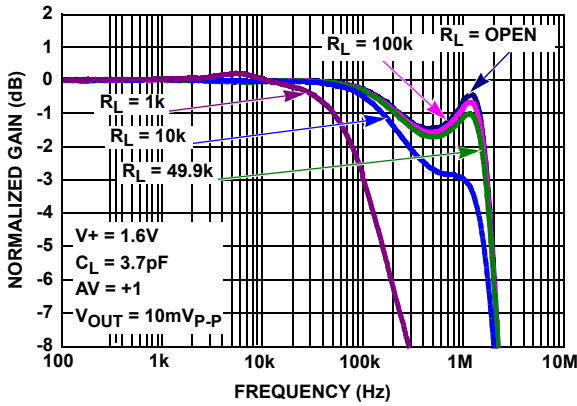


FIGURE 17. GAIN vs FREQUENCY vs  $R_L, V_S = 1.6V$

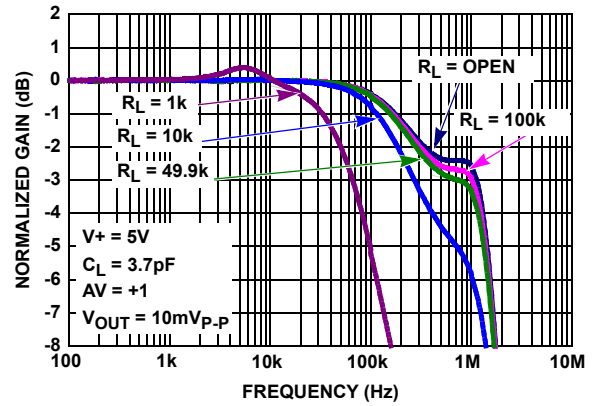


FIGURE 18. GAIN vs FREQUENCY vs  $R_L, V_S = 5V$

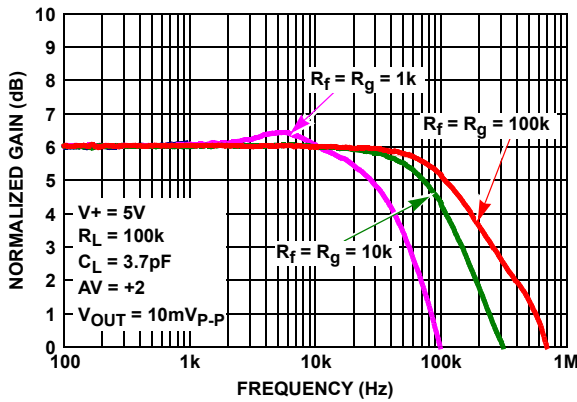


FIGURE 19. GAIN vs FREQUENCY vs FEEDBACK RESISTOR VALUES  $R_f/R_g$

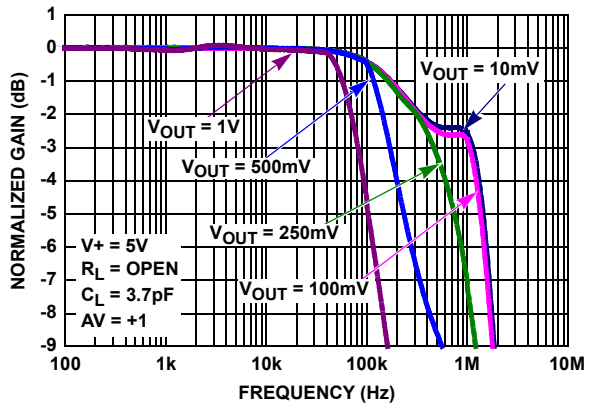


FIGURE 20. GAIN vs FREQUENCY vs  $V_{OUT}, R_L = \text{OPEN}$

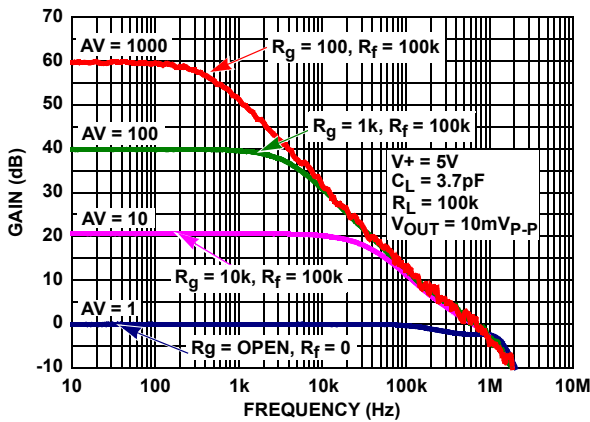


FIGURE 21. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

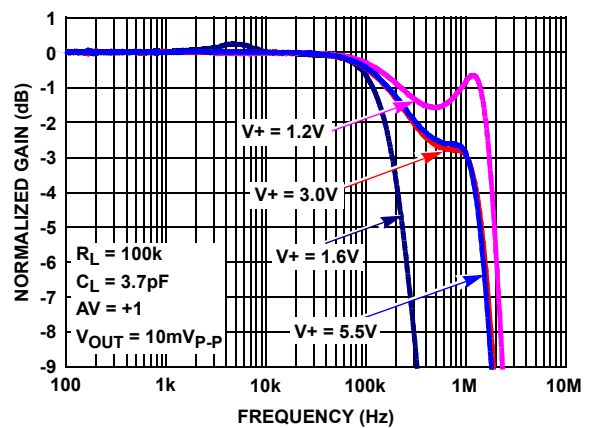


FIGURE 22. GAIN vs FREQUENCY vs SUPPLY VOLTAGE



**Typical Performance Curves**  $V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = \text{Open. (Continued)}$

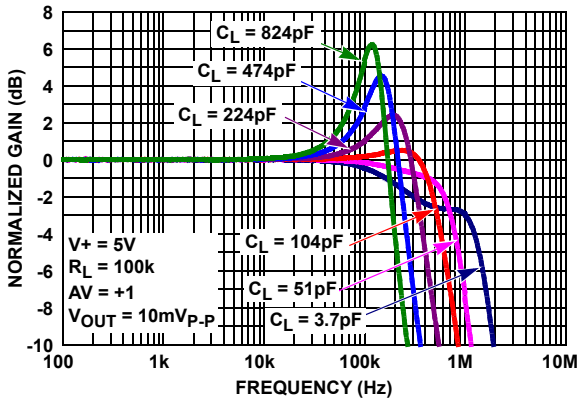


FIGURE 23. GAIN vs FREQUENCY vs  $C_L$

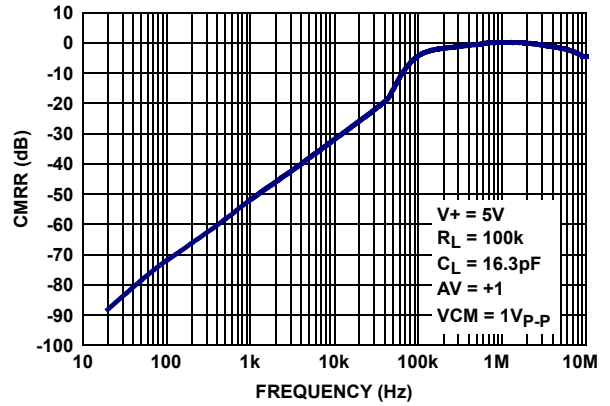


FIGURE 24. CMRR vs FREQUENCY,  $V_S = 5V$

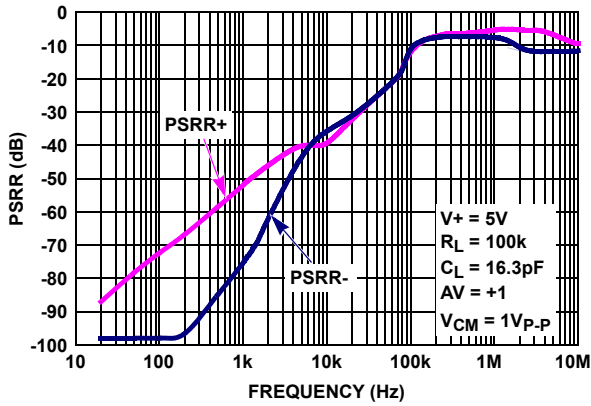


FIGURE 25. PSRR vs FREQUENCY,  $V_S = 5V$

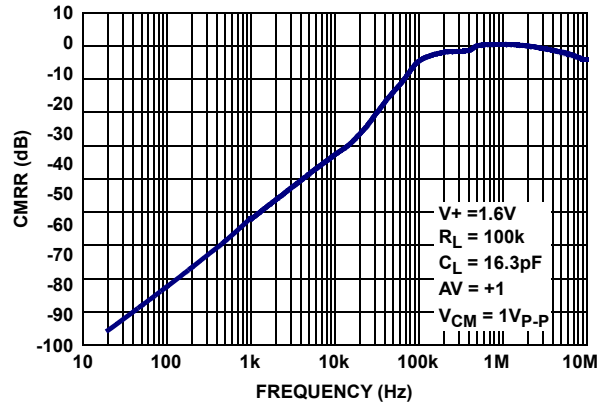


FIGURE 26. CMRR vs FREQUENCY,  $V_S = 1.6V$

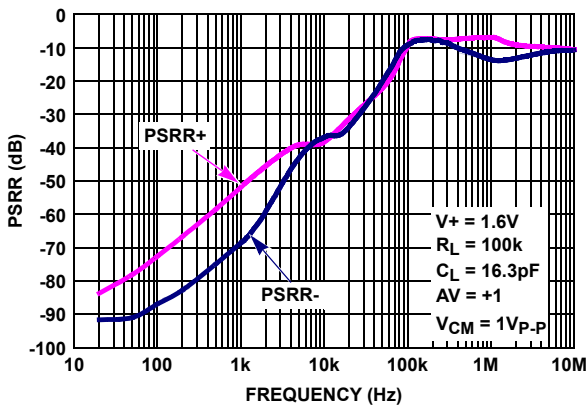


FIGURE 27. PSRR vs FREQUENCY,  $V_S = 1.6V$

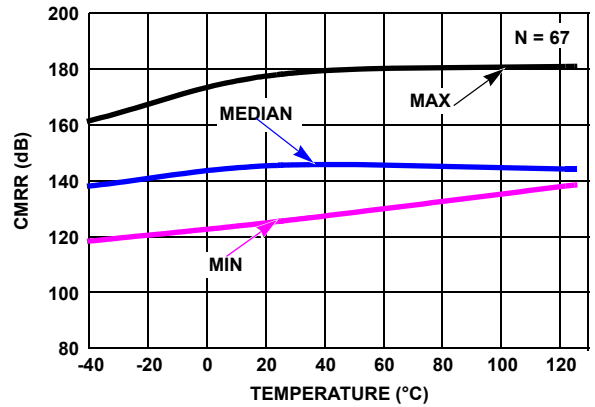


FIGURE 28. CMRR vs TEMPERATURE,  $V_{CM} = -2.5V \text{ TO } +2.5V, V_+ = \pm 2.5V$

**Typical Performance Curves**  $V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = \text{Open}$ . (Continued)

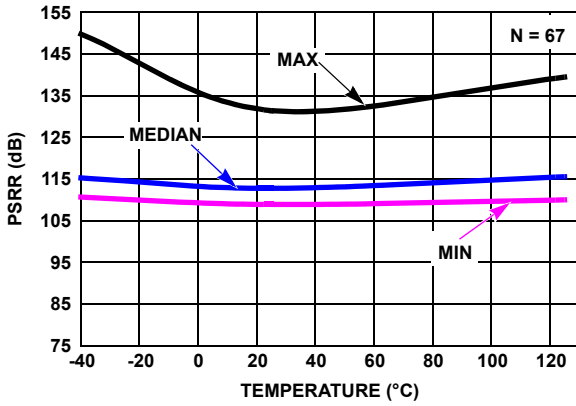


FIGURE 29. PSRR vs TEMPERATURE,  $V_+ = 2V$  TO  $5.5V$

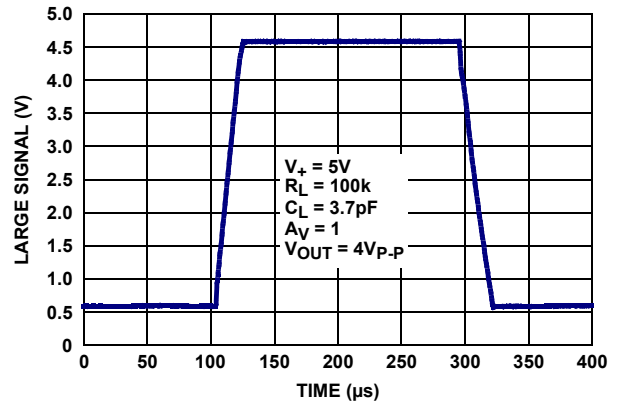


FIGURE 30. LARGE SIGNAL STEP RESPONSE (4V)

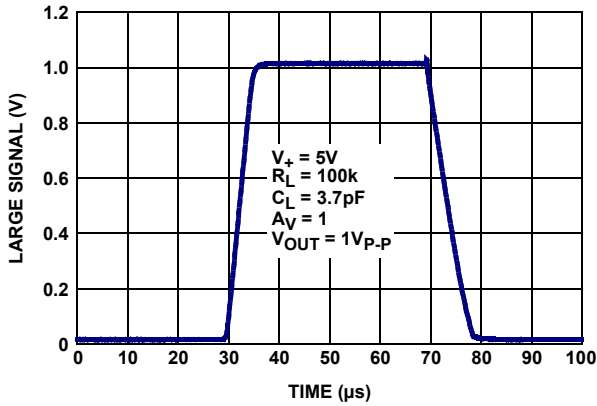


FIGURE 31. LARGE SIGNAL STEP RESPONSE (1V)

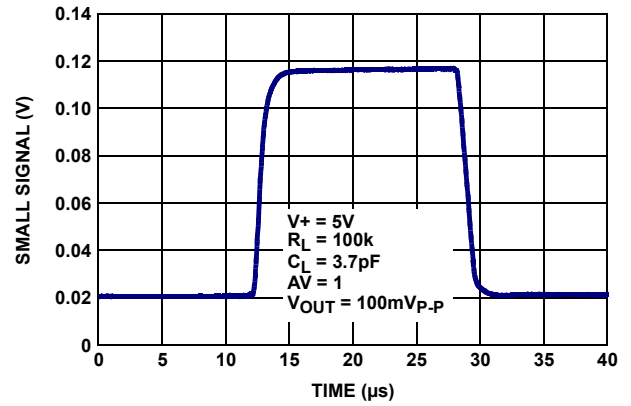


FIGURE 32. SMALL SIGNAL STEP RESPONSE (100mV)

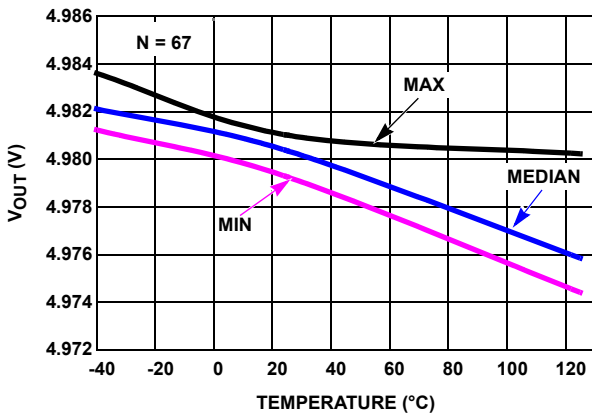


FIGURE 33.  $V_{OUT}$  HIGH vs TEMPERATURE,  $R_L = 10k, V_S = 5V$

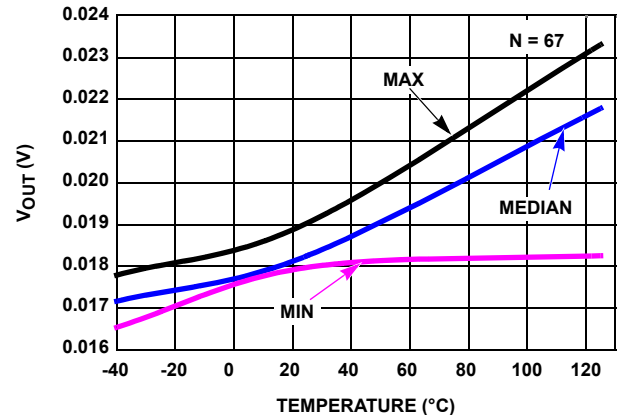


FIGURE 34.  $V_{OUT}$  LOW vs TEMPERATURE,  $R_L = 10k, V_S = 5V$

## Typical Performance Curves $V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = \text{Open. (Continued)}$

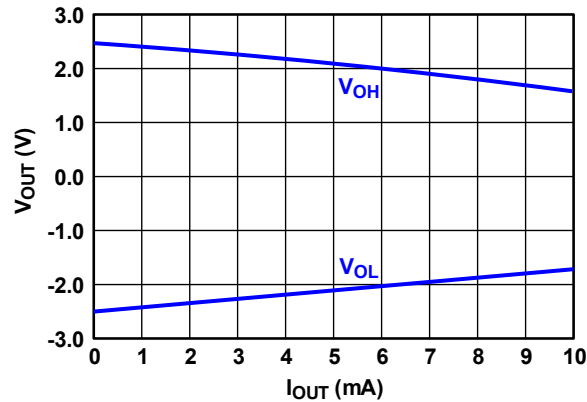


FIGURE 35.  $V_{OH}, V_{OL}$  vs  $I_{OUT}$ ,  $V_S = \pm 2.5V$

## Applications Information

### Functional Description

The ISL28133 uses a proprietary chopper-stabilized architecture shown in the “Block Diagram” on page 2. The ISL28133 combines a 400kHz main amplifier with a very high open loop gain (174dB) chopper stabilized amplifier to achieve very low offset voltage and drift ( $2\mu V, 0.02\mu V/^\circ C$  typical) while consuming only  $18\mu A$  of supply current per channel.

This multi-path amplifier architecture contains a time continuous main amplifier whose input DC offset is corrected by a parallel-connected, high gain chopper stabilized DC correction amplifier operating at 100kHz. From DC to  $\sim 5kHz$ , both amplifiers are active with DC offset correction and most of the low frequency gain is provided by the chopper amplifier. A 5kHz crossover filter cuts off the low frequency amplifier path leaving the main amplifier active out to the 400kHz gain-bandwidth product of the device.

The key benefits of this architecture for precision applications are very high open loop gain, very low DC offset, and low  $1/f$  noise. The noise is virtually flat across the frequency range from a few mHz out to 100kHz, except for the narrow noise peak at the amplifier crossover frequency (5kHz).

### Rail-to-rail Input and Output (RRIO)

The RRIO CMOS amplifier uses parallel input PMOS and NMOS that enable the inputs to swing 100mV beyond either supply rail. The inverting and non-inverting inputs do not have back-to-back input clamp diodes and are capable of maintaining high input impedance at high differential input voltages. This is effective in eliminating output distortion caused by high slew-rate input signals.

The output stage uses common source connected PMOS and NMOS devices to achieve rail-to-rail output drive capability with 17mA current limit and the capability to swing to within 20mV of either rail while driving a  $10k\Omega$  load.

### IN+ and IN- Protection

All input terminals have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to within one diode beyond the supply rails. For applications where either input is expected to exceed the rails by 0.5V, an external series resistor must be used to ensure the input currents never exceed 20mA (see Figure 36).

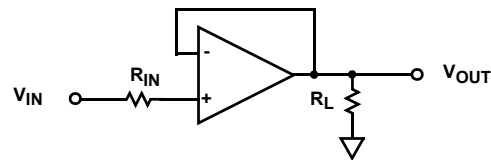


FIGURE 36. INPUT CURRENT LIMITING

### Layout Guidelines for High Impedance Inputs

To achieve the maximum performance of the high input impedance and low offset voltage of the ISL28133 amplifiers, care should be taken in the circuit board layout. The PC board surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board will reduce surface moisture and provide a humidity barrier, reducing parasitic resistance on the board.

### High Gain, Precision DC-Coupled Amplifier

The circuit in Figure 37 implements a single-stage,  $10kV/V$  DC-coupled amplifier with an input DC sensitivity of under  $100nV$  that is only possible using a low  $V_{OS}$  amplifier with high open loop gain. This circuit is practical down to 1.8V due to its rail-to-rail input and output capability. Standard high gain DC amplifiers operating from low voltage supplies are not practical at these high gains using typical low offset precision op amps because the input offset voltage and temperature coefficient consume most of the available output voltage swing. For example, a typical precision amplifier in a gain of  $10kV/V$  with a  $\pm 100\mu V$   $V_{OS}$  and a temperature coefficient of  $0.5\mu V/^\circ C$  would produce a DC error at the output of  $>1V$  with an additional  $5mV/^\circ C$  of temperature dependent error. At 3V, this DC error

consumes > 30% of the total supply voltage, making it impractical to measure sub-microvolt low frequency signals.

The  $\pm 8\mu\text{V}$  max  $V_{OS}$  and  $0.075\mu\text{V}/^\circ\text{C}$  of the ISL28133 produces a temperature stable maximum DC output error of only  $\pm 80\text{mV}$  with a maximum temperature drift of  $0.75\text{mV}/^\circ\text{C}$ . The additional benefit of a very low  $1/f$  noise corner frequency and some feedback filtering enables DC voltages and voltage fluctuations well below  $100\text{nV}$  to be easily detected with a simple single stage amplifier.

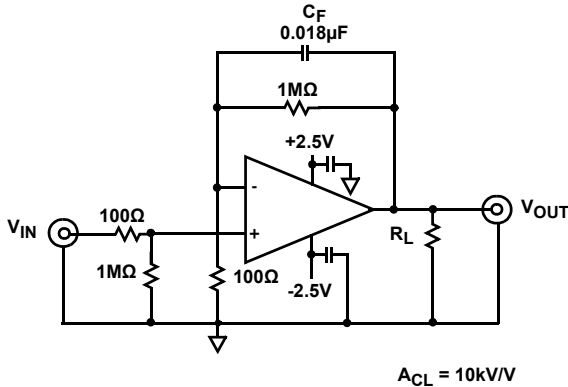


FIGURE 37. HIGH GAIN, PRECISION DC-COUPLED AMPLIFIER

### Long Term $V_{OS}$ Drift

Figure 38 shows a plot of daily  $V_{OS}$  drift measurements of 30 individual ISL28133 amplifiers over a continuous 572 day period at  $+25^\circ\text{C}$ . The 30 units were connected in a gain of 10k, mounted on a single PC board and kept at room temp. The 30 amplifier outputs were measured daily by a DVM and scanner under computer control. The daily  $V_{OS}$  measurements were subtracted from the initial  $V_{OS}$  value to calculate the  $V_{OS}$  shift. The test board was powered from a UPS to maintain uninterrupted power to the test units. Three instances of lost measurement data ranging from 2 days to 2 weeks due to power loss to the measurement scanner were detected, and data were interpolated.

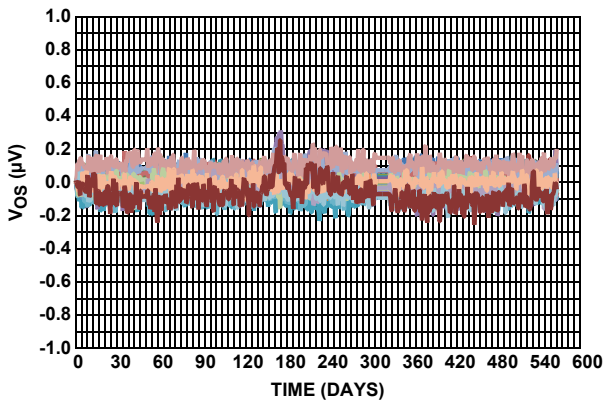


FIGURE 38. LONG TERM DRIFT ( $V_{OS}$  vs TIME) FOR 30 UNITS

The change in amplifier  $V_{OS}$  over the 572 day period for all 30 amplifiers (see Figure 39) was less than  $\pm 100\text{nV}$ , and no clear  $V_{OS}$  long term drift trend was evident in the data. The excellent long term drift performance is a result of the chopper amplifier's ability to measure and correct  $V_{OS}$  errors, leaving only the  $V_{OS}$  error contribution due to changes in the long term stability of the external components (see Figure 40).

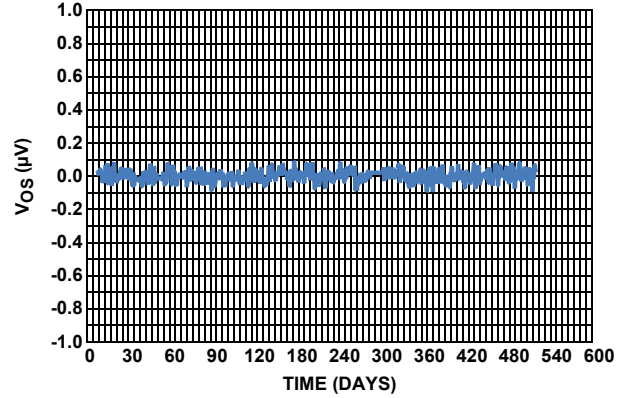


FIGURE 39. LONG TERM DRIFT ( $V_{OS}$  vs TIME) FOR A SINGLE UNIT

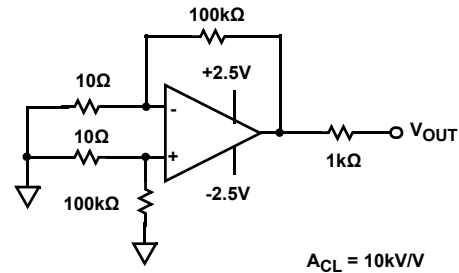


FIGURE 40. LONG TERM DRIFT TEST CIRCUIT

### ISL28133 SPICE Model

Figure 41 shows the SPICE model schematic and Figure 42 shows the net list for the ISL28133 SPICE model. The model is a simplified version of the actual device and simulates important parameters such as noise, Slew Rate, Gain and Phase. The model uses typical parameters from the ISL28133. The poles and zeros in the model were determined from the actual open and closed-loop gain and phase response. This enables the model to present an accurate AC representation of the actual device. The model is configured for ambient temperature of  $+25^\circ\text{C}$ .

Figures 43 through 50 show the characterization vs simulation results for the Noise Density, Frequency Response vs Close Loop Gain, Gain vs Frequency vs CL and Large Signal Step Response (4V).

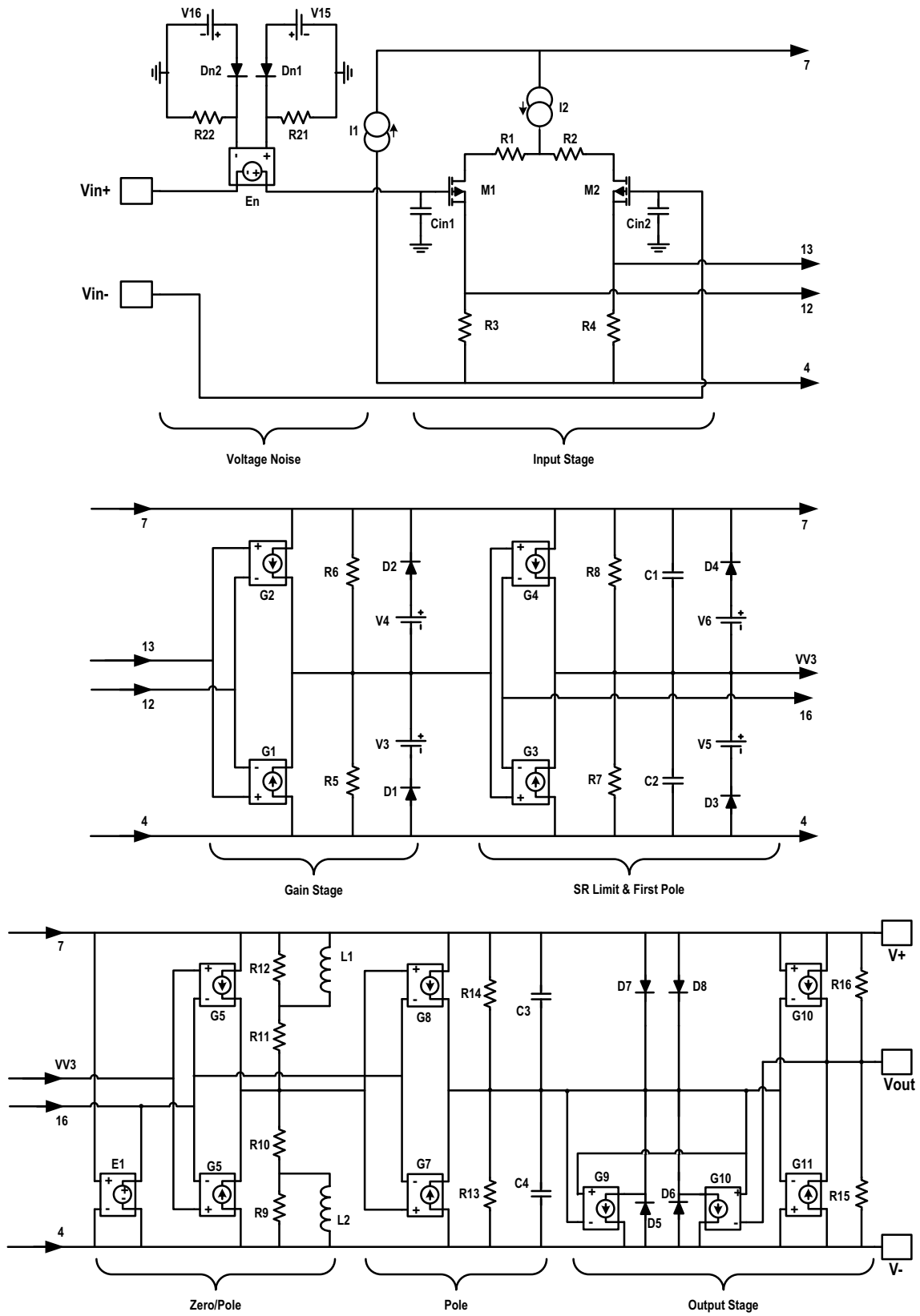


FIGURE 41. SPICE CIRCUIT SCHEMATIC



## Characterization vs Simulation Results

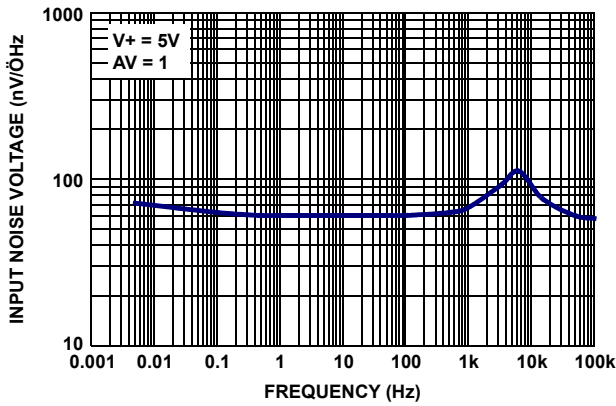


FIGURE 43. CHARACTERIZED INPUT NOISE VOLTAGE DENSITY vs FREQUENCY

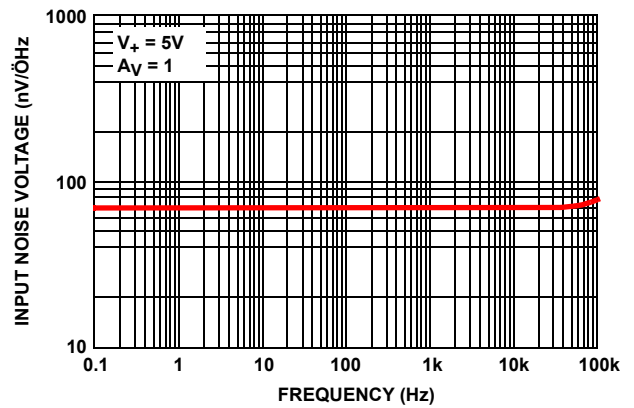


FIGURE 44. SIMULATED INPUT NOISE VOLTAGE DENSITY vs FREQUENCY

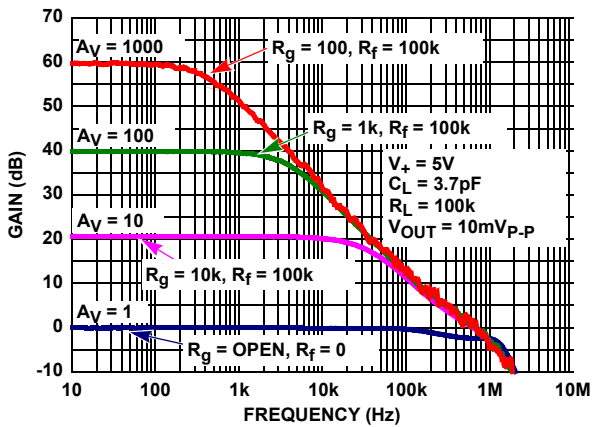


FIGURE 45. CHARACTERIZED FREQUENCY RESPONSE vs CLOSED LOOP GAIN

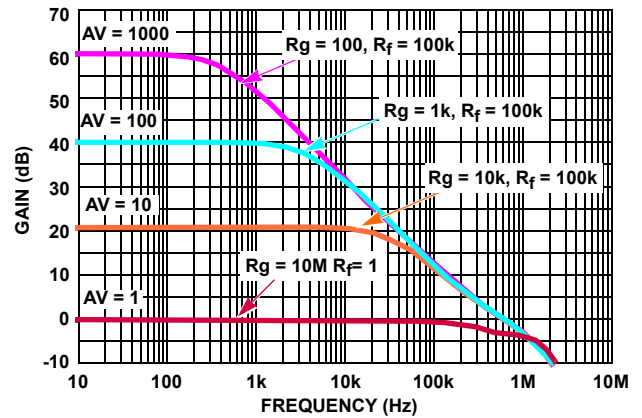


FIGURE 46. SIMULATED FREQUENCY RESPONSE vs CLOSED LOOP GAIN

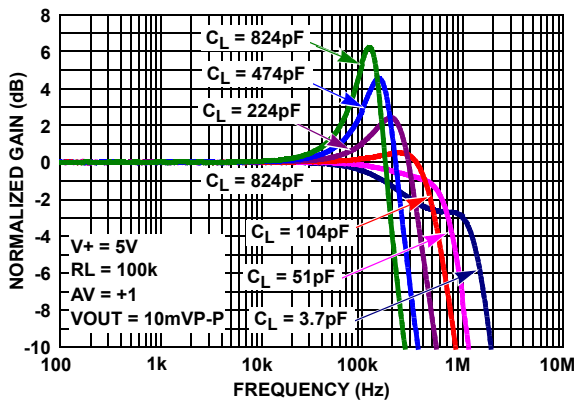


FIGURE 47. CHARACTERIZED GAIN vs FREQUENCY vs  $C_L$

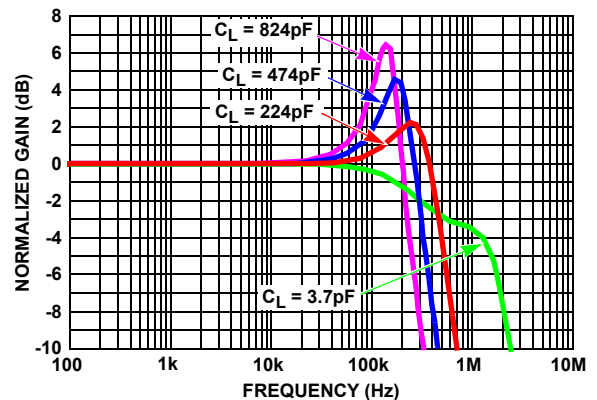


FIGURE 48. SIMULATED GAIN vs FREQUENCY vs  $C_L$

## Characterization vs Simulation Results (Continued)

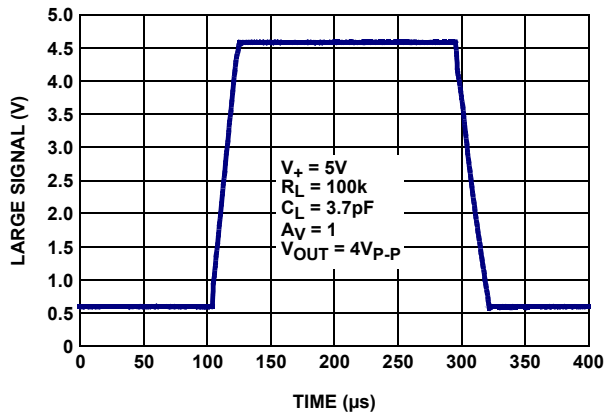


FIGURE 49. CHARACTERIZED LARGE SIGNAL STEP RESPONSE (4V)

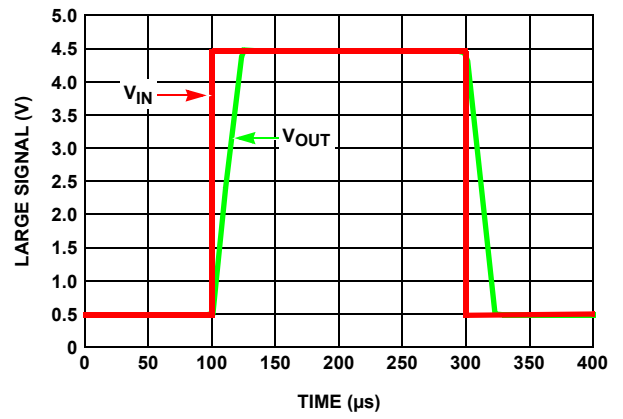


FIGURE 50. SIMULATED LARGE SIGNAL STEP RESPONSE (4V)



## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

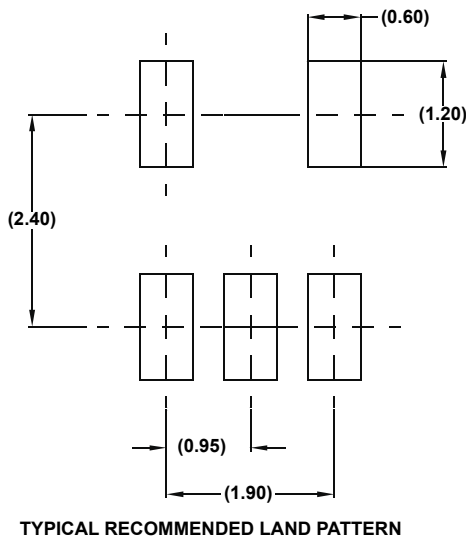
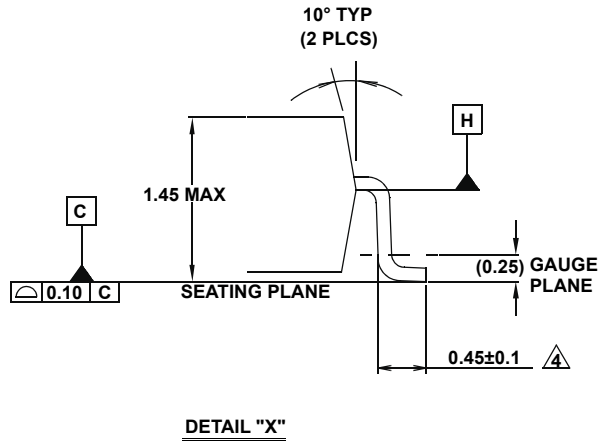
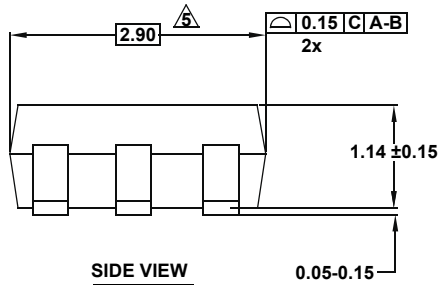
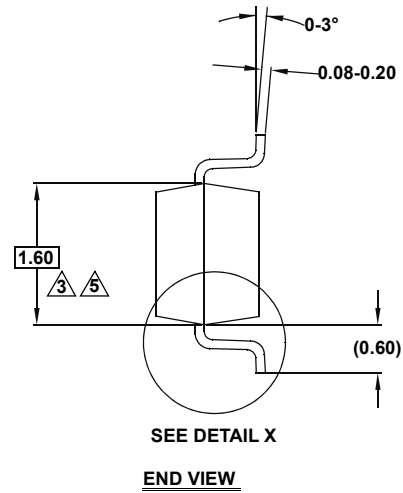
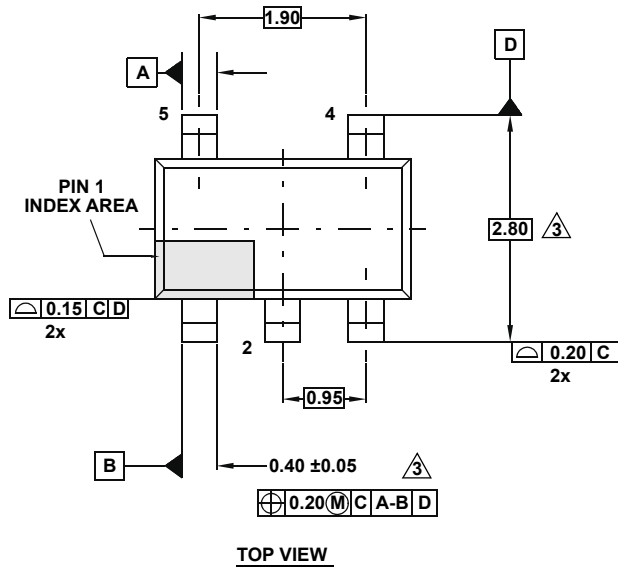
DATE	REVISION	CHANGE
Apr 22, 2021	7.1	Removed retired part and applicable package information from document. Updated the titles for Figure 33 and Figure 34. Added Figure 35. Removed About Intersil section
Sep 16, 2015	7.0	Updated Ordering Information table on page 2. Updated About Intersil Verbiage.
Feb 19, 2014	6.0	Updated location of note references. Added ISL28133CSENSEV1Z to ordering information table on page 2.
May 31, 2011	5.0	Changed minimum operating supply voltage from +1.65V to +1.8V throughout entire datasheet. Added Tjc information for 5 Ld SOT-23 package in Thermal information on page 5.
Feb 1, 2011	4.0	-Converted to Updated Intersil Template. -Page 1 Graphics numbered as Figures 1 and 2. -Updated Ordering Information on page 2 by adding part ISL28133FHZ-T7A. -Changed Note on page 5, which read "Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested." to "Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design." -Added two Long Term Drift Curves (Figures 38 and 39) and section "Long Term VOS Drift" on page 12 -Replaced POD MDP0038 (no dimension changes), now obsolete with P5.064A.
May 3, 2010	3.0	Title Page 1: Replaced "Zero-Drift" with "Chopper Stabilized" for title and part description On page 3: Pin Configuration: MTDFN -> uTDFN On page 7: Figure 12: Changed 0.1Hz to 0.01Hz in Figure caption On page 11: In "Functional Description"; Paragraph 1, 2nd sentence: Changed text from "...open loop gain (200dB)..." -to- "...open loop gain (174dB)..." Changed TYP for "Open Loop Gain" on page 4 from 200dB to 174dB. On page 11: In "High Gain, Precision DC-Coupled Amplifier"; Paragraph 2, 1st sentence: Changed text from "...DC output error of only ±80mV with a maximum temperature drift of 0.75µV/°C." to "... DC output error of only ±80mV with a maximum temperature drift of 0.75mV/C." Removed "Coming Soon" from ISL28133EVAL1Z in the ordering information table on pg 2.
Sep 24, 2009	2.0	Converted to new Intersil template. Removed ISL28233 and ISL28433 from data sheet, added Applications, Related Literature, Typical Application Circuit, Performance Curve, updated ordering information by removing "coming soon" on SC70 and uTDFN packages and adding Eval board listed as "coming soon". Added Block Diagram, Changed in Abs Max Rating Voltage from "5.75V" to "6.5V". Removed Tjc from Thermal Information until provided by packaging scheduled for 9-11-09. Changed Low Offset "drift" to Low Offset "TC", added Max Junction Temp 140C, added SPICE model and simulation results, removed supply current graph at +-3V, re-ordered typical performance curves, removed guard ring information from application section. Added Revision History and Products Information
May 29, 2009	1.0	Page 4: Removed the RL = 100 Curve from Figures 3, 4 and 5. Page 1: Under Features, removed the word "Output" from "Low Output Noise"
Mar 25, 2009	0.0	Initial Release

# Package Outline Drawings

P5.064A

5 Lead Small Outline Transistor Plastic Package

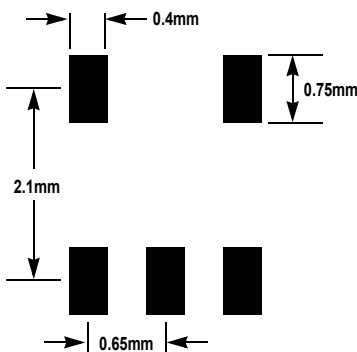
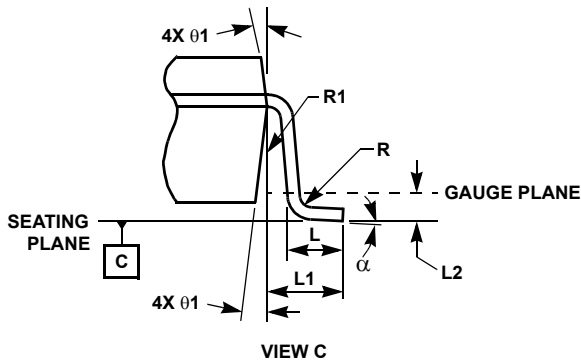
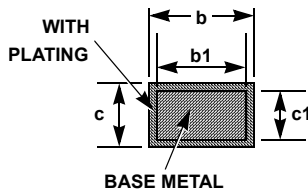
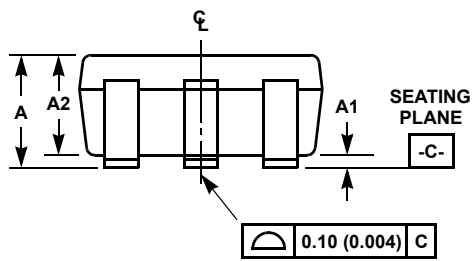
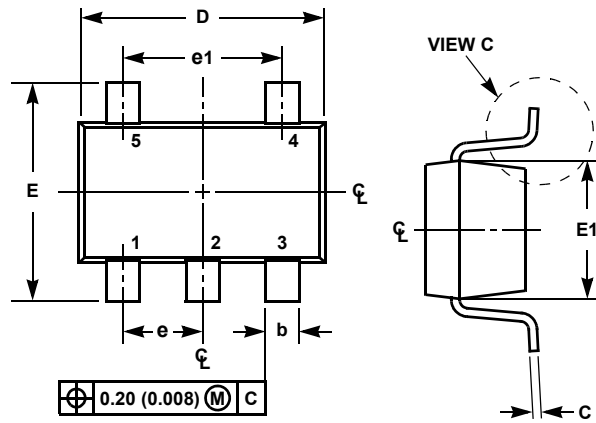
Rev 0, 2/10



**NOTES:**

1. Dimensions are in millimeters.  
Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Dimension is exclusive of mold flash, protrusions or gate burrs.
4. Foot length is measured at reference to gauge plane.
5. This dimension is measured at Datum "H".
6. Package conforms to JEDEC MO-178AA.

**Small Outline Transistor Plastic Packages (SC70-5)**



TYPICAL RECOMMENDED LAND PATTERN

**P5.049**

**5 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.031	0.043	0.80	1.10	-
A1	0.000	0.004	0.00	0.10	-
A2	0.031	0.039	0.80	1.00	-
b	0.006	0.012	0.15	0.30	-
b1	0.006	0.010	0.15	0.25	-
c	0.003	0.009	0.08	0.22	6
c1	0.003	0.009	0.08	0.20	6
D	0.073	0.085	1.85	2.15	3
E	0.071	0.094	1.80	2.40	-
E1	0.045	0.053	1.15	1.35	3
e	0.0256 Ref		0.65 Ref		-
e1	0.0512 Ref		1.30 Ref		-
L	0.010	0.018	0.26	0.46	4
L1	0.017 Ref.		0.420 Ref.		-
L2	0.006 BSC		0.15 BSC		-
alpha	0°	8°	0°	8°	-
N	5		5		5
R	0.004	-	0.10	-	-
R1	0.004	0.010	0.15	0.25	-

Rev. 3 7/07

NOTES:

1. Dimensioning and tolerances per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC70 and JEDEC MO-203AA.
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength L measured at reference to gauge plane.
5. "N" is the number of terminal positions.
6. These Dimensions apply to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
7. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:  
[www.renesas.com/contact/](http://www.renesas.com/contact/)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.