1-To-1 Differential-to-LVCMOS/LVTTL Translator

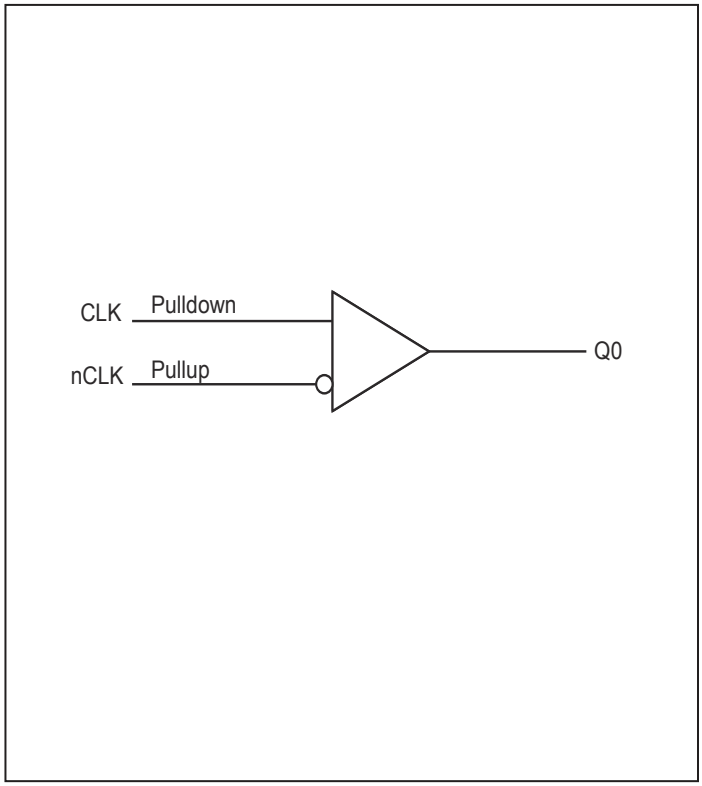
Features

- One LVCMOS/LVTTL output
- Differential CLK/nCLK input pair
- CLK/nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Output frequency: 360MHz
- Part-to-part skew: 500ps (maximum)
- Additive phase jitter, RMS: 0.09ps (typical), 3.3V output
- Full 3.3V and 2.5V operating supply
- -40°C to 85°C ambient operating temperature

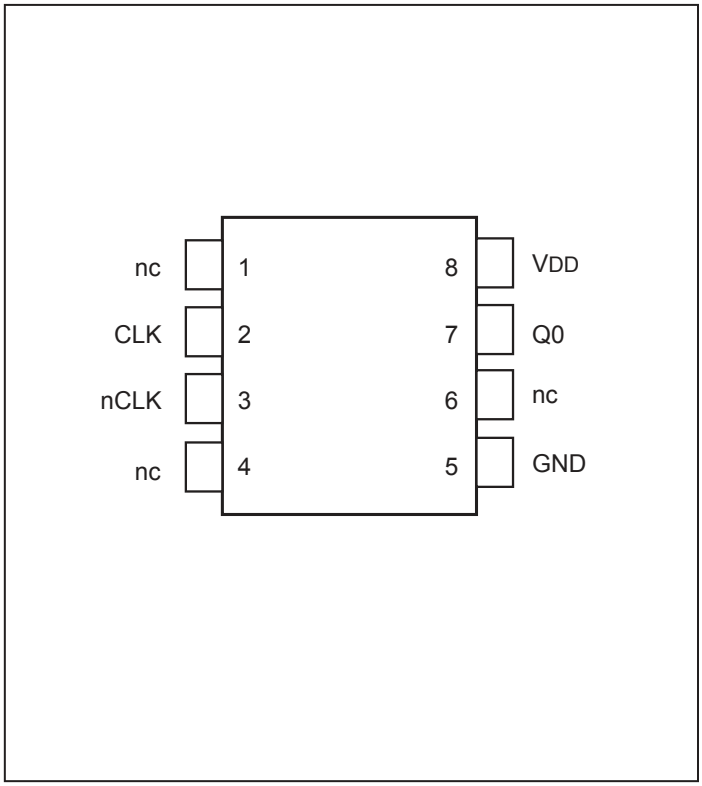
Description

The PI6C49X0201 is a 1-to-1 Differential-to-LVCMOS/LVTTL Translator High Performance Buffer. The differential input is highly flexible and can accept LVPECL, LVDS, LVHSTL, SSTL, and HCSL. The small 8-lead SOIC footprint makes this device ideal for use in applications with limited board space.

Block Diagram



Pin Assignment



Pin Descriptions

Pin#	Pin Name	Pin Type		Pin Description
1, 4, 6	nc	Unused		No connect.
2	CLK	Input	Pulldown	Non-inverting differential clock input.
3	nCLK	Input	Pullup	Inverting differential clock input.
5	GND	Power		Power supply ground.
7	Q0	Output		Single-ended clock output. LVCMOS/LVTTL interface levels.
8	VDD	Power		Positive supply pin.

Note: *Pullup* and *Pulldown* refer to internal input resistors.

Pin Characteristics

Symbol	Parameter	Test Conditions	Min.	Typical	Max.	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance	VDD = 3.6V		23		pF
R_{OUT}	Output Impedance		5	7	13	Ω

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Supply Voltage, VDD 4.6V
Inputs, V_I .....–0.5V to VDD +0.5V
Output, V_O .....–0.5V to VDD +0.5V
Package Thermal Impedance, θ_{JA} .....103°C/W (0 lfpm)
Storage Temperature, T_{STG} .....-65°C to 150°C
ESD Protection (Input) ..... 2000V min (HBM)

Note:

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the DC Characteristics or AC Characteristics

is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

DC Electrical Characteristics

Power Supply DC Characteristics, VDD = 3.3V ± 0.3V or 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD	Positive Supply Voltage		3.0	3.3	3.6	V
			2.375	2.5	2.625	V
IDD	Power Supply Current	25MHz, unloaded			25	mA
		250MHz, unloaded			35	mA

LVCMOS / LVTTL DC Characteristics, VDD = 3.3V ± 0.3V or 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage; NOTE 1	VDD = 3.6V	2.6		3.6	V
		VDD = 2.625V	1.8		2.625	V
V_{OL}	Output Low Voltage; NOTE 1	VDD = 3.6V or 2.625V			0.5	V

NOTE 1: Outputs terminated with 50Ω to VDD/2.

Differential DC Characteristics, VDD = 3.3V ± 0.3V or 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Units
I_{IH}	Input High Current	nCLK	V_{IN} = VDD = 3.6V or 2.625V			5	µA
		CLK	V_{IN} = VDD = 3.6V or 2.625V			150	µA
I_{IL}	Input Low Current	nCLK	V_{IN} = 0V, VDD = 3.6V or 2.625V	-150			µA
		CLK	V_{IN} = 0V, VDD = 3.6V or 2.625V	-5			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CRM}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		VDD – 0.85	V

NOTE 1: For single ended applications, the maximum input voltage for CLK, nCLK is VDD + 0.3V.

NOTE 2: Common mode voltage is defined as (V_{IH} + V_{IL})/2.

AC Electrical Characteristics

AC Characteristics, VDD = 3.3V ± 0.3V, T_A = -40°C to 85°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{MAX}	Output Frequency		4		360	MHz
t_{PD}	Propagation Delay, NOTE 1	$f \leq 350$MHz	1.6	1.8	2.0	ns
tsk(pp)	Part-to-Part Skew; NOTE 2, 3				500	ps
tjit	Buffer Additive Phase Jitter, RMS	156.25MHz, Integration Range (12kHz – 20MHz)		0.09		ps
		125MHz, Integration Range (12kHz – 20MHz)		0.15		
t_R/t_F	Output Rise/Fall Time	0.8V to 2V	80	250	350	ps
odc	Output Duty Cycle	$f \leq 166$MHz	45	50	55	%
		166MHz < $f \leq 350$MHz	40	50	60	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range. The device will meet specifications after thermal equilibrium has been reached under these conditions.

All parameters measured at f_{MAX} unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the output at VDD/2.

NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at VDD/2.

AC Characteristics, VDD = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{MAX}	Output Frequency		4		360	MHz
t_{PD}	Propagation Delay, NOTE 1	$f \leq 350$MHz	1.9	2.2	2.5	ns
tsk(pp)	Part-to-Part Skew; NOTE 2				500	ps
tjit	Buffer Additive Phase Jitter, RMS	156.25MHz, Integration Range (12kHz – 20MHz)		0.04		ps
		125MHz, Integration Range (12kHz – 20MHz)		0.14		
t_R/t_F	Output Rise/Fall Time	20% to 80%	180		350	ps
odc	Output Duty Cycle	$f \leq 250$MHz	45	50	55	%
		250MHz < $f \leq 350$MHz	40	50	60	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range. The device will meet specifications after thermal equilibrium has been reached under these conditions.

All parameters measured at f_{MAX} unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the output at VDD/2.

NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at VDD/2.

Application Information

Wiring the differential input to accept single ended levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = VDD/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to postion the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and VDD = 3.3V, V_REF should be 1.25V and R1/R2 = 0.609.

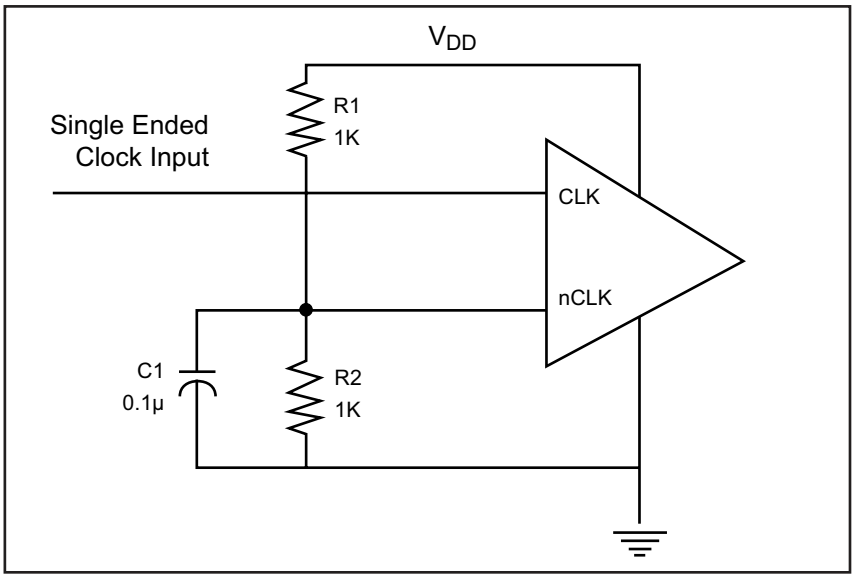
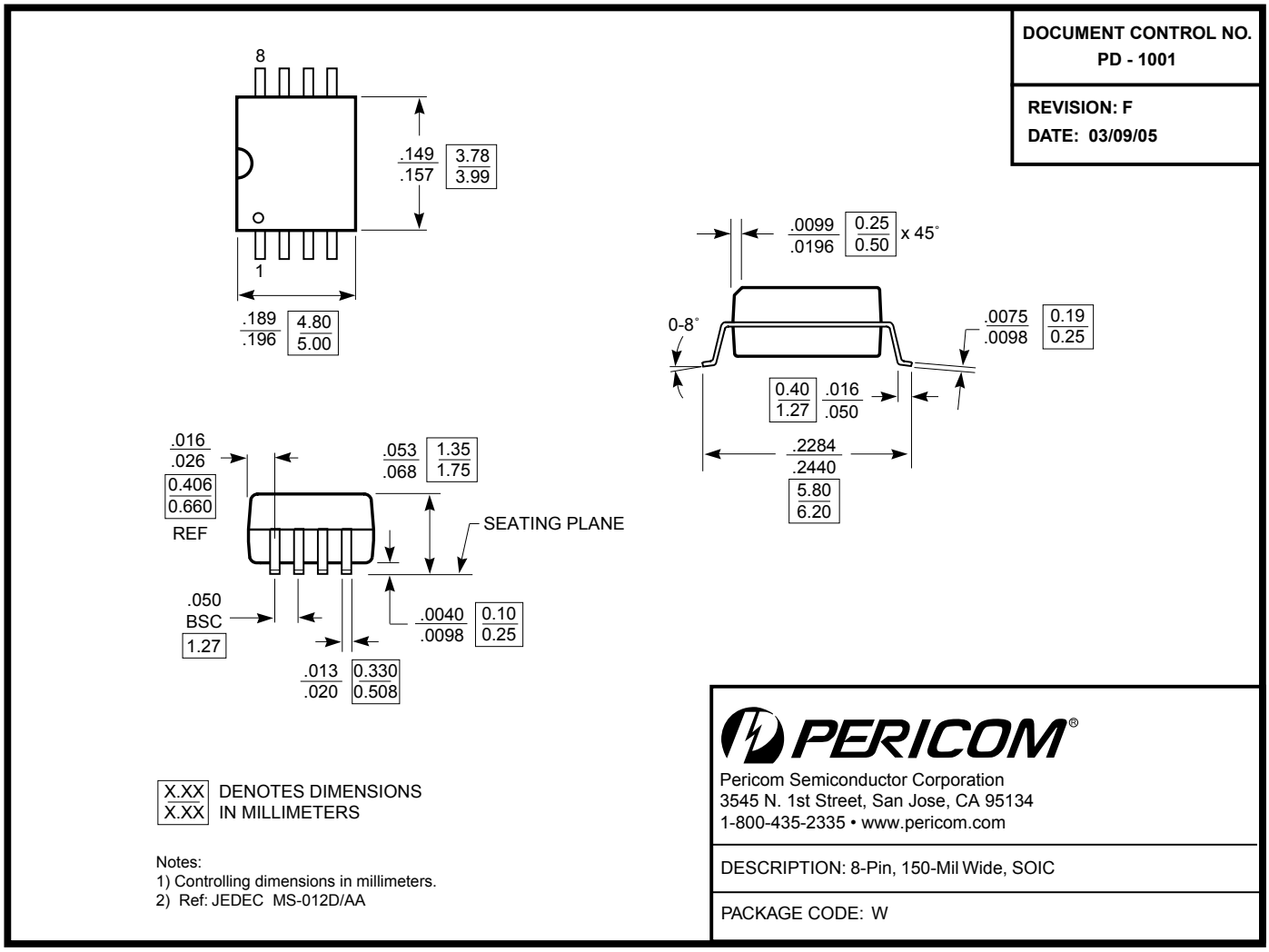


Figure 1. Single-ended input to Differential input device

Thermal Information

Symbol	Description	Condition	
Θ_{JA}	Junction-to-ambient thermal resistance	Still air	157 °C/W
Θ_{JC}	Junction-to-case thermal resistance		42 °C/W



Note:
- For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information(1-3)

Ordering Code	Package Code	Package Description
PI6C49X0201WIE	W	8-pin, Pb-free & Green, SOIC

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green
3. Adding an X suffix = Tape/Reel