Low Charge Injection, 8-Channel, Unipolar, Negative High Voltage, Analog Switch With Bleed Resistors

Features

- Low on-resistance, 14Ω max.
- Integrated bleed resistors on the outputs
- 3.3 or 5.0V CMOS input logic level
- 20MHz data shift clock frequency
- Very low quiescent power dissipation (-10µA)
- Low parasitic capacitance
- ***DC to 50MHz small signal frequency response***
- -60dB typical off-isolation at 5.0MHz
- CMOS logic circuitry for low power
- Excellent noise immunity
- Cascadable serial data register with latches

Applications

- NDT metal flaw detection
- Medical ultrasound imaging
- Piezoelectric transducer drivers
- Inkjet printer heads
- Optical MEMS modules

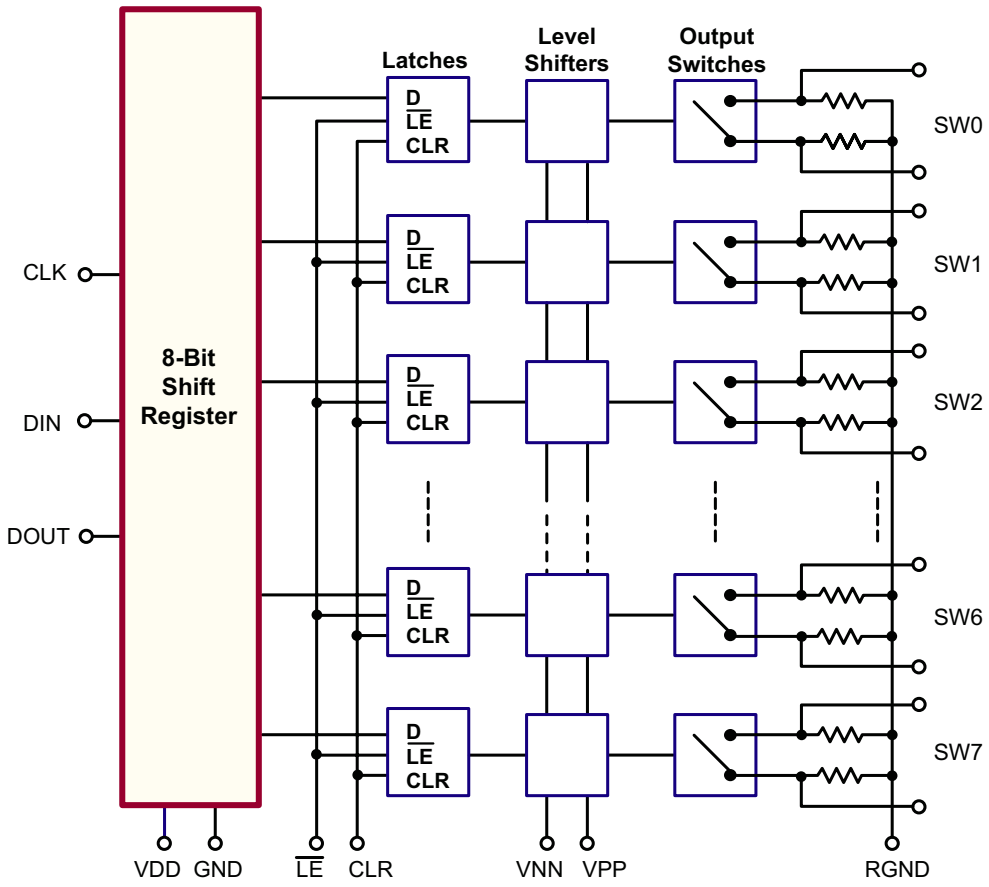
General Description

The Supertex HV2321 is a low charge injection, 8-channel, unipolar, negative high voltage, analog switch integrated circuit (IC) with bleed resistors. The device can be used in applications requiring high voltage switching controlled by low voltage signals, such as NDT metal flaw detection, medical ultrasound imaging, piezoelectric transducer drivers, and printers. The bleed resistors eliminate voltage built up on capacitive loads such as piezoelectric transducers.

Data is input into an 8-bit shift register and then retained in an 8-bit latch. To reduce any possible clock feed-through noise, the latch enable bar should be left high until all bits are clocked in. Data is clocked in during the rising edge of the clock.

Using HVCMOS technology, this device combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

Block Diagram

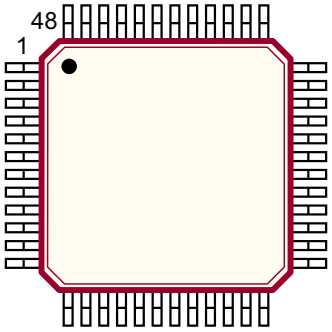


Ordering Information

Device	48-Lead LQFP *7.00x7.00mm body* *1.60mm height (max)* *0.50mm pitch*
HV2321	HV2321FG-G

-G indicates package is RoHS compliant ('Green')

Pin Configuration



48-Lead LQFP (FG)

Absolute Maximum Ratings

Parameter	Value
V_{DD} logic supply	-0.5V to +7.0V
V_{PP}-V_{NN} differential supply	260V
V_{PP} positive supply	-0.5V to V_{NN}+260V
V_{NN} negative supply	+0.5V to -250V
Logic input voltage	-0.5V to V_{DD} +0.3V
Analog signal range	V_{NN} to V_{PP}
Peak analog signal current/channel	4.5A
Storage temperature	-65°C to 150°C
Power dissipation	1.0W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Product Marking

Top Marking

Bottom Marking

YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*
____ = "Green" Packaging

**May be part of top marking*

Package may or may not include the following marks: Si or

48-Lead LQFP (FG)

Operating Conditions

Sym	Parameter	Value
V_{DD}	Logic power supply voltage	3.0V to 5.5V
V_{PP} - V_{NN}	Supply voltage differential	240V
V_{PP}	Positive driver supply	+15V to +50V
V_{NN}	Negative high voltage supply	-100V to -225V
V_{IH}	High level input voltage	0.9V_{DD} to V_{DD}
V_{IL}	Low-level input voltage	0V to 0.1V_{DD}
V_{SIG}	Analog signal voltage peak-to-peak	V_{NN} +10V to V_{PP} -10V
T_A	Operating free air temperature	0°C to 70°C

Notes:

1. *Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.*
2. *V_{SIG} must be $V_{NN} \le V_{SIG} \le V_{PP}$ or floating during power up/down transition.*
3. *Rise and fall times of power supplies V_{DD}, V_{PP} and V_{NN} should not be less than 1.0msec.*

DC Electrical Characteristics

(Over operating conditions unless otherwise specified)

Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions	
		Min	Max	Min	Typ	Max	Min	Max			
R_{ONS}	Small signal switch on-resistance	-	-	-	-	14	-	-	Ω	I_{SIG} = 5.0mA	V_{PP} = +50V, V_{NN} = -190V
		-	-	-	-	14	-	-		I_{SIG} = 200mA	
		-	-	-	-	15	-	-		I_{SIG} = 5.0mA	V_{PP} = +40V, V_{NN} = -200V
		-	-	-	-	15	-	-		I_{SIG} = 200mA	
		-	--	-	-	23	-	-		I_{SIG} = 5.0mA	V_{PP} = +15V, V_{NN} = -225V
		-	-	-	-	23	-	-		I_{SIG} = 200mA	
ΔR_{ONS}	Small signal switch on-resistance matching	-	20	-	5.0	20	-	20	%	I_{SIG} = 5.0mA, V_{PP} = +40V, V_{NN} = -200V	
R_{ONL}	Large signal switch on-resistance	-	-	-	9.2	-	-	-	Ω	V_{SIG} = 0V, I_{SIG} = -1.0A	
R_{INT}	Output switch bleed resistor	-	-	30	50	70	-	-	KΩ	Switch outputs to RGND pin	
I_{SOL}	Switch off-leakage per switch	-	5.0	-	1.0	10	-	15	µA	V_{SIG} = V_{PP} -10V, V_{NN} +10V	
$V_{OS(OFF)}$	DC offset switch off	-	300	-	100	300	-	300	mV	100KΩ load	
$V_{OS(ON)}$	DC offset switch on	-	500	-	100	500	-	500			
I_{DDQ}	Quiescent V_{DD} supply current	-	-	-	-	50	-	-	µA	All switches off	
I_{PPQ}	Quiescent V_{PP} supply current	-	-	-	-	50	-	-			
I_{NNQ}	Quiescent V_{NN} supply current	-	-	-	-	-50	-	-			
I_{DDQ}	Quiescent V_{DD} supply current	-	-	-	-	50	-	-	µA	All switches on, I_{SW} = 5.0mA	
I_{PPQ}	Quiescent V_{PP} supply current	-	-	-	-	50	-	-			
I_{NNQ}	Quiescent V_{NN} supply current	-	-	-	-	-50	-	-			
I_{SW}	Switch output peak current	-	-	-	4.5	-	-	-	A	V_{SIG} duty cycle < 0.1%, 1.0µs	V_{PP} = +50V, V_{NN} = -190V
		-	-	-	4.0	-	-	-			V_{PP} = +40V, V_{NN} = -200V
		-	-	-	2.0	-	-	-			V_{PP} = +15V, V_{NN} = -225V
f_{SW}	Output switching frequency	-		-	-	50	-	-	kHz	Duty cycle = 50%	
I_{PP}	Average V_{PP} supply current	-	-	-	5.6	7.5	-	-	mA	V_{PP} = +40V, V_{NN} = -200V	50kHz output switching frequency with no load
		-	-	-	5.6	7.5	-	-		V_{PP} = +50V, V_{NN} = -190V	
		-	-	-	5.6	7.5	-	-		V_{PP} = +15V, V_{NN} = -225V	
I_{NN}	Average V_{NN} supply current	-	-	-	5.8	7.5	-	-	mA	V_{PP} = +40V, V_{NN} = -200V	50kHz output switching frequency with no load
		-	-	-	5.8	7.5	-	-		V_{PP} = +50V, V_{NN} = -190V	
		-	-	-	5.8	7.5	-	-		V_{PP} = +15V, V_{NN} = -225V	
I_{DD}	Average V_{DD} supply current	-	4.5	-	-	4.5	-	4.5	mA	f_{CLK} = 5.0MHz, V_{DD} = 5.0V	
I_{DDQ}	Quiescent V_{DD} supply current	-	10	-	-	10	-	10	µA	All logic inputs are static	
I_{SOR}	D_{OUT} source current	0.45	-	0.45	0.70	-	0.40	-	mA	V_{OUT} = V_{DD} -0.7V	
I_{SINK}	D_{OUT} sink current	0.45	-	0.45	0.70	-	0.40	-	mA	V_{OUT} = 0.7V	
C_{IN}	Logic input capacitance	-	10	-	-	10	-	10	pF	---	

AC Electrical Characteristics

(Over recommended operating conditions: V_{DD} = +5.0V, t_R = t_F ≤5.0ns, 50% duty cycle, V_{PP} = +40V, V_{NN} = -200V, C_{LOAD} = 20pF, unless otherwise specified)

Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions
		Min	Max	Min	Typ	Max	Min	Max		
t_{SD}	Set up time before $\overline{LE}$ rises	-	-	25	-	-	-	-	ns	---
t_{WLE}	Time width of $\overline{LE}$	-	-	-	56	-	-	-	ns	V_{DD} = 3.0V
		-	-	-	12	-	-	-		V_{DD} = 5.0V
t_{DO}	Clock delay time to data out	-	-	-	78	-	-	-	ns	V_{DD} = 3.0V
		-	-	-	30	-	-	-		V_{DD} = 5.0V
t_{WCL}	Time width of CLR	-	-	55	-	-	-	-	ns	---
t_{SU}	Set up time data to clock	-	-	-	21	-	-	-	ns	V_{DD} = 3.0V
		-	-	-	7.0	-	-	-		V_{DD} = 5.0V
t_H	Hold time data from clock	2.0	-	2.0	-	-	2.0	-	ns	V_{DD} = 3.0 or 5.0V
f_{CLK}	Clock frequency	-	-	-	-	8.0	-	-	MHz	V_{DD} = 3.0V
		-	-	-	-	20	-	-		V_{DD} = 5.0V
t_R, t_F	Clock rise and fall times	-	50	-	-	50	-	50	ns	---
t_{ON}	Turn on time	-	5.0	-	-	5.0	-	5.0	µs	V_{SIG} = -100V, R_{LOAD} = 10kΩ to GND
t_{OFF}	Turn off time	-	5.0	-	-	5.0	-	5.0		
dv/dt	Maximum V_{SIG} slew rate	-	20	-	-	20	-	20	V/ns	V_{PP} = +40V, V_{NN} = -200V
		-	20	-	-	20	-	20		V_{PP} = +50V, V_{NN} = -190V
		-	20	-	-	20	-	20		V_{PP} = +15V, V_{NN} = -225V
K_O	Off isolation	-30	-	-30	-33	-	-30	-	dB	f = 5.0MHz, V_{OFFSET} = -15V, 1.0KΩ/15pF load
		-58	-	-58	-	-	-58	-		f = 5.0MHz, V_{OFFSET} = -15V, 50Ω load
K_{CR}	Switch crosstalk	-	-	-60	-	-	-	-	dB	f = 5.0MHz, V_{OFFSET} = -15V, 50Ω load
I_{ID}	Output switch isolation diode current	-	300	-	-	300	-	300	mA	300ns pulse width, 2.0% duty cycle
$C_{SG(OFF)}$	Off capacitance SW to GND	-	-	-	18	-	-	-	pF	f = 1.0MHz, V_{OFFSET} = -15V
$C_{SG(ON)}$	On capacitance SW to GND	-	-	-	70	-	-	-	pF	f = 1.0MHz, V_{OFFSET} = -15V
$+V_{SPK}$	Output voltage spike	-	-	-	59	-	-	-	mV	V_{PP} = +40V, V_{NN} = -200V, R_{LOAD} = 50Ω
$-V_{SPK}$		-	-	-	115	-	-	-		
$+V_{SPK}$		-	-	-	71	-	-	-		V_{PP} = +50V, V_{NN} = -190V, R_{LOAD} = 50Ω
$-V_{SPK}$		-	-	-	115	-	-	-		
$+V_{SPK}$		-	-	-	56	-	-	-		V_{PP} = +15V, V_{NN} = -225V, R_{LOAD} = 50Ω
$-V_{SPK}$		-	-	-	115	-	-	-		
QC	Charge injection	-	-	-	1950	-	-	-	pC	V_{PP} = +40V, V_{NN} = -200V, V_{SIG} = 0V
		-	-	-	1890	-	-	-		V_{PP} = +50V, V_{NN} = -190V, V_{SIG} = 0V
		-	-	-	2110	-	-	-		V_{PP} = +15V, V_{NN} = -225V, V_{SIG} = 0V

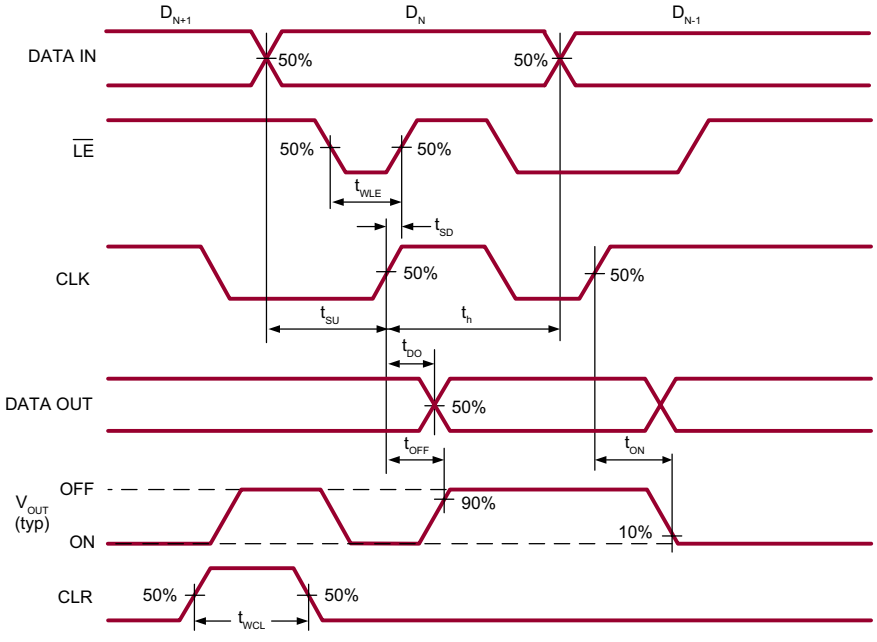
Truth Table

D0	D1	D2	D3	D4	D5	D6	D7	$\overline{LE}$	CLR	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	L	Off							
H								L	L	On							
	L							L	L		Off						
	H							L	L		On						
		L						L	L			Off					
		H						L	L			On					
			L					L	L				Off				
			H					L	L				On				
				L				L	L					Off			
				H				L	L					On			
					L			L	L						Off		
					H			L	L						On		
						L		L	L							Off	
						H		L	L							On	
							L	L	L								Off
							H	L	L								On
X	X	X	X	X	X	X	X	H	L	Hold Previous State							
X	X	X	X	X	X	X	X	X	H	All Switches Off							

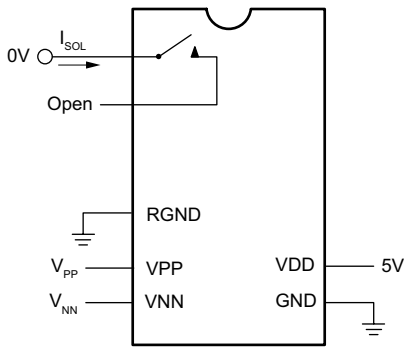
Notes:

1. *The eight switches operate independently.*
2. *Serial data is clocked in on the L to H transition of the CLK.*
3. *The switches go to a state retaining their present condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low the shift register data flow through the latch.*
4. *D_{OUT} is high when data in the shift register 7 is high.*
5. *Shift register clocking has no effect on the switch states if $\overline{LE}$ is high.*
6. *The CLR clear input overrides all other inputs.*

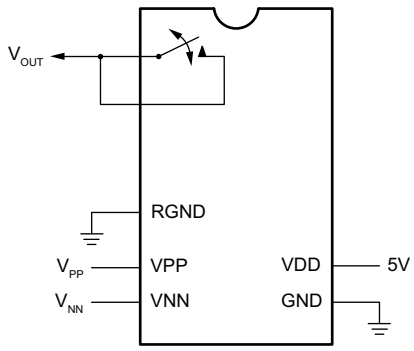
Logic Timing Waveforms



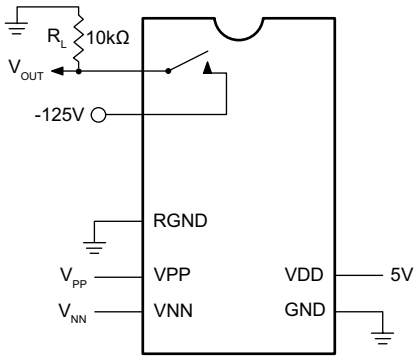
Test Circuits



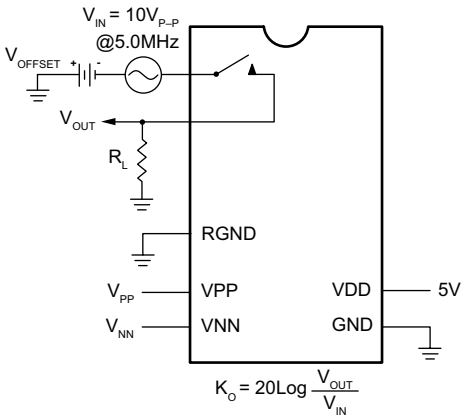
Switch OFF Leakage



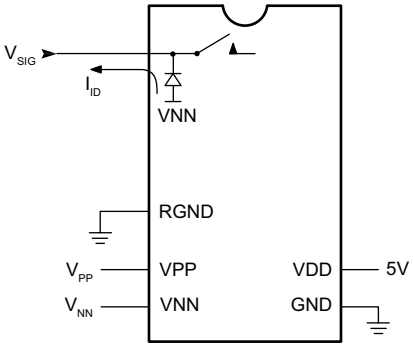
DC Offset ON/OFF



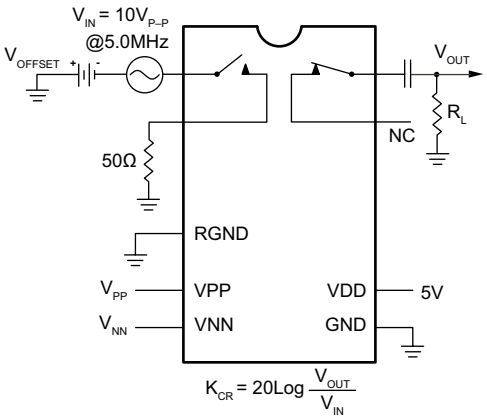
T_{ON}/T_{OFF} Test Circuit



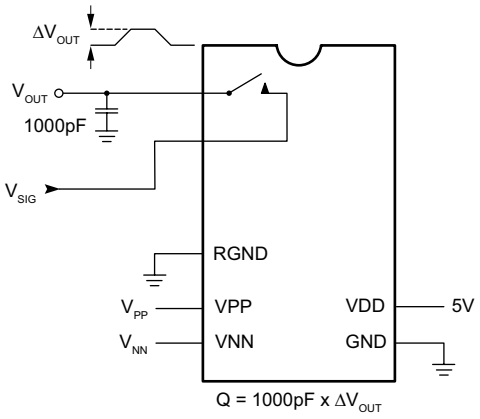
OFF Isolation



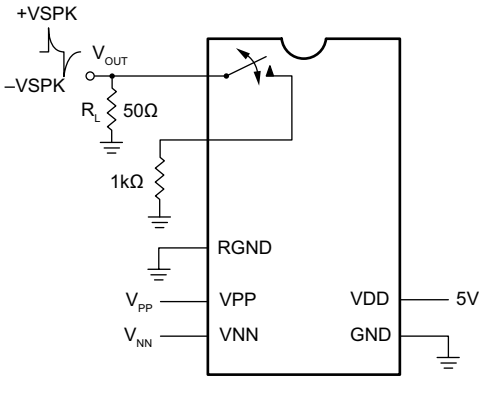
Isolation Diode Current



Crosstalk



Charge Injection



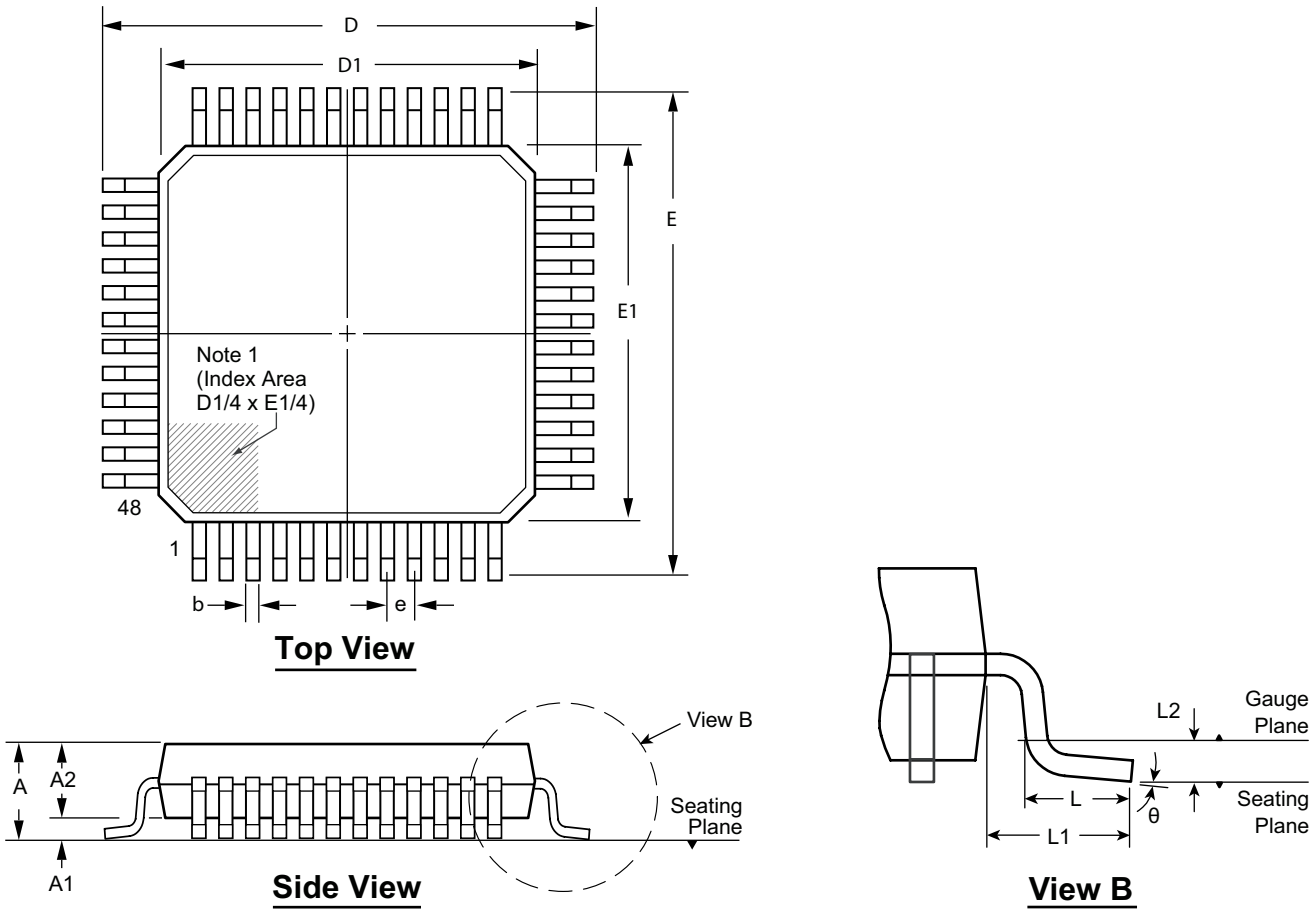
Output Voltage Spike

Pin Configuration - 48-Lead LQFP (FG)

Pin #	Pin Name	Pin #	Pin Name
1	SW5	25	VNN
2	NC	26	NC
3	SW4	27	RGND
4	NC	28	GND
5	SW4	29	VDD
6	NC	30	NC
7	NC	31	NC
8	SW3	32	NC
9	NC	33	DIN
10	SW3	34	CLK
11	NC	35	$\overline{\text{LE}}$
12	SW2	36	CLR
13	NC	37	DOUT
14	SW2	38	NC
15	NC	39	SW7
16	SW1	40	NC
17	NC	41	SW7
18	SW1	42	NC
19	NC	43	SW6
20	SW0	44	NC
21	NC	45	SW6
22	SW0	46	NC
23	NC	47	SW5
24	VPP	48	NC

48-Lead LQFP Package Outline (FG)

7.00x7.00mm body, 1.60mm height (max), 0.50mm pitch



Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ
Dimension (mm)	MIN	1.40*	0.05	1.35	0.17	8.80*	6.80*	8.80*	6.80*	0.50 BSC	0.45	1.00 REF	0.25 BSC	0°
	NOM	-	-	1.40	0.22	9.00	7.00	9.00	7.00		0.60			3.5°
	MAX	1.60	0.15	1.45	0.27	9.20*	7.20*	9.20*	7.20*		0.75			7°

JEDEC Registration MS-026, Variation BBC, Issue D, Jan. 2001.
** This dimension is not specified in the JEDEC drawing.*

Drawings are not to scale.

Supertex Doc. #: *DSPD-48LQFPFG Version, D041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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