# CAT4103

# 3-Channel Constant-Current RGB LED Driver

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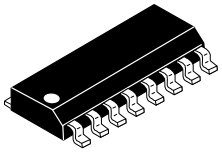


**SOIC−16**
**V SUFFIX**
**CASE 751BG**

### Description

The CAT4103 is a 3−channel, linear based constant−current LED driver designed for RGB LED control, requiring no inductor and provides a low noise operation. LED channel currents up to 175 mA are programmed independently via separate external resistors. Low output voltage operation of 0.4 V at 175 mA allows for more power efficient designs across wider supply voltage range. The three LED pins are compatible with high voltage up to 25 V supporting applications with long strings of LEDs.

A high−speed 4−wire 25 MHz serial interface controls each individual channel using a shift register and latch configuration. Output data pins allow multiple devices to be cascaded and programmed via one serial interface with no need for external drivers or timing considerations. The device also includes a blanking control pin (BIN) that can be used to disable all channels independently of the interface.

Thermal shutdown protection is incorporated in the device to disable the LED outputs whenever the die temperature exceeds 150°C.

The device is available in a 16−lead SOIC package.

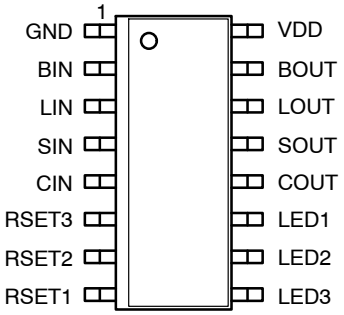
### Features

- 3 Independent Current Sinks Rated to 25 V
- LED Current to 175 mA per Channel Set by Separate External Resistors
- High−speed 25 MHz 4−wire Serial Interface
- Buffered Output Drivers to Ensure Data Integrity
- Cascadable Devices
- Low Dropout Current Source (0.4 V at 175 mA)
- 3 V to 5.5 V Logic Supply
- Thermal Shutdown Protection
- 16−lead SOIC Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

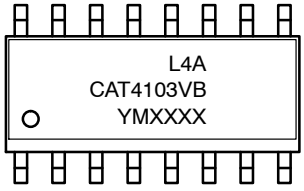
- Multi−color, Intelligent LED, Architectural Lighting
- High−visual Impact LED Signs and Displays
- LCD Backlight

### PIN CONNECTIONS




(Top View)

### MARKING DIAGRAM




L = Assembly Location
4 = Lead Finish − NiPdAu
A = Product Revision (Fixed as “A”)
CAT4103V = Device Code
B = Leave Blank
Y = Production Year (Last Digit)
M = Production Month (1−9, A, B, C)
XXXX = Last Four Digits of Assembly Lot Number

### ORDERING INFORMATION

| Device | Package | Shipping |
|---|---|---|
| CAT4103V−GT2 (Note 1) | SOIC−16 (Pb−Free) | 2,000/ Tape & Reel |

1. Lead Finish NiPdAu

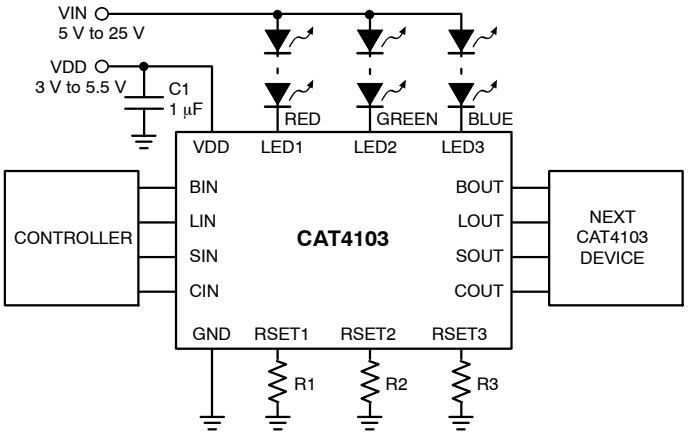



**Figure 1. Typical Application Circuit**

**Table 1. ABSOLUTE MAXIMUM RATINGS**

| Parameter | Rating | Units |
|---|---|---|
| VDD Voltage | 6 | V |
| Input Voltage Range (SIN, BIN, CIN, LIN) | −0.3 V to VDD+0.3 V | V |
| Output voltage range (SOUT, BOUT, COUT, LOUT) | −0.3 V to VDD+0.3 V | V |
| LED1, LED2, LED3 Voltage | 25 | V |
| DC Output Current on LED1 to LED3 | 200 | mA |
| Storage Temperature Range | −55 to +160 | °C |
| Junction Temperature Range | −40 to +150 | °C |
| Lead Soldering Temperature (10 sec.) | 300 | °C |
| ESD Rating: All Pins<br>Human Body Model<br>Machine Model | <br>2000<br>200 | V |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Table 2. RECOMMENDED OPERATING CONDITIONS**

| Parameter | Range | Units |
|---|---|---|
| VDD | 3.0 to 5.5 | V |
| Voltage applied to LED1 to LED3, outputs off | up to 25 | V |
| Voltage applied to LED1 to LED3, outputs on | up to 6 (Note 2) | V |
| Output Current on LED1 to LED3 | 2 to 175 | mA |
| Ambient Temperature Range | −40 to +85 | °C |

2. Keeping the LEDx pin voltage below 6 V in operation is recommended to minimize thermal dissipation in the package.

**Table 3. ELECTRICAL OPERATING CHARACTERISTICS** (Min and Max values are over recommended operating conditions unless specified otherwise. Typical values are at $V_{IN}$ = 5.0 V, $T_{AMB}$ = 25°C.)

| Symbol | Name | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | | |
| $I_{DD1}$ | Supply Current Outputs Off | $V_{LED}$ = 5 V, $R_{SET}$ = 24.9 kΩ | | 2 | 5 | mA |
| $I_{DD2}$ | Supply Current Outputs Off | $V_{LED}$ = 5 V, $R_{SET}$ = 5.23 kΩ | | 4 | 10 | mA |
| $I_{DD3}$ | Supply Current Outputs On | $V_{LED}$ = 0.5 V, $R_{SET}$ = 24.9 kΩ | | 2 | 5 | mA |
| $I_{DD4}$ | Supply Current Outputs On | $V_{LED}$ = 0.5 V, $R_{SET}$ = 5.23 kΩ | | 4 | 10 | mA |
| $I_{LKG}$ | LED Output Leakage | $V_{LED}$ = 5 V, Outputs Off | −1 | | 1 | μA |
| $R_{LIN}$ | LIN Pull−down Resistance | | 140 | 180 | 250 | kΩ |
| $R_{BIN}$ | BIN Pull−up Resistance | | 140 | 180 | 250 | kΩ |
| $V_{IH}$<br>$V_{IL}$ | SIN, BIN, CIN, LIN logic high level<br>SIN, BIN, CIN, LIN logic low level | | 0.7x $V_{DD}$ | | <br>0.3x $V_{DD}$ | V |
| $I_{IL}$ | Logic Input Leakage Current (CIN, SIN) | $V_I$ = $V_{DD}$ or GND | −5 | 0 | 5 | μA |
| $V_{OH}$<br>$V_{OL}$ | xOUT Logic High Output Voltage<br>xOUT Logic Low Output Voltage | $I_{OH}$ = −1 mA<br>$I_{OL}$ = 1 mA | $V_{CC}$ − 0.3 V | | <br>0.3 | V |
| $V_{RSET}$ | RSETx Regulated Voltage | | 1.17 | 1.2 | 1.23 | V |
| $T_{SD}$ | Thermal Shutdown | | | 150 | | °C |
| $T_{HYS}$ | Thermal Hysteresis | | | 20 | | °C |
| $I_{LED}/I_{RSET}$ | RSET to LED Current Gain ratio | 100 mA LED Current | | 400 | | |
| $V_{UVLO}$ | Undervoltage Lockout (UVLO) Threshold | | | 1.8 | | V |

**Table 4. TIMING CHARACTERISTICS** (Min and Max values are over recommended operating conditions unless specified otherwise. Typical values are at $V_{IN}$ = 5.0 V, $T_{AMB}$ = 25°C.)

| Symbol | Name | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **CIN** | | | | | | |
| $f_{cin}$ | CIN Clock Frequency | | | | 25 | MHz |
| $t_{cwh}$ | CIN Pulse Width High | | 18 | | | ns |
| $t_{cwl}$ | CIN Pulse Width Low | | 18 | | | ns |
| **SIN** | | | | | | |
| $t_{ssu}$ | Setup time SIN to CIN | | 4 | | | ns |
| $t_{sh}$ | Hold time SIN to CIN | | 4 | | | ns |
| **LIN** | | | | | | |
| $T_{lwh}$ | LIN Pulse width | | 20 | | | ns |
| $t_{lchd}$ | Hold time LIN to CIN | | 4 | | | ns |
| $t_{lcsu}$ | Setup time LIN to CIN | | 8 | | | ns |
| **LEDn** | | | | | | |
| $t_{ledplon}$ | Turn on Propagation delay LIN | LIN to LED(n) on | | 380 | | ns |
| $t_{ledploff}$ | Turn off Propagation delay LIN | LIN to LED(n) off | | 130 | | ns |
| $t_{ledpbon}$ | Turn on Propagation delay BIN | BIN to LED(n) on | | 380 | | ns |
| $t_{ledpboff}$ | Turn off Propagation delay BIN | BIN to LED(n) off | | 130 | | ns |
| $t_{ledr}$ | LED rise time (10% to 90%) | Pullup resistor = 50 Ω to 3.0 V | | 160 | | ns |
| $t_{ledf}$ | LED fall time (90% to 10%) | Pullup resistor = 50 Ω to 3.0 V | | 140 | | ns |
| **SOUT** | | | | | | |
| $t_{sr}$ | SOUT rise time (10% to 90%) | $C_L$ = 15 pF | | 5 | | ns |
| $t_{sf}$ | SOUT fall time (90% to 10%) | $C_L$ = 15 pF | | 5 | | ns |
| $t_{sdf}$ | Propagation delay time SOUT | CIN falling to SOUT falling | | 6 | 18 | ns |
| $t_{sdr}$ | Propagation delay time SOUT | CIN falling to SOUT rising | | 6 | 18 | ns |
| **COUT** | | | | | | |
| $t_{cr}$ | COUT rise time (10% to 90%) | $C_L$ = 15 pF | | 5 | | ns |
| $t_{cf}$ | COUT fall time (90% to 10%) | $C_L$ = 15 pF | | 5 | | ns |
| $t_{cdf}$ | Propagation delay time COUT | CIN falling to COUT falling | | 4 | 10 | ns |
| $t_{cdr}$ | Propagation delay time COUT | CIN rising to COUT rising | | 4 | 10 | ns |
| **LOUT** | | | | | | |
| $t_{lr}$ | LOUT rise time (10% to 90%) | $C_L$ = 15 pF | | 5 | | ns |
| $t_{lf}$ | LOUT fall time (90% to 10%) | $C_L$ = 15 pF | | 5 | | ns |
| $t_{ldf}$ | Propagation delay time LOUT | LIN falling to LOUT falling | | 4 | 10 | ns |
| $t_{ldr}$ | Propagation delay time LOUT | LIN rising to LOUT rising | | 5 | 10 | ns |
| **BOUT** | | | | | | |
| $t_{br}$ | BOUT rise time (10% to 90%) | $C_L$ = 15 pF | | 5 | | ns |
| $t_{bf}$ | BOUT fall time (90% to 10%) | $C_L$ = 15 pF | | 5 | | ns |
| $t_{bdf}$ | Propagation delay time BOUT | BIN falling to BOUT falling | | 6 | 20 | ns |
| $t_{bdr}$ | Propagation delay time BOUT | BIN rising to BOUT rising | | 8 | 20 | ns |

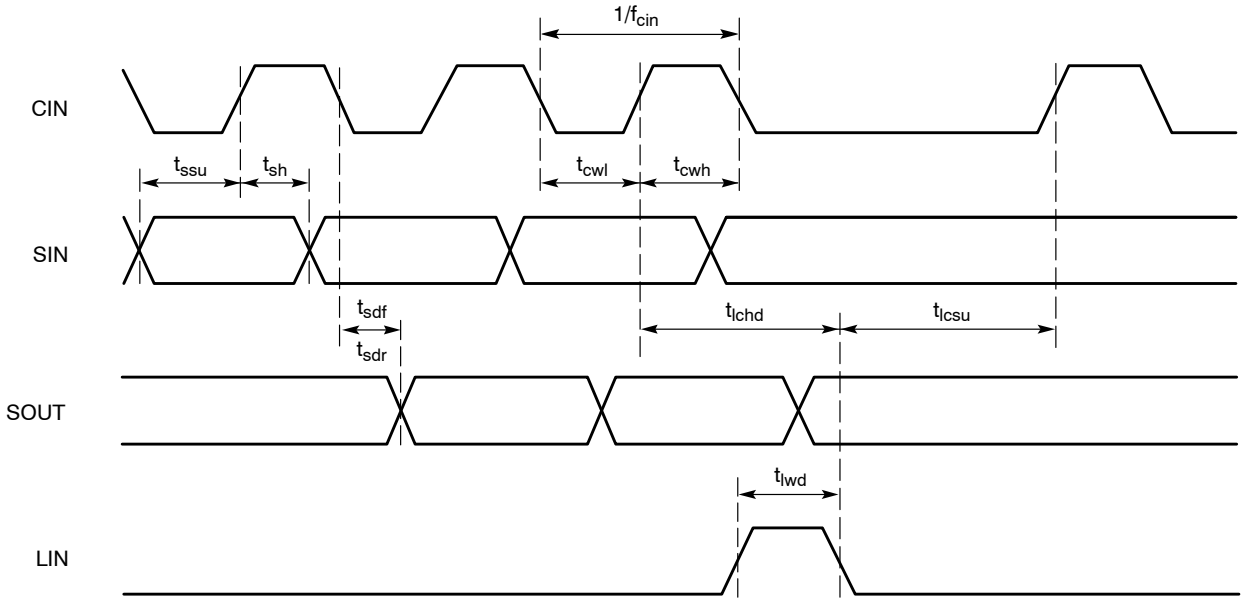



**Figure 2. Timing Diagram A**

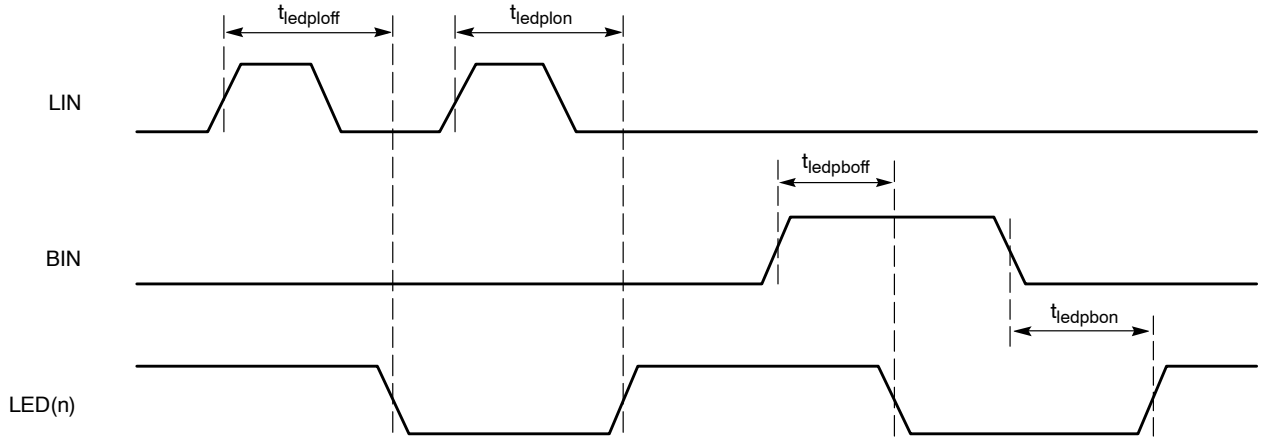



**Figure 3. Timing Diagram B**

## TYPICAL PERFORMANCE CHARACTERISTICS

($V_{IN}$ = 5 V, $V_{DD}$ = 5 V, C1 = 1 μF, $T_{AMB}$ = 25°C unless otherwise specified.)

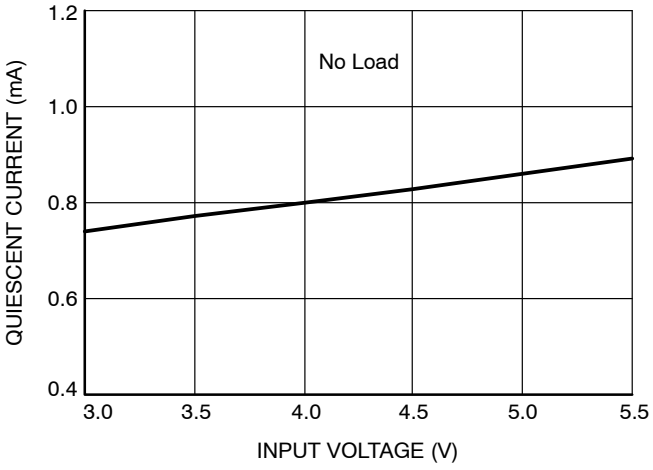



**Figure 4. Quiescent Current vs. Input Voltage ($I_{LED}$ = 0 mA)**

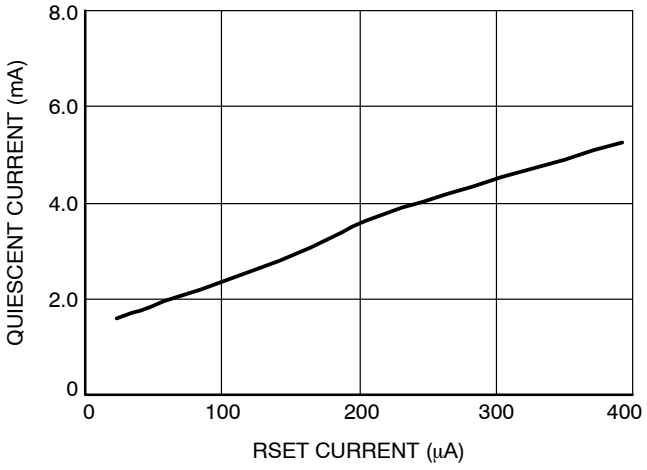



**Figure 5. Quiescent Current vs. RSET Current**

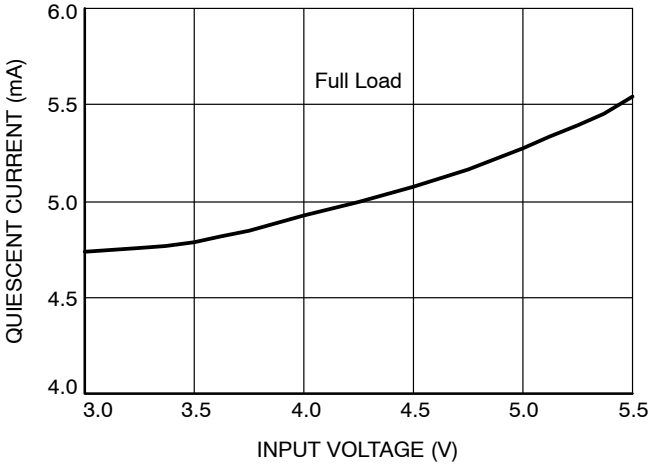



**Figure 6. Quiescent Current vs. Input Voltage ($I_{LED}$ = 175 mA)**

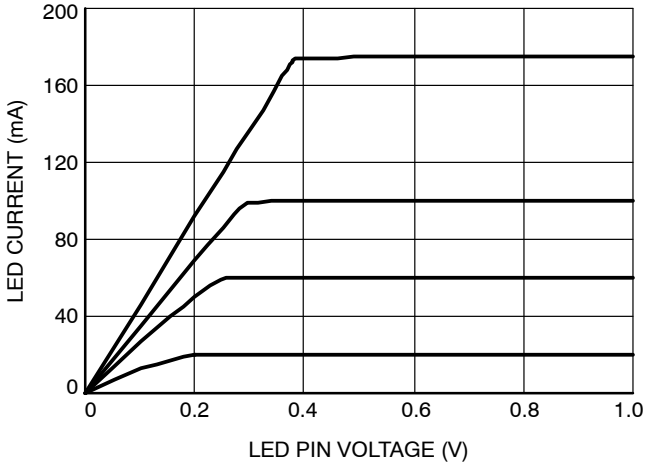



**Figure 7. LED Current vs. LED Pin Voltage**

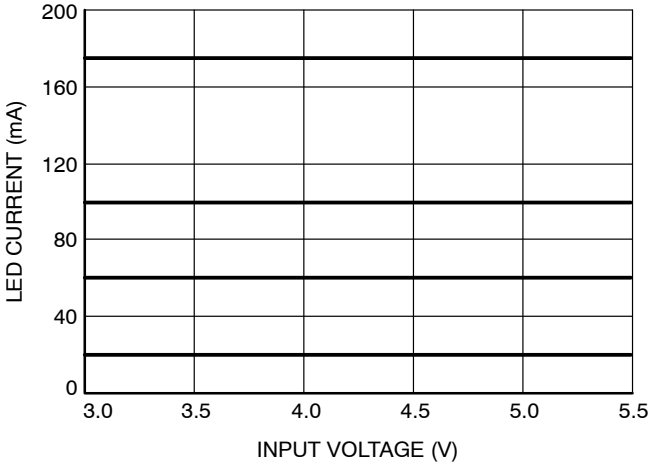



**Figure 8. LED Current Change vs. Input Voltage**

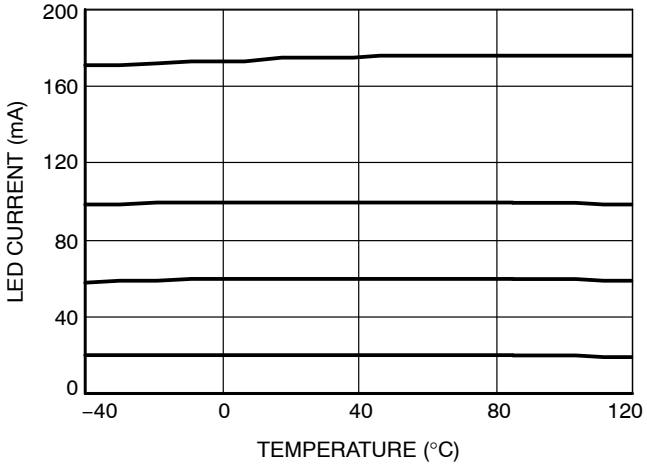



**Figure 9. LED Current Change vs. Temperature**

## TYPICAL PERFORMANCE CHARACTERISTICS

($V_{IN}$ = 5 V, $V_{DD}$ = 5 V, $C_1$ = 1 μF, $T_{AMB}$ = 25°C unless otherwise specified.)

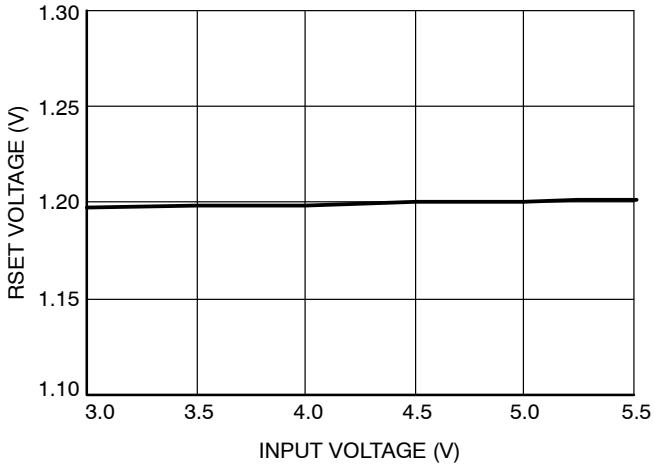



**Figure 10. RSET Pin Voltage vs. Input Voltage**

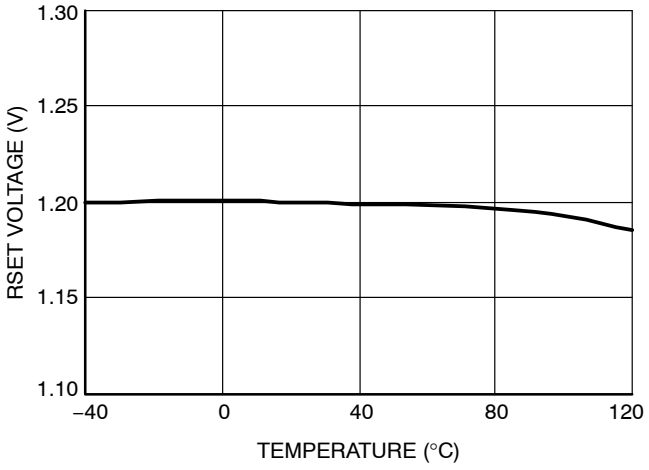



**Figure 11. RSET Pin Voltage vs. Temperature**

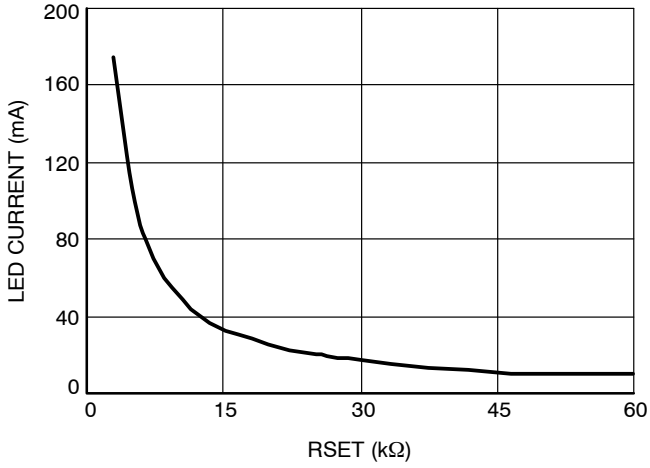



**Figure 12. LED Current vs. RSET Resistor**

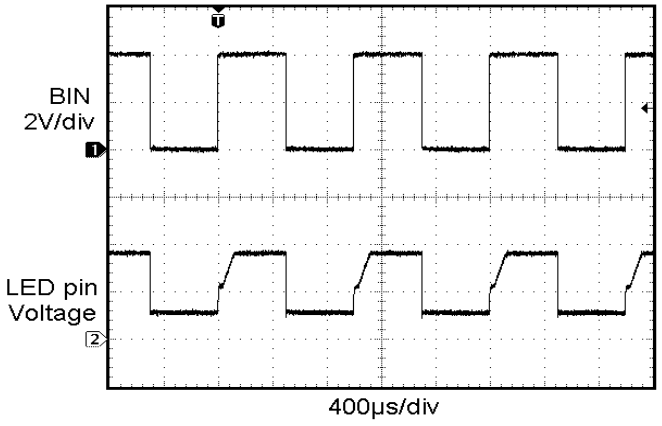



**Figure 13. BIN Transient Response**

**Table 5. PIN DESCRIPTIONS**

| Name | Pin Number | Function |
|---|---|---|
| GND | 1 | Ground Reference |
| BIN | 2 | Blank input pin |
| LIN | 3 | Latch Data input pin |
| SIN | 4 | Serial Data input pin |
| CIN | 5 | Serial Clock input pin |
| RSET3 | 6 | LED current set pin for LED3 |
| RSET2 | 7 | LED current set pin for LED2 |
| RSET1 | 8 | LED current set pin for LED1 |
| LED3 | 9 | LED channel 3 cathode terminal |
| LED2 | 10 | LED channel 2 cathode terminal |
| LED1 | 11 | LED channel 1 cathode terminal |
| COUT | 12 | Serial Clock output pin |
| SOUT | 13 | Serial Data output pin |
| LOUT | 14 | Latch Data output pin |
| BOUT | 15 | Blank output pin |
| VDD | 16 | Device Supply pin |

## Pin Function

**GND** is the ground reference pin for the entire device. This pin must be connected to the ground plane on the PCB.

**BIN** is the blank input used to disable all channels. When low, all LED channels are enabled according to the output latch content. When high, all LED channels are turned off. This pin can be used to turn all the LEDs off while preserving the data in the output latches.

**LIN** is the latch data input. On the rising edge of LIN, data is loaded from the 3−bit serial shift register into the output register latch. On the falling edge of LIN the data is latched in the output register and isolated from the state of the serial shift register.

**SIN** is the serial data input. Data is loaded into the internal register on each rising edge of CIN.

**CIN** is the serial clock input. On each rising CIN edge, data is transferred from SIN to the internal 3−bit serial shift register.

**RSET1 to RSET3** are the LED current set inputs. The current pulled out of these pins will be mirrored in the corresponding LED channel with a gain of 400.

**LED1 to LED3** are the LED current sink inputs. These pins are connected to the bottom cathodes of the LED strings. The current sinks bias the LEDs with a current equal to 400 times the RSET pin current. For the LED sink to operate correctly, the voltage on the LED pin must be above 0.4 V. Each LED channel can withstand and operate with voltages up to 25 V.

**COUT** is a driven output of CIN and can be connected to the next device in the cascade.

**SOUT** is the output of the 3−bit serial shift register. Connect to SIN of the next device in the cascade. SOUT is clocked on the falling edge of CIN.

**LOUT** is a driven output of LIN and can be connected to the next chip in the cascade.

**BOUT** is a driven output of BIN and can be connected to the next chip in the cascade.

**VDD** is the positive supply pin voltage for the entire device. A small 1 μF ceramic capacitor is recommended close to the pin.

## Block Diagram

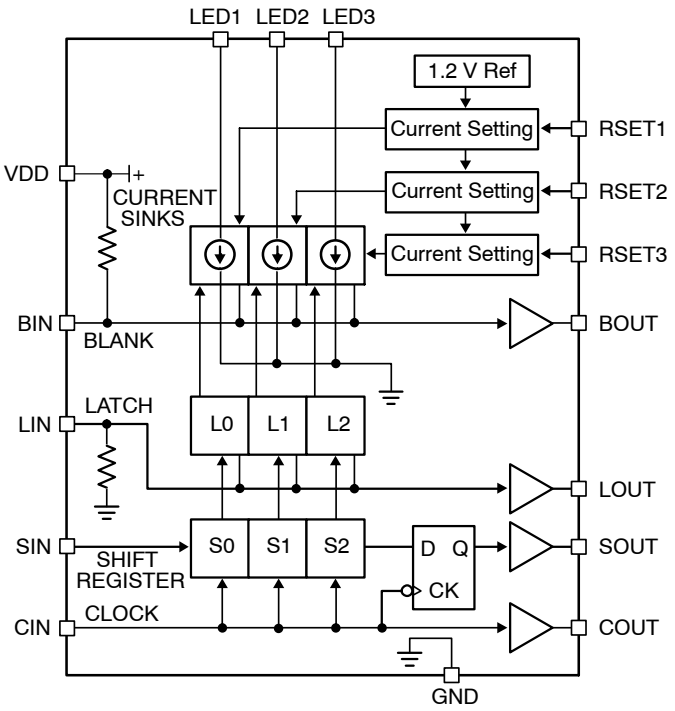



**Figure 14. CAT4103 Functional Block Diagram**

## Basic Operation

The CAT4103 uses 3 independent current sinks to accurately regulate the current in each LED channel to 400 times the current sink from the corresponding RSET pin. Each of the resistors tied to the RSET1, RSET2, RSET3 pins set the current respectively in the LED1, LED2, and LED3 channels. Table 6 shows some standard resistor values for RSET and the corresponding LED current.

**Table 6. RSET RESISTOR SETTINGS**

| LED Current [mA] | RSET [kΩ] |
|---|---|
| 20 | 24.9 |
| 60 | 8.45 |
| 100 | 5.23 |
| 175 | 3.01 |

Tight current regulation for all channels is possible over a wide range of input and LED voltages due to independent current sensing circuitry on each channel. The LED channels have a low dropout of 0.4 V or less for all current ranges and supply voltages. This helps improve heat dissipation and efficiency over other competing solutions.

Upon power−up, an under−voltage lockout circuit clears all latches and shift registers and sets all outputs to off. Once the VDD supply voltage is greater than the under−voltage lockout threshold, the device can be programmed.

Pull−up and pull−down resistors are internally provided to set the state of the BIN and LIN pins to low current off state when not externally driven.

A high−speed 4−wire interface is provided to program the state of each LED channel ON or OFF.

The 4−wire interface contains a 3−bit serial−to−parallel shift register (S0−S2) and a 3−bit latch (L0−L2). The shift register operates on a first−in first−out (FIFO) basis. The most significant bit S2 corresponds to the first data entered in from SIN. Programming the serial−to−parallel register is accomplished via SIN and CIN input pins. On each rising edge of the CIN signal the data from SIN is moved through the shift register serially. Data is also moved out of SOUT to the next device if programming more than one device on the same interface.

On the rising edge of LIN, the data content of the serial to parallel shift register is reflected in the latches. On the falling edge of LIN, the state of the serial−to−parallel register at that particular time is saved in the latches and does not change regardless of the content of the serial to parallel register.

BIN is used to disable all LEDs off at one time while still maintaining the data contents of the latch register. BIN is an active low input pin. When low the outputs reflect the data in the latches. When high the outputs are all high impedance (LEDs off).

All 4−wire inputs have a corresponding output driver for cascaded systems (SOUT, COUT, LOUT, BOUT). These output buffers allow many CAT4103 drivers to be cascaded without signal and timing degradation due to long wire interconnections.

## Application Information

### Cascading Multiple Devices

The CAT4103 is designed to be cascaded for driving multiple RGD LEDs. Figure 16 shows three CAT4103 drivers cascaded together. The programming data from the controller travels serially through each device. Figure 15 shows a programming example turning on the following LED channels: BLUE3, GREEN2 and RED1. The programming waveforms are measured from the controller to the inputs of the first CAT4103.

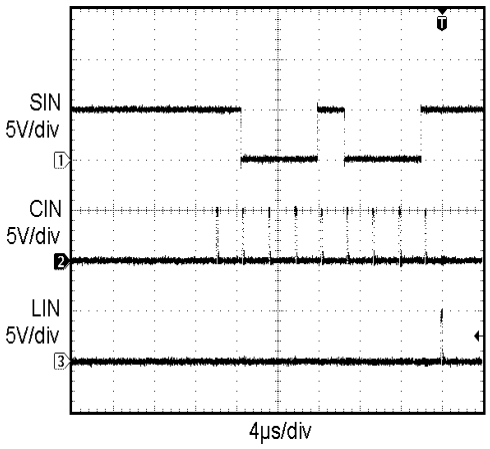



**Figure 15. Programming Example**

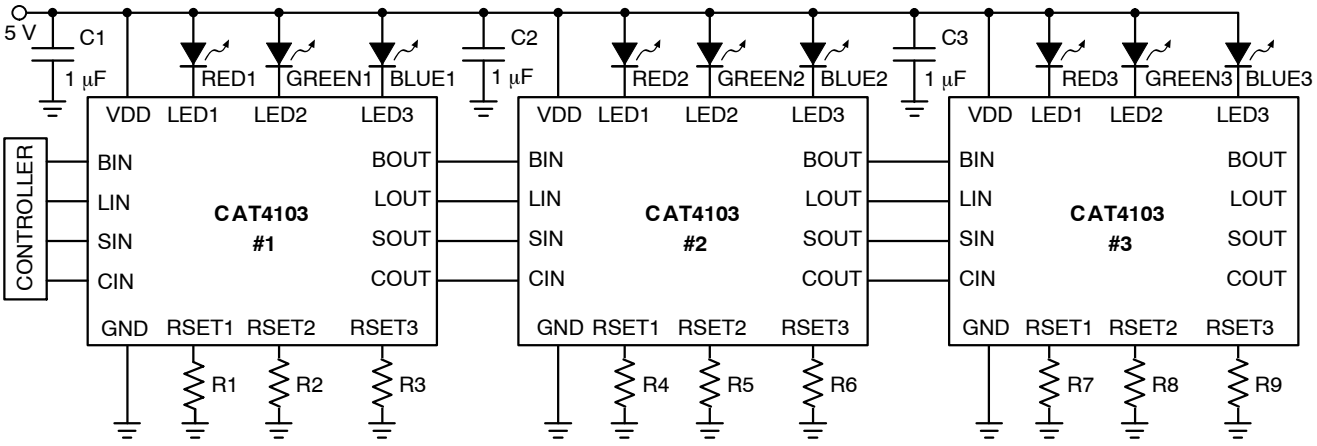



**Figure 16. Three Cascaded CAT4103 Devices**

### Power Dissipation

The power dissipation ($P_D$) of the CAT4103 can be calculated as follows:

$$P_D = (V_{DD} \times I_{DD}) + \Sigma(V_{LEDN} \times I_{LEDN})$$

where $V_{LEDN}$ is the voltage at the LED pin, and $I_{LEDN}$ is the associated LED current. Combinations of high $V_{LED}$ voltage or high ambient temperature can cause the CAT4103 to enter thermal shutdown. In applications where $V_{LEDN}$ is high, a resistor can be inserted in series with the LED string to lower $P_D$.

Thermal dissipation of the junction heat consists primarily of two paths in series. The first path is the junction to the case ($\theta_{JC}$) thermal resistance which is defined by the package style, and the second path is the case to ambient ($\theta_{CA}$) thermal resistance, which is dependent on board layout. The overall junction to ambient ($\theta_{JA}$) thermal resistance is equal to:

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

For a given package style and board layout, the operating junction temperature $T_J$ is a function of the power dissipation $P_D$, and the ambient temperature, resulting in the following equation:

$$T_J = T_{AMB} + P_D\,(\theta_{JC} + \theta_{CA}) = T_{AMB} + P_D\,\theta_{JA}$$

When mounted on a double−sided printed circuit board with two square inches of copper allocated for “heat spreading”, the resulting $\theta_{JA}$ is about 74°C/W.

For example, at 60°C ambient temperature, the maximum power dissipation is calculated as follow:

$$P_{Dmax} = \frac{(T_{Jmax} - T_{AMB})}{\theta_{JA}} = \frac{(150 - 60)}{74} = 1.2\ W$$

### Recommended Layout

Bypass capacitor C1 should be placed as close to the IC as possible. RSET resistors should be directly connected to the GND pin of the device. For better thermal dissipation, multiple via can be used to connect the GND pad to a large ground plane. It is also recommended to use large pads and traces on the PCB wherever possible to spread out the heat. The LEDs for this layout are driven from a separate supply (VLED+), but they can also be driven from the same supply connected to VDD.

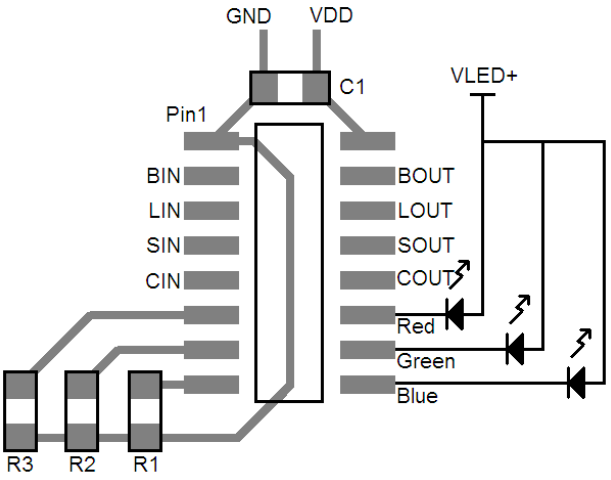
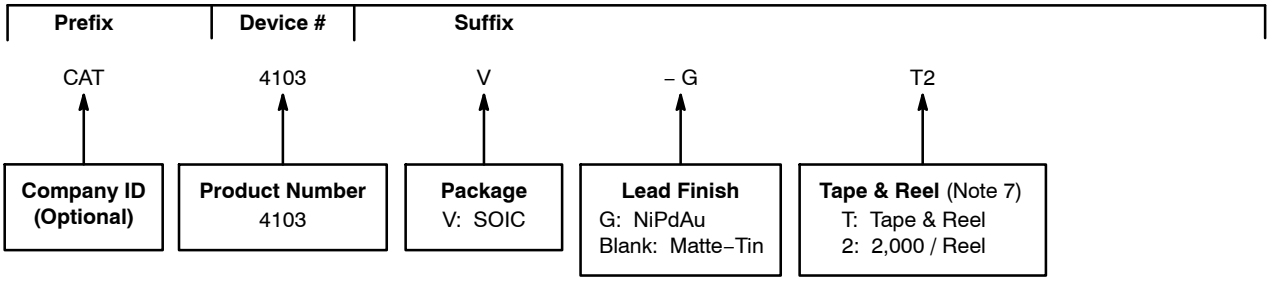



**Figure 17. Recommended Layout**

**Notes:**

(1) All dimensions are in millimeters. Angles in degre
(2) Complies with JEDEC MS-0

## Example of Ordering Information (Note 5)




3. All packages are RoHS−compliant (Lead−free, Halogen−free).
4. The standard plated finish is NiPdAu.
5. The device used in the above example is a CAT4103V−GT2 (SOIC, NiPdAu, Tape & Reel, 2,000/Reel).
6. For additional temperature options, please contact your nearest ON Semiconductor Sales office.
7. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**SOIC−16, 150 mils**
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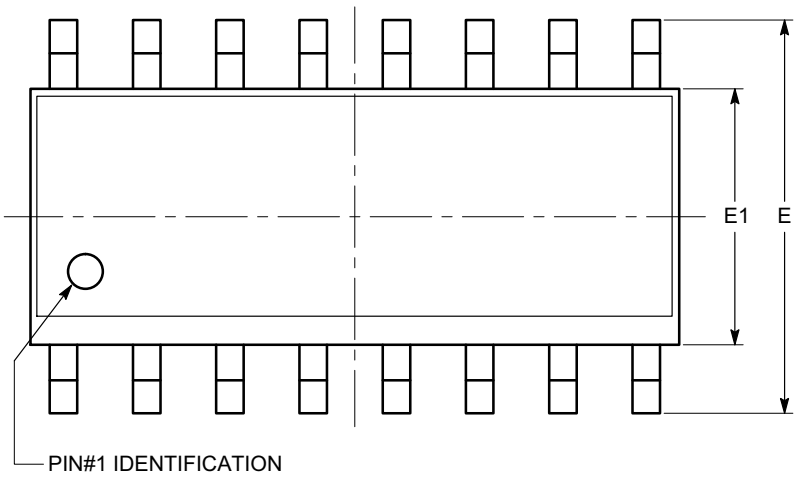
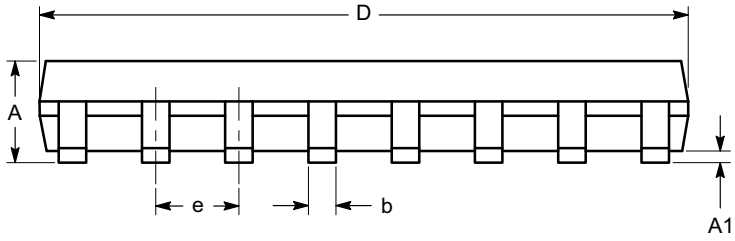
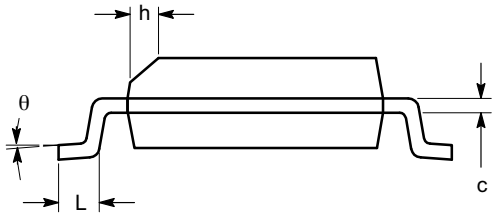



**TOP VIEW**

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 1.35 | | 1.75 |
| A1 | 0.10 | | 0.25 |
| b | 0.33 | | 0.51 |
| c | 0.19 | | 0.25 |
| D | 9.80 | 9.90 | 10.00 |
| E | 5.80 | 6.00 | 6.20 |
| E1 | 3.80 | 3.90 | 4.00 |
| e | | 1.27 BSC | |
| h | 0.25 | | 0.50 |
| L | 0.40 | | 1.27 |
| θ | 0º | | 8º |




**SIDE VIEW**




**END VIEW**

**Notes:**
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

| | | |
|---|---|---|
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| **DESCRIPTION:** | **SOIC−16, 150 MILS** | **PAGE 1 OF 1** |

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