DS33Z44DK
Ethernet Transport Design Kit

www.maxim-ic.com

GENERAL DESCRIPTION

The DS33Z44 design kit is an easy-to-use evaluation board for the DS33Z44 Ethernet transport-over-serial link device. The DS33Z44DK is intended to be used with a resource card for the serial link. The serial link resource cards are complete with transceivers, transformers, and network connections. Dallas' ChipView software is provided with the design kit, giving point-and-click access to configuration and status registers from a Windows®-based PC. On-board LEDs indicate receive loss-of-signal, queue overflow, Ethernet link, Tx/Rx, and interrupt status.

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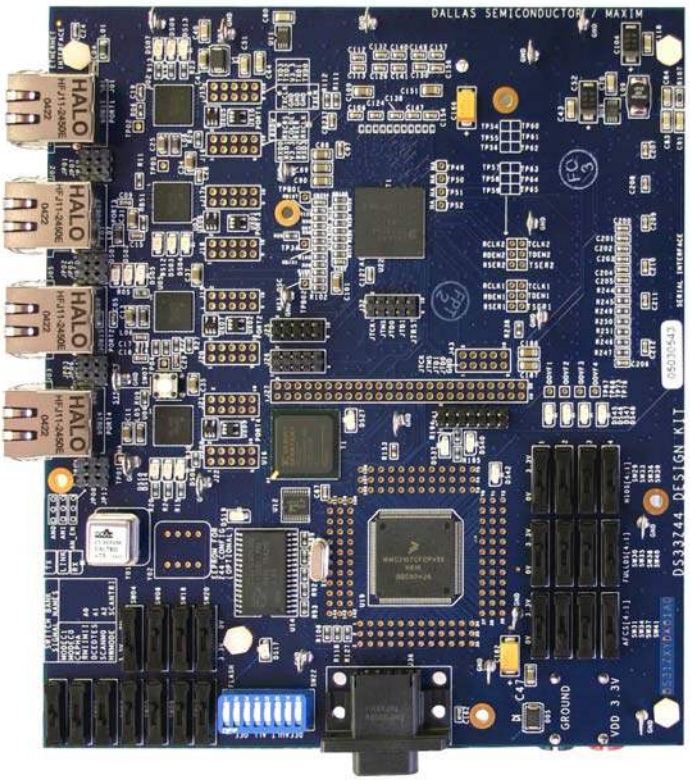
ORDERING INFORMATION

PART	DESCRIPTION
DS33Z44DK	DS33Z44 demo card, T3/E3, T1/E1 transceiver resource card included

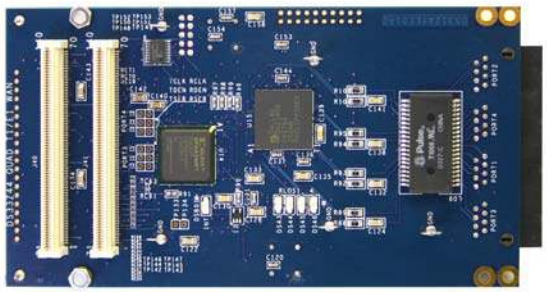


FEATURES

- **Demonstrates Key Functions of DS33Z44 Ethernet Transport Chipset**
- **Includes Two Resource Cards: One with DS21458 T1/E1 SCT and one with DS3174 T3/E3 SCT, Transformers, BNC and RJ48 Network Connectors, and Termination**
- **Provides Support for Hardware and Software Modes**
- **On-Board MMC2107 Processor and ChipView Software Provide Point-and-Click Access to the DS33Z44 Register Set**
- **All DS33Z44 Interface Pins are Easily Accessible for External Data Source/Sink**
- **LEDs for Loss-of-Signal, Queue Overflow, Ethernet Link, Tx/Rx, and Interrupt Status**
- **Easy-to-Read Silkscreen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDs**

DESIGN KIT CONTENTS

- DS33Z44DK Main Board
- Quad-Port Serial Card with DS21458 T1/E1 SCT
- Quad-Port Serial Card with DS3174 T3/E3 SCT
- CD_ROM
  - ChipView Software and Manual
  - DS33Z44DK Data Sheet
  - Configuration Files



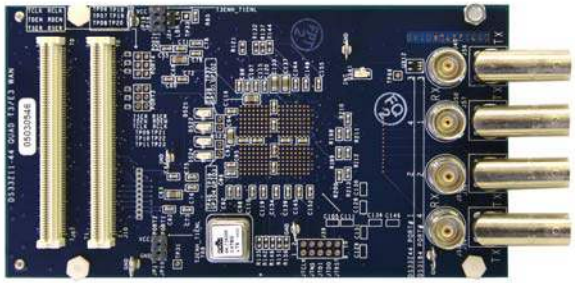


TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

COMPONENT LIST

Table 1 shows the component list for the DS33Z44 and DS33Z11/DS33Z41 design kits and resource cards. This BOM contains the part listing for five boards. These boards are the DS33Z11DK, DS33Z44DK, DS21458RC, DS3174RC, and DS2155-DS21348-DS3170RC. Each reference designator is only used once. For example, U18 only appears on the DS33Z11DK and is not used on any of the other boards. See Table 2.

Table 1. Component List (Decoupling Caps Not Shown)

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
U18	1	ELITE 10/100 ETHERNET TRANSPORT OVER SERIAL LINK 14X14 CSBGA 169 PIN	Dallas Semiconductor	DS33Z11
U20	1	3.3V T1.E1.J1 QUAD TRANSCEIVER 0-70C 256P BGA	Dallas Semiconductor	DS21458
U22	1	QUAD 10/100 ETHERNET EXTENSION TO WAN 17X17 PBGA 256 PIN	Dallas Semiconductor	DS33Z44
U23	1	DS3/E3 SCT, 11X11 CSBGA, 100 PIN	Dallas Semiconductor	DS3170
U24	1	T1/E1/J1 XCVR 100P QFP 0-70C	Dallas Semiconductor	DS2156L
U25	1	3.3V LIU	Dallas Semiconductor	DS21348
UB08	1	QUAD TRIPLE DUAL SINGLE ATM PACKET PHYS FOR DS3 E3 STS1 0-70C 400P BGA	Dallas Semiconductor	DS3184
U01, U09	2	SOIC 8PIN STEP-UP DC-DC CONVERTER 0.5A LIMIT	Maxim	MAX1675EUA
U07, U11	2	8-Pin µMAX/SOIC 1.8V or Adj	Maxim	MAX1792EUA18
U13, UB01	2	MICROPROCESSOR VOLTAGE MONITOR, 2.93V RESET, 4PIN SOT143	Maxim	MAX811SEUS-T
U21, UB07	2	Dual RS-232 transceivers with 3.3V/5V internal capacitors	MAXIM	NA
U31, UB06, UB11	3	8-Pin µMAX/SOIC 2.5V or Adj	Maxim	MAX1792EUA25
C11, C13, C16, C25, C27, C31–C35, C37, C41, C47, CB10, CB63, CB114, CB128, CB164, CB496	19	1206 CERAM 10uF 10V 20%	Panasonic	ECJ-3YB1A106M
CB390, CB391, CB395, CB396	4	1206 CERAM 0.1uF 25V 10%	Panasonic	ECJ-3VB1E104K
D01–D03, D05, DB03–DB05	7	SCHOTTKY DIODE, 1 AMP 40 VOLT	International Rectifier	10BQ040
DS01, DS07, DS10–DS12, DS17, DS20	7	LED, AMBER, SMD	Panasonic	LN1451C
DS02, DS03, DS09, DS14, DS15	5	L_LED, GREEN, SMD	Panasonic	LN1351C
DS04–DS06, DS08, DS13, DS16, DS18, DS27, DS28, DS35, DS37, DS38, DS40	13	LED, RED, SMD	Panasonic	LN1251C
DS19, DS43	2	LED, GREEN, SMD	Panasonic	LN1351C
DS21–DS26, DS30, DS32–DS34, DS36, DS39, DS41, DS42, DS44–DS48	19	L_LED, RED, SMD	Panasonic	LN1251C
GND_TP01–GND_TP07, GND_TP09—GND_TP44, GND_TP46–GND_TP68, GND_TPB01–GND_TPB10	76	STANDARD GROUND CLIP	KEYSTONE	4954
H1–H8, H17–H19	8	KIT, 4-40 HARDWARE, .50 NYLON STANDOFF AND NYLON HEX-NUT	NA	Lab Stock

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
H9–H16	16	KIT, 4-40 HARDWARE, 1.12 NYLON STANDOFF AND NYLON HEX-NUT (1.12 STANDOFF PN = 4807K-ND)	NA	Lab Stock
J01–J05	5	CONNECTOR, FASTJACK SINGLE, 8 PIN	Halo Electronics	HFJ11-2450E
J06, J41	2	100 MIL 2*7 POS JUMPER	NA	Lab Stock
J07–J12	6	RECEPTACLE, SMD, 140 PIN, .8MM, 2 ROW VERTICAL	AMP	5-179010-6
J13–J22	10	L_TERMINAL STRIP, 10 PIN, DUAL ROW, VERT DO NOT POPLUATE	NA	Lab Stock
J23, J29, J32, J38, J39, J43, J44, J47, JB07	9	L_TERMINAL STRIP, SHROUDED, 10 PIN, DUAL ROW, VERT	3M Electronics	2510-6002UB
J24, J30, J31, J33	4	100 MIL 2 POS JUMPER	NA	Lab Stock
J25, J26, J45, J46	4	TERMINAL STRIP, 10 PIN, DUAL ROW, VERT	NA	Lab Stock
J27, J42	2	CONN 50 PIN, 2 ROW, POSTS VERT, MOTHERBOARD FOOTPRINT	SAMTEC	TSW-125-07-T-D
J28, J36	2	L_CONN, DB9 RA, LONG CASE	AMP	747459-1
J48, J54, JB01	3	SOCKET, BANANA PLUG, HORIZONTAL, BLACK	Mouser Electronics	164-6218
J49–J52	4	CONNECTOR BNC 75 OHM VERTICAL 5PIN	Cambridge	CP-BNCPC-004
J53, JB02, JB08	3	SOCKET, BANANA PLUG, HORIZONTAL, RED	Mouser Electronics	164-6219
J55, JB11	2	L_RJ48 8 PIN SINGLE PORT CONNECTOR	MOLEX	15-43-8588
J56–J59, J61, J63	6	CONNECTOR BNC 75 OHM RA 5PIN	Trompetor	UCBJR220
J60, J62, J64, J65	4	CONNECTOR BNC RA 5PIN	Trompetor	UCBJR220
JB05, JB06, JB09, JB10, JB13, JB14	6	PLUG, SMD, 140 PIN, .8MM, 2 ROW VERTICAL	AMP	179031-6
JB12	1	RA RJ45 8PIN 4PORT JACK	MOL	43223-8140
JP01–JP19	19	100 MIL 3 POS JUMPER	NA	NA
L01, L03–L08, LB01, LB02	9	FERRITE 3A 100 OHM AT 100 MHZ 1206 SMD	Steward	HI1206N101R-00
L02, L09	2	INDUCTOR 22.0uH 2PIN SMT 20%	Coiltronics	UP1B-220
L10	1	XFMR 1-2CT XMIT, 1-1CT RCV, 40P WIDE SOIC	Pulse	T1068
R01, R02, RB10, RB11, RB18, RB19, RB22, RB23, RB26, RB27	10	RES 0603 54.9 Ohm 1/16W 1%	Panasonic	ERJ-3EKF54R9V
R03, R04, RB12, RB13, RB20, RB21, RB24, RB25, RB28, RB29	10	RES 0603 49.9 Ohm 1/16W 1%	Panasonic	ERJ-3EKF49R9V
R05, R06, R08, R09, R11	5	RES 0603 10.0K Ohm 1/16W 1% - Must be 1% tolerance	Panasonic	ERJ-3EKF1002V
R07, R12, R16, R79, R160, R244, R248, R250, R251, R254, R255, RB126, RB143, RB147, RB150, RB157	16	RES 0603 1.0K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ102V
R10, R107	2	RES 1206 5.6 Ohm 1/8W 5%	Panasonic	ERJ-8GEYJ5R6V
R132, R137, R142, R144, R156, RB194, RB208, RB227	8	L_RES 0603 0 Ohm 1/16W 1%	AVX	CJ10-000F

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
R13–R15, R18–R20, R22, R23, R29, R30, RB01, RB03, RB07, RB09, RB15–RB17, RB30–RB32, RB34–RB38, RB41, RB44, RB47, RB48, RB50–RB52, B55, RB60, RB62, RB72, RB73, RB75, RB80, RB82	40	RES 0603 5.1K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ512V
R17, R21, R25–R28, R31, R55, R57–R59, R71, R74–R76, R83, R96–R102, R105, R106, R109, R111, R112, R115–R117, R120, R122–R126, R128, R133, R134, R140, R141, RB61, RB96, RB97, RB99, RB100, RB102–RB110, RB112, RB114–RB119, RB121, RB123–RB125, RB127, RB128, RB130, RB131, RB133, RB135–RB138, RB145, RB148, RB149, RB160, RB161, RB164, RB165, RB167–RB171, RB173–RB181, RB184, RB187, RB311, RB320, RB335, RB339, RB359	104	RES 0603 30 Ohm 1/16W	Panasonic	ERJ-3GEYJ300V
R171, R172, R174, R175, R190, R191, R240, R241	8	L_RES 0805 0.0 Ohm 1/10W 5%	Panasonic	ERJ-6GEY0R00V
R198–R200, R210–R213, RB306, RB325, RB326	10	RES 0603 332 Ohm 1/16W 1%	Panasonic	ERJ-3EKF3320V
R201–R208, RB321–RB324, RB327–RB330	16	RES 1206 0 Ohm 1/8W 5%	Panasonic	ERJ-8GEYJ0R00V
R239, RB349	2	RES 0805 51.1 Ohm 1/10W 1%	Panasonic	ERJ-6ENF51R1V
R24, R114, R197, RB14, RB33, RB40, RB42, RB43, RB49, RB53, RB54, RB57–RB59, RB71, RB77, RB78, RB152–RB156, RB221, RB234, RB251, RB284, RB304, RB331, RB332, RB342, RB344, RB350, RB354, RB360	34	L_RES 0603 330 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ331V
R242, R243, RB144, RB166, RB355–RB358, RB368–RB371	12	RES 0603 51 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ510V
R32, R70, R78, R161, R176, R194, R195, R237, R238, RB129, RB134, RB146, RB193	13	RES 0603 330 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ331V
R33–R54, R60–R69, R72, R73, R131, R136, R143, R147, R150, R154, R158, R163, R166, R169, R173, R178–R189, R215–R228, RB89–RB95, RB101, RB188–RB191, RB196–RB199, RB202–RB205, RB210–RB213, RB216–RB219, RB223–RB226, RB230–RB233, RB239–RB242, RB244–RB249, RB252–RB260, RB265–RB268, RB270-RB282, RB289–RB297	152	RES 0402 30 Ohm 1/16W 5%	Panasonic	ERJ-2GEJ300X
R56, R90	2	RES 0603 1.0M Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ105V
R77, RB159	2	L_RES 1206 0 Ohm 1/8W 5%	Panasonic	ERJ-8GEYJ0R00V
R80, R81, R84, R87, R89, R91–R93, R95, R108, R110, R118, R127, R152, R153, R196, R209, R214, R229–R236, RB200, RB237, RB238, RB263, RB264, RB286, RB287, RB300, RB301, RB333, RB364	37	RES 0603 10K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ103V

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
R85, R88, R94, R104, R113, RB02, RB04–RB06, RB08, RB39, RB45, RB46, RB56, RB63–RB70, RB76, RB83, RB98, RB183, RB185, RB192, RB209, RB228, RB302, RB303, RB305, RB338, RB340, RB341, RB346–RB348, RB351–RB353, RB361–RB363, RB365–RB367	48	RES 0603 2.0K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ202V
R86, R103, R119, R121, R129, R130, R135, R138, R139, R145, R146, R149, R151, R157, R162, R164, R167, R168, R170, R177, R192, R193, R245-R247, R249, R252, R253, R256, R257, RB74, RB79, RB132, RB139-RB141, RB151, RB162, RB163, RB172, RB182, RB186, RB206, RB207, RB214, RB215, RB220, RB222, RB229, RB235, RB236, RB243, RB250, RB261, RB262, RB269, RB308–RB310, RB343, RB345	61	L_RES 0603 10K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ103V
RB201, RB285	2	RES 0805 330 Ohm 1/10W 5%	Panasonic	ERJ-6GEYJ331V
RB283	1	RES 0603 10K Ohm 1/10W 5% - SEE SPECIAL INSTRUCTIONS	Panasonic	603_ERJ-3GEYJ103V
RB298, RB299, RB312–RB319, RB336, RB337	12	RES 0805 61.9 Ohm 1/10W 1%	Panasonic	ERJ-6ENF61R9V
RB81, RB84–RB88, RB111, RB113, RB120, RB122	10	RES 0603 DO NOT POPULATE	NA	NA
SW01–SW05, SW08–SW21, SW24–SW26, SW29–SW31, SW33–SW44	37	L_SWITCH, SP3T SLIDE, 4PIN TH	Tyco	3-1437575-3
SW06, SW22	2	L_SWITH 8POS 16PIN DIP LOW PROFILE	AMP	435668-7
SW07, SW23	2	SWITCH MOM 4PIN SINGLE POLE	Panasonic	EVQPAE04M
SW27, SW28, SW32	3	L_DIPSWITCH, 10 POS	AMP	435668-9
T01, T03	2	XFMR 16P SMT	Pulse	TX1099
T02, TB01	2	XFMR, OCTAL T3/E3, 1 TO 2, SMT 32 PIN	Pulse	T3049
TP01–TP78, TPB01, TPB02	80	TESTPOINT, 1 PLATED HOLE, DO NOT STUFF	NA	NA
U02–U06	5	IC, DsPHYTER11-SINGLE 10/100 ETHERNET TRANSCEIVER, 65 PIN LLP	National Semiconductor	DP83847ALQA56A
U08, U12, U29	3	1MBit Flash based config mem	Avnet	XCF01SV020C
U10	1	XILINX SPARTAN xc200 2.5V FPGA,256 PIN BGA	Xilinx	XC2S200-5FG256C
U14, U26, U30, UB05	4	CYPRESS SRAM, LAB STOCK	NA	NA
U15, U19	2	mmc2107 processor	Motorola	MMC2107
U16, U27	2	XILINX SPARTAN 2.5V FPGA,256 PIN BGA	Xilinx	XC2S50-5FG256C
U17, U28, U32	3	10 pin res pack, 10K ohm	NA	NA
UB02, UB03, UB04	3	100 PIN CPLD	XILINX	XC95144XL-10TQ100C
UB09, UB10	2	SYNCHRONOUS DRAM, 1MEGX32X4 BANKS, TSOP 86 PIN	Micron	MT48LC4M32B2TG-7

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
UX01–UX12, UXB02–UXB04, UXB06–UXB08	18	HIGH SPEED BUFFER	Fairchild	NC7SZ86
UXB01, UXB05	2	HIGH SPEED INVERTER	Fairchild	NC7SZ86
X01, X02	2	XTAL LOW PROFILE 8.0MHZ	ECL	EC1-8.000M
Y01, Y09	2	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 25.000 MHZ, Low Jitter required for PHY	SaRonix	NTH089AA3-25.000
Y02, Y13	2	SPI SERIAL EEPROM 16K 8 PIN DIP 2.7V NEEDS SOCKET	Atmel	AT25160A-10PI-2.7
Y03	1	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 2.048 MHZ	SaRonix	NTH039A3-2.0480
Y05, Y06	2	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 100.000 MHZ	SaRonix	NTH089A3-100.0000
Y07	1	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 44.736 MHZ	SaRonix	NTH089AA3-44.736
Y08	1	OSCILLATOR, CRYSTAL CLOCK, 5.0V - 44.736 MHZ	SaRonix	NTH089AA-44.736
YB02	1	L_OSCILLATOR, CRYSTAL CLOCK, 3.3V - 2.048 MHZ	SaRonix	NTH039A3-2.0480

Figure 1. System Floorplan

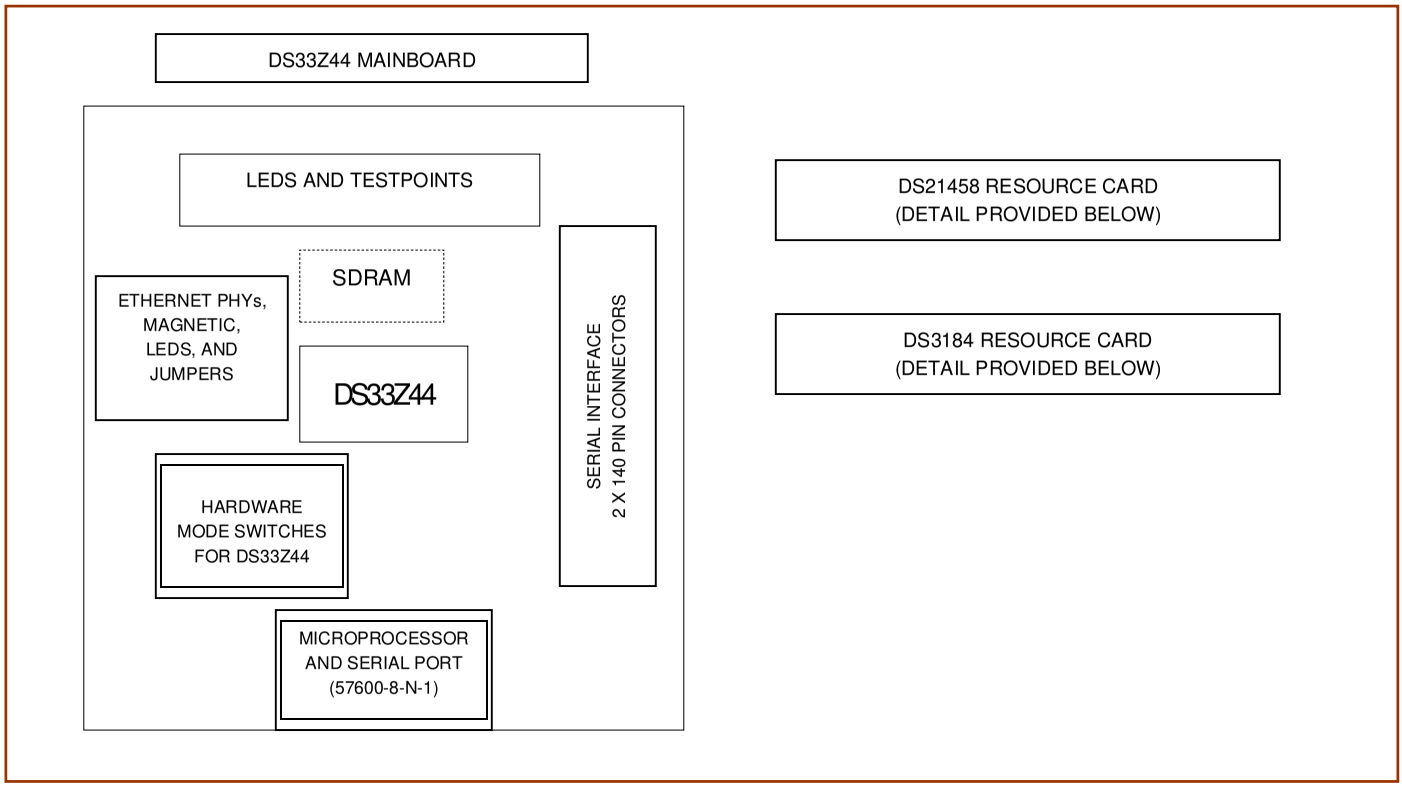
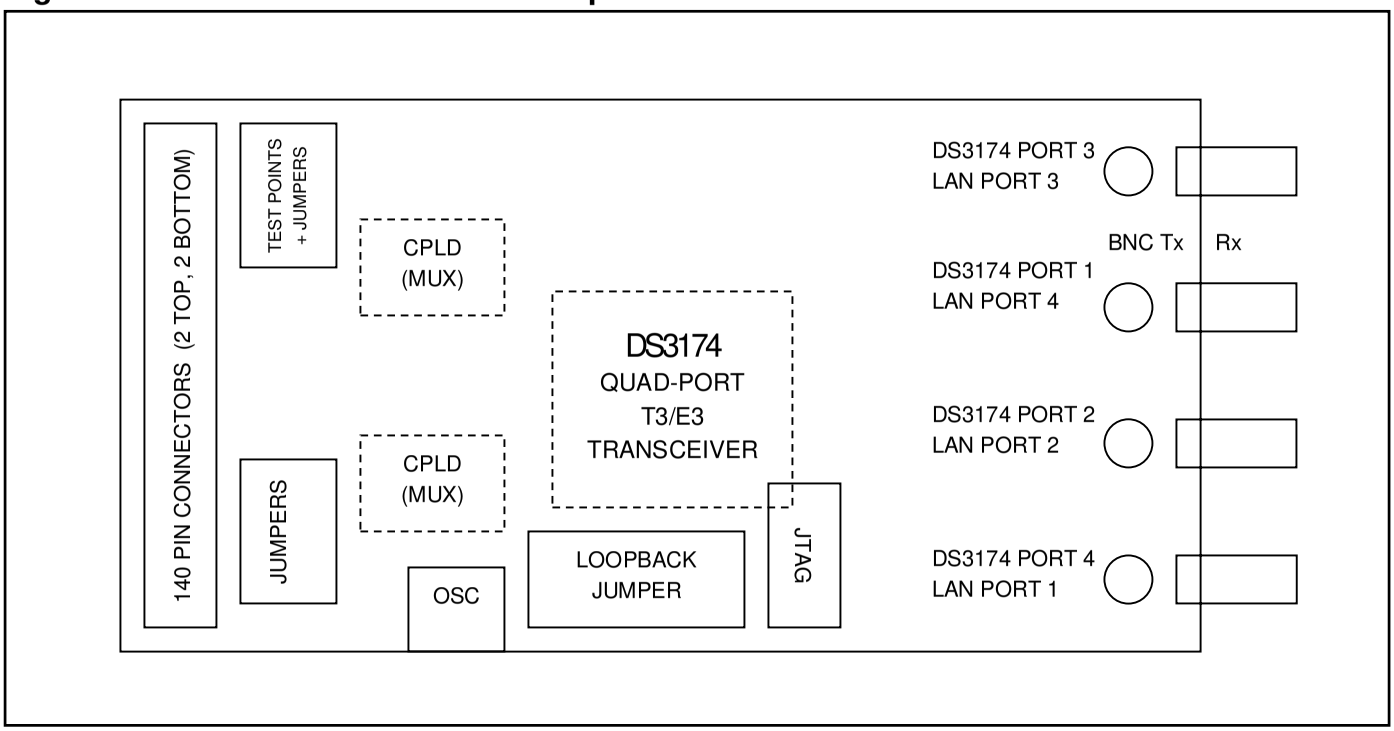


Figure 2. DS3174 Resource Card Floorplan



The DS3174 quad T3/E3 PC board floorplan is shown in Figure 2. Jumpers JP16, JP17, JP18, and JP19 are 3-pin jumpers used to tri-state/enable T3/E3 ports. With the board oriented as shown in Figure 2, the top 2 pins of each jumper would be connected to enable T3/E3 traffic.

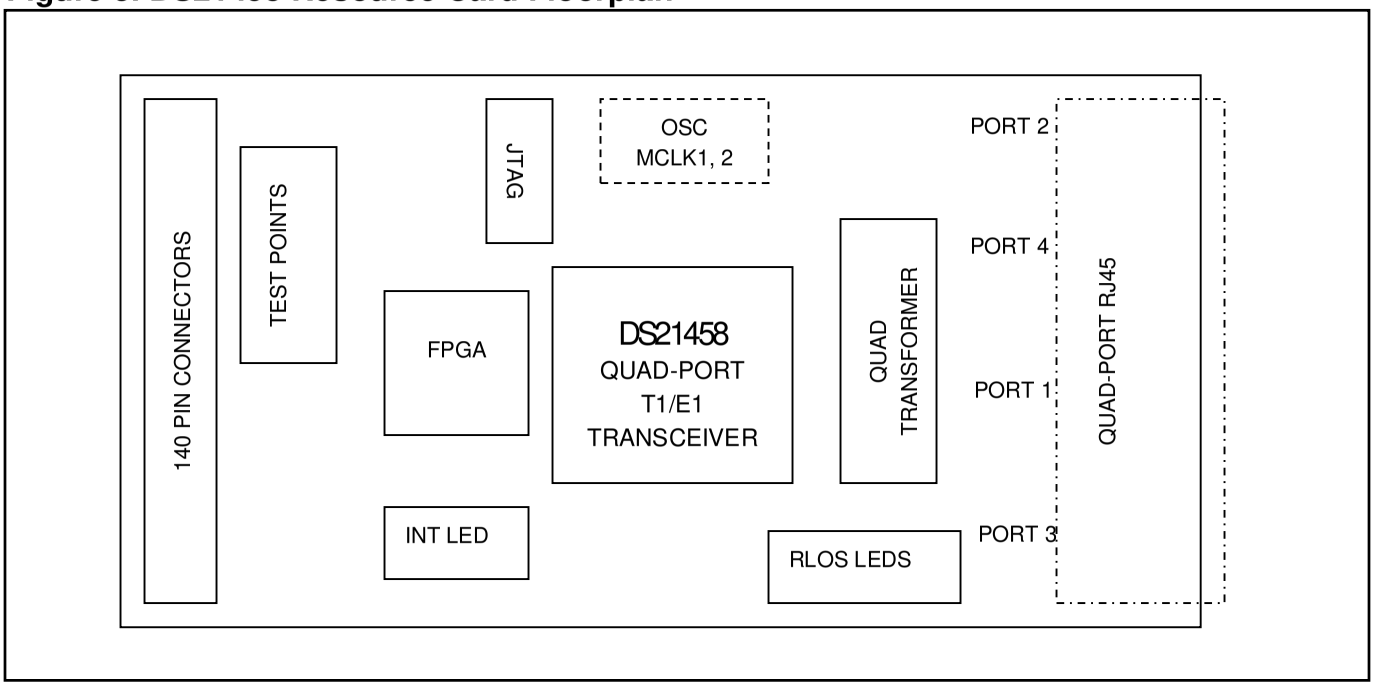
A 2-pin jumper, JP24, has been added to allow loopback. When installed, the board is in loopback at the CPLD; all traffic sent by the DS33Z44 is then sent back to the Z44. Traffic sent by the DS3174 is ignored in CPLD loopback mode.

The quad T3/E3 board is intended to be connected to the DS33Z11 or DS33Z44 motherboards. The quad T3/E3 board can be used with the quad T1/E1 board. When used in this manner, the quad T1/E1 board is stacked underneath the quad T3/E3 board. Jumpers on the T3/E3 board are then used to tri-state or enable individual ports on either board.

Figure 3 shows the DS21458 quad T1/E1 PC board floorplan. The current configuration is to populate oscillators for MCLK1 with a 2.048MHz oscillator. Testpoints for port 3 and port 4 are provided on the WAN card, and testpoints for ports 1 and 2 are provided on the motherboard.

The quad T1/E1 board can be used with the quad T3/E3 board. When used in this manner, the quad T1/E1 board is stacked underneath the quad T3/E3 board. Jumpers on the T3/E3 board are then used to tri-state or enable individual ports on either board.

Figure 3. DS21458 Resource Card Floorplan



PC BOARD ERRATA

- Silk screen for the serial resource card has V_{CC} and ground indicators pointing the wrong direction for configuration switches SW27, SW28, and SW32. This should be corrected with an adhesive label.
- Signal descriptions for JTAG connector are incorrect on the Quad T1E1 card. This should be corrected with an adhesive label.
- In the PCB layout the transformer TX primary is on the wrong side (creating a 2:1 winding instead of a 1:2). This has been corrected in the schematic, the PCB / assembly has been modified to correct this.

FILE LOCATIONS

This design kit relies upon several supporting files, which are provided on the CD and are available as a zip file from the Maxim website at www.maxim-ic.com/DS33Z44DK.

All locations are given relative to the top directory of the CD/zip file.

- DS33Z44 register definition files and configuration files:
  - .\cfg_demo_gui\DS33Z44_cfg_demo_gui\DS33Z44.def
  - .\DS33Z44_cfg_demo_gui\SU_LI_PORT4.def (def files for port 3, 2, 1 not shown)
  - .\DS33Z44_cfg_demo_gui\basic_config.mfg

- DS21458 register definition files and configuration files:
  - .\DS33Z44_cfg_demo_gui\Qt1e1_DS21458\DS21458RC.def
  - .\DS33Z44_cfg_demo_gui\Qt1e1_DS21458\DS21458RC_FPGA.def
  - .\DS33Z44_cfg_demo_gui\Qt1e1_DS21458\e1_gapclk_crc4_hdb3_nocas.ini
  - .\DS33Z44_cfg_demo_gui\Qt1e1_DS21458\gapclk_DS21458_T1_ESF_LBO0.ini

- DS3174 register definition files and configuration files:
  - .\DS33Z44_cfg_demo_gui\Qt3e3_DS3184\ds3184_evbrd_reduced.def
  - ….. 14 other low level def files ….
  - .\DS33Z44_cfg_demo_gui\Qt3e3_DS3184\84_t3_sct_needscoaxlb.mfg

BASIC OPERATION

Powering Up the Design Kit

- Attach resource card to main board.
- Connect PCB 3.3V and GND banana plugs to power supply. At power-up the system should draw approximately 1A.
- Set switches for software mode as described in Table 2 (short description follows).
  - Top left bank: All low, except for MODEC0, which is high.
  - Top right bank: A2, A1, A0 in mid position, SCANTRI low
  - Bottom Bank: All high (AFCS, FULLDS, H1OS)

General

- Upon power-up, the processor FPGA Status LEDs (DS19 green) will be lit. Interrupt LEDs (DS42 red) will not be lit. DS33Z44 Queue overflow LEDs (DS45, DS46, DS47, DS48 red) will not be lit. PHY LINK LED (DS02, DS03, DS14 green) should be lit if the Ethernet is connected.

Following are several basic system initializations.

Basic DS33Z44 Initialization (Used for All Quick Setups)

This section covers four basic methods for configuring the Z44. Any one of these initializations can be used with the following Quick Setup examples:

1. Upon power-up, the on-board device driver provides a basic configuration for the DS33Z44 and attached serial cards. This enables traffic to pass from the Ethernet port to the serial port. Consult the device driver documentation for further details. Device driver behavior is dependant upon jumper settings, which are detailed in Table 2.
2. Register-Based Configuration. Launch ChipView.exe and select *Register View.* When prompted for a definition file, pick the file named **DS33Z44.def**. After the definition file loads, go to the File menu and select File→Memory Config File→Load .MFG file. When prompted, select the file named **4Portsbasic_config.mfg**.
3. Hardware Mode. Set switches as described in the section for powering up the design kit, then change the following: HWMODE←3.3V, A0←3.3VV, A1←3.3V, A2←0V. This sets the part for LSB first, scrambling off, HDLC encapsulated. At this point traffic will pass from the Ethernet port to the serial port. In this mode broadcast frames are not passed (i.e., ping).
4. EEPROM mode is available with the DK, but is beyond the scope of this manual.

Quick Setup #1 (Device Driver + CPLD Loopback)

- On the serial resource card install jumper 24. Jumpers JP16–JP19 should be set high. This places the card in CPLD loopback and enables all four ports as described in Table 3.
- Complete the hardware configuration and one of the basic DS33Z44 configurations as described in the previous section.
- Using a patch cable, connect the Ethernet connector to an ordinary PC, or network test equipment. This should cause the link LED to turn on.
- At this point any packets sent to the DS33Z44 are echoed back. Incoming packets (i.e., ping) should cause the RX LED to blink, after which the TX LED should also blink.
- To interact with the device driver select from the drop down menu:
  - Tools→Plugins→Load Plugins. When asked if DLLs have already registered select yes
  - Select Tools→Plugins→DS33Z44/11/41 Device Driver Demo
  - A new form called ‘Zchip Configuration’ pops up.
  - Preload basic configuration for the GUI by selecting File→Load Settings (in the ‘Zchip Configuration’ form). Select the file named ‘basic_Config.eset’

Quick Setup #2 (DS3174 T3E3)

- On the DS3174 serial resource card install jumper J24. Jumpers JP16–JP19 should be set high. This places the card in DS3174 mode and enables all four ports as described in Table 3.
- Complete the hardware configuration and one of the basic DS33Z44 configurations as previously described.
- Using a patch cable, connect the Ethernet connector to an ordinary PC, or network test equipment. This should cause the link LED to turn on.
- Launch ChipView.exe (or use existing session if it is already open) and select *Register View*. When prompted for a definition file, pick the file name **ds3184_evbrd_reduced.def**. After the definition file loads, go to the File menu and select File→Memory Config File→Load .MFG file. When prompted, select the file named **84_t3_sct_needscoaxlb.mfg**.
- Place a loopback connector at the DS3174 network side.
- At this point, any packets sent to the DS33Z44 are echoed back. Incoming packets (i.e., ping) should cause the RX LED to blink, after which the TX LED should also blink.

Quick Setup #3 (DS21458 T1E1)

- Complete the hardware configuration and one of the basic DS33Z44 configurations as previously described.
- Using a patch cable, connect the Ethernet connector to an ordinary PC, or network test equipment. This should cause the link LED to turn on.
- Launch ChipView.exe (or use existing session if it is already open) and select *Register View.* When prompted for a definition file, pick the file named **DS21458.def**. After the definition file loads, go to the File menu and select File→Reg Ini File→Load Ini File. When prompted, pick the file named **e1_gapclk_crc4_hdb3_nocas.ini**.
- Place a loopback connector at the DS21458 network side; RLOS LED should go out.
- At this point any packets sent to the DS33Z44 are echoed back. Incoming packets (i.e. ping) should cause the RX LED to blink, after which the TX LED should also blink.

CONFIGURATION SWITCHES AND JUMPERS

The DS33Z44DK has several configuration switches, banana plugs, oscillators, and jumpers. Table 2 provides a description of these signals, given in order of appearance on the PC board (going from left to right, top to bottom).

Table 2. Main Board PC Board Configuration

SILKSCREEN REFERENCE	FUNCTION	BASIC SETTING		DESCRIPTION
		SW MODE	HW MODE	
J25.9 + J25.10	Reserved	Not Installed	—	This jumper is not for use with the DS33Z44 design kit. Pin J25.10 has been removed to prevent accidental installation.
J25.7 + J25.8	Enable device driver	User decision	—	When installed the device driver will configure the DS33Z44 and the Transceiver during power-up.
J25.5 + J25.6	Enable callbacks	User decision	—	When installed the driver will respond to interrupts.
GROUND (banana plug)	Power supply ground	—	—	System Ground. Always connected to power supply.
VDD 3.3V (banana plug)	Power supply VDD	—	—	System VDD. Always connected to power supply.
OnCe	BDM	—	—	Debug connector for processor
DCEDTES (3pos switch)	DS33Z44 mode pin; DTE/DCE selection	Low	Low	Low for DTE
RMIIMII (3pos switch)	DS33Z44 mode pin	Low	Low	High for RMII, low for MII
CKPHA (3pos switch)	DS33Z44 mode pin	Low	Low	SPI EEPROM hardware mode configuration switch
MODEC0 (3pos switch)	DS33Z44 mode pin	High	Low	Software mode selected
MODEC1 (3pos switch)	DS33Z44 mode pin	Low	Low	Software mode selected
HWMODE (3pos switch)	DS33Z44 mode pin	Low	Low	Hardware/software mode (software mode selected)
SCANMO (3pos switch)	DS33Z44 mode pin	Low	Low	Set low for normal operation
SCANTRI (3pos switch)	DS33Z44 mode pin	Low	Low	Set low for normal operation
….testpoints….	DS33Z44 testpoints	—	—	Processor bus, JTAG and LAN side testpoints for Zchip
Z-RESET (button)	DS33Z44 reset	—	—	System reset
A2, A1, A0 (3pos switches)	DS33Z44/SPI pins	Mid position	Mid position	Address pin/EEPROM config switch. Set to mid position to allow connection to processor.
SDRAM CLOCK	DS33Z44 SDRAM clock	Installed	Installed	100MHz oscillator to drive SDRAM clock
MII CLOCK	PHY MII clock	Installed	Installed	25MHz oscillator to drive SDRAM clock
spi_cs, spi_ck, spi_miso, spi_mosi	—	—	—	SPI signals (for EEPROM memory)
….testpoints…..	DS33Z44 testpoints	—	—	DS33Z44 serial port testpoints
AFCS (1 per port)	DS33Z44 mode pin	HW mode only	High	Set high to enable auto flow control.

SILKSCREEN REFERENCE	FUNCTION	BASIC SETTING		DESCRIPTION
		SW MODE	HW MODE	
FULLDS (1 per port)	DS33Z44 mode pin	HW mode only	High	Set high to enable full duplex.
H10S (1 per port)	DS33Z44 mode pin	HW mode only	High	Set high to confg for 100Mb.
GROUND/VDD (banana plug)	Power supply ground/3.3V	—	—	Redundant connection to system power. Use plugs at either top or bottom of board.
VDD 3.3V (banana plug)	Power supply VDD	—	—	Redundant connection to system power. Use plugs at either top or bottom of board.

Table 3. DS3174 Serial Reference Card Jumper Settings

JUMPER SETTINGS	MODE	COMMENT
JP16	Port 4 tri-state (at CPLD)	When the middle pin of this 3 position jumper is set to VCC, the CPLD passes traffic from the DS3174 to the DS33Z44. When the pin is set low, the CPLD tri-states this port.
JP17	Port 2 tri-state (at CPLD)	When the middle pin of this 3 position jumper is set to VCC, the CPLD passes traffic from the DS3174 to the DS33Z44. When the pin is set low, the CPLD tri-states this port.
JP18	Port 3 tri-state (at CPLD)	When the middle pin of this 3 position jumper is set to VCC, the CPLD passes traffic from the DS3174 to the DS33Z44. When the pin is set low, the CPLD tri-states this port.
JP19	Port 1 tri-state (at CPLD)	When the middle pin of this 3 position jumper is set to VCC, the CPLD passes traffic from the DS3174 to the DS33Z44. When the pin is set low, the CPLD tri-states this port.
J243	CPLD loopback	CPLD loopback makes the following connections: Zrser ← Ztser, Ztden ← 3.3V, Zrden ← 3.3V, Ztclki ← OscY03, Zrclki ← OscY03

ADDRESS MAP (ALL CARDS)

Motorola resource card address space begins at 0x81000000. All offsets given below are relative to the beginning of the daughter card address space (shown previously).

Table 4. Overview of Daughter Card Address Map

OFFSET	DEVICE	DESCRIPTION
0X0000 to 0X0087	FPGA	Processor board identification
0X1000 to 0X1FFF	DS33Z44	DS33Z44. Uses CS_X1.
0X2000 to 0X2FFF	DS21458	T1E1 DS21458 resource card. Uses CS_X2.
0X4000 to 0X4010	FPGA	FPGA on DS21458 resource card. Used to facilitate IBO mode. Default configuration of FPGA is compatible with non-IBO mode functionality. The FPGA settings do not require modification for use with the DS33Z44.
0X3000 to 0X3FFF	DS3174	T3E3 resource card. Uses CS_X3.

Registers in the DS33Z44, DS21458, and DS3174 can be easily modified using the ChipView host-based user-interface software with the definition files previously mentioned.

DS33Z44 INFORMATION

For more information about the DS33Z44, consult the DS33Z44 data sheet available on our website at www.maxim-ic.com/DS33Z44.

DS33Z44DK INFORMATION

For more information about the DS33Z44DK, including software downloads, consult the DS33Z44DK data sheet available on the our website at www.maxim-ic.com/DS33Z44DK.

TECHNICAL SUPPORT

For additional technical support, go to www.maxim-ic.com/support.

DOCUMENT REVISION HISTORY

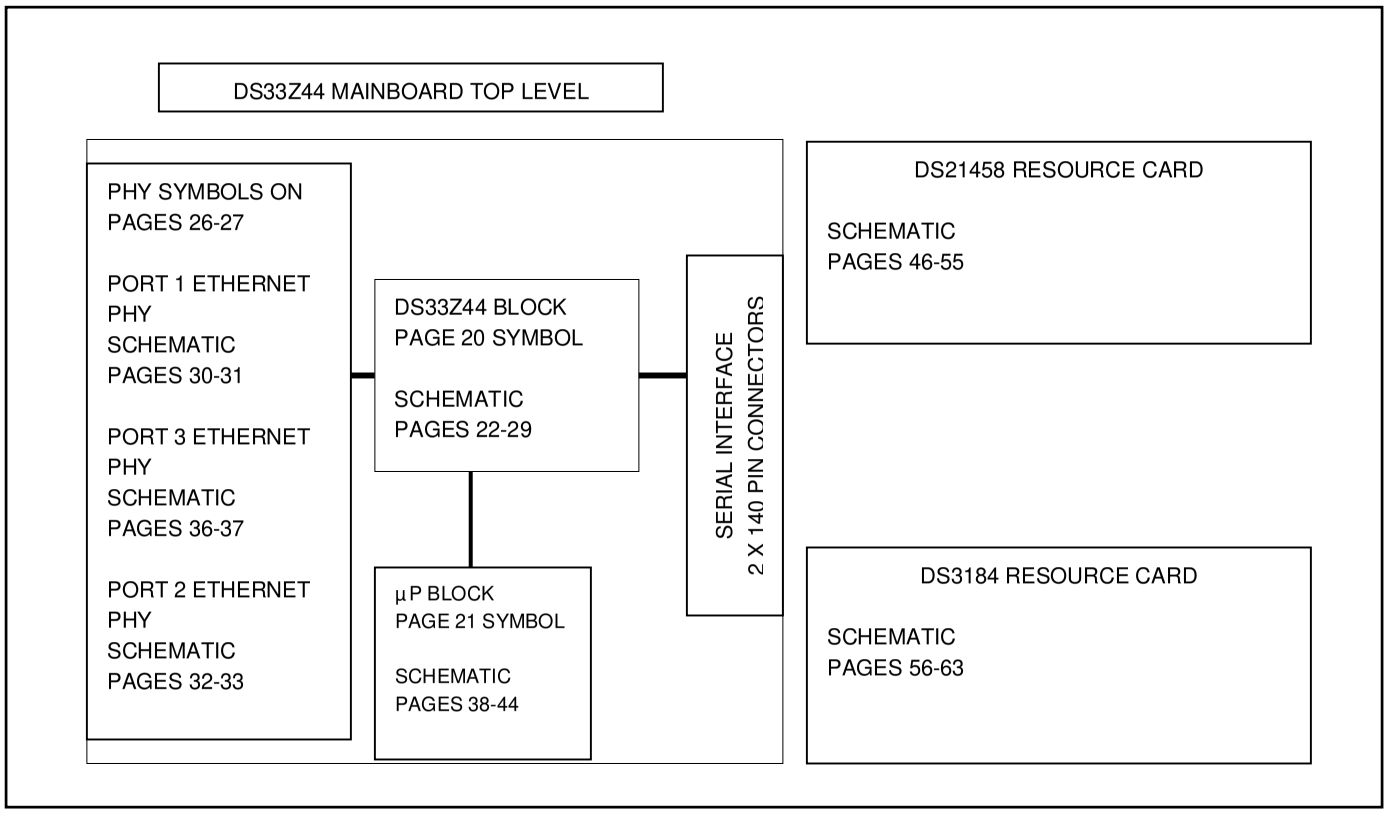
REVISION DATE	DESCRIPTION
032305	Initial DS33Z44DK data sheet release.
042205	Updated *Basic DS33Z44 Initialization* section; added step to *Quick Setup #1*.
051105	Added new PC board errata.
110106	Updated schematics.

SCHEMATICS

The DS33Z44DK schematics are featured in the following pages. As this is a hierarchal schematic some explanation is in order. The main board is composed of six hierarchal blocks: the processor block, the DS33Z44 block, and four Ethernet blocks inside the DS33Z44 block, which is a nested hierarchy block. Each serial card (DS21458 and DS3174) consists of a single hierarchy block, which connects to a 140-pin AV bus that snaps into the mainboard.

All signals inside a hierarchy block are local, with exception for V_{CC} and ground. In-port and out-port connectors are used to allow signals inside a hierarchy block to become accessible as pins on the hierarchy blocks symbol. From here, blocks are wired together as if they were ordinary components. The system diagram is shown again below, with schematic page numbers given for each functional block.

This system contained other hierarchy blocks that are not shown (primarily a single-port serial card and the DS33Z11 mainboard). Due to this, page numbers will not be continuous and some gaps in numbering will be seen when referring to the total page count. However, page numbers inside any given hierarchy block will be continuous.



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CR-20 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_IB@_ZTOP_LIB\._Z44TOP_DN\(SCH_1):PAGE1

DS33Z44 TOP LEVEL

PLUG
P2 CONNECTOR (PLUG)

JB14

PLUG
P1 CONNECTOR (PLUG)

JB10

HIERARCHICAL BLOCK
_z44and1an_dn

PAGES 22-29

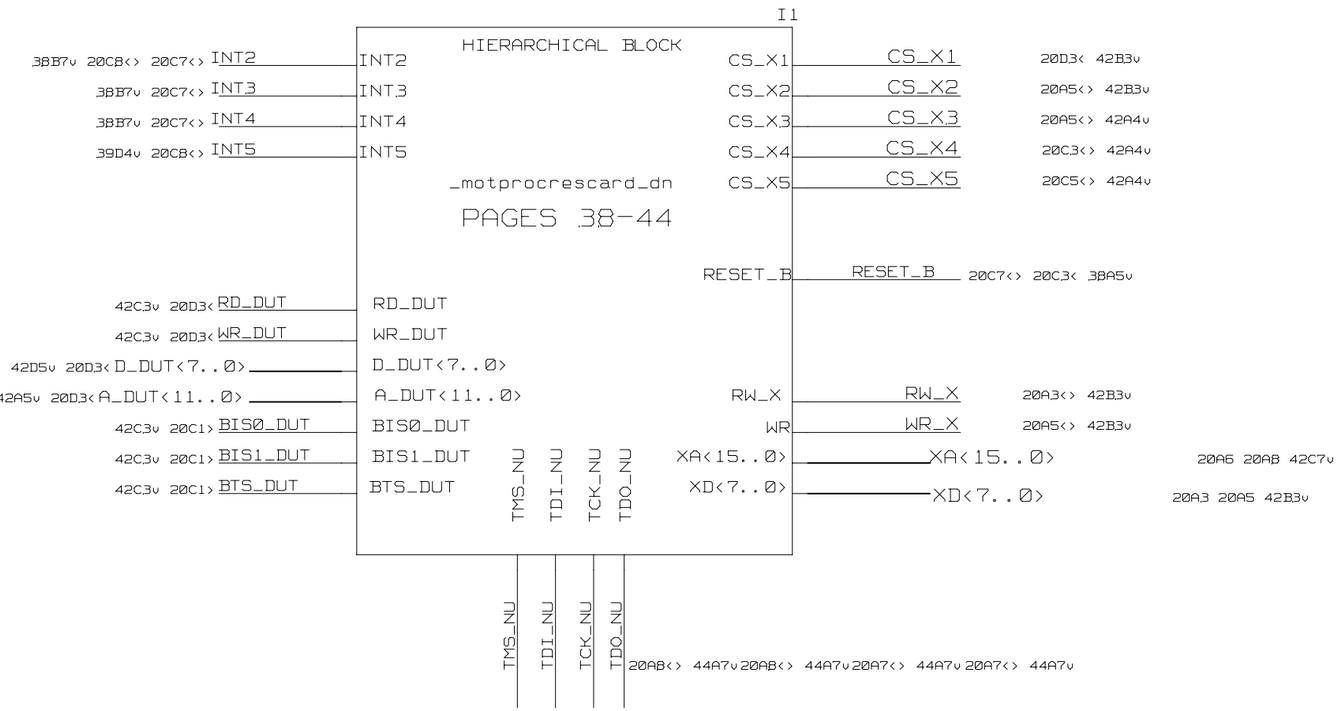
MOTHERBOARD CONNECTORS FOR WAN R.C.

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 1/2(BLOCK) 20/71(TOTAL)

BLOCK NAME: _z44top_dn. PARENT BLOCK: _ztopdn_\

PRINTED Fri Oct 20 11:06:56 2006

CR-21 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_IB@_ZTOP_LIB\._Z44TOP_DN\(SCH_1):PAGE2



TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 2/2 (BLOCK) 21/71 (TOTAL)

BLOCK NAME: _z44top_dn. PARENT BLOCK: _ztopdn_\

JTAG

F7 JTMS 22A5<> — JTMS
E4 JTDI 22A5<> — JTDI
E5 JTDO 22A5<> — JTDO
D4 JTCLK 22A5<> — JTCLK
E6 JTRST 22A5<> — JTRST

U22

DS33Z44_U1

MII/RMII

28A4< REF_CLK	YTPB02	C15	REF_CLK
REF_CLKO	RB181	B15	REF_CLKO
27B3> 26B6> 26B3> 27B6> MDC	R99	F11	MDC
27B3> 26B6> 26B3> 27B6> MDIO	RB161 / YTPB01	F10	MDIO

SDRAM CONTROL

24B4< SD_BA0	RB230	R8	SBA<0>
24B4< SD_BA1	RB246	R9	SBA<1>
24C4< SD_DQM0	R166	T8	SDMASK<0>
24C4< SD_DQM1	RB239	M7	SDMASK<1>
24C4< SD_DQM2	R147	T11	SDMASK<2>
24C4< SD_DQM3	RB217	N11	SDMASK<3>
24C4< SD_CS	R158	P8	SDCS*
24C3< SD_CLKO	RB226	T7	SDCLKO
28D5< SD_CLKI		T15	SYSCLKI
24C4< SD_RAS	RB219	P15	SRAS*
24C4< SD_CAS	R163	N7	SCAS*
24C4< SD_WE	RB282	R7	SWE*

UNMARKED RESISTORS ARE 30 OHM

MICRO PORT/SPI MASTER PORT

INT*	INT	D3	20D2^ 22A6<>
CS*	CS	D1	20D3^ OUT
SPI_CS*	SPICSZ	E13	22C2< IN
RD*/DS*	RD	E1	20D3^ IN
WR*/RW*	WR	E2	20D3^ IN
RST*	RESET_B	B2	20D3^
HWMODE	HWMODE	D5	28D4< 20C2^ OUT
MODEC<0>	MODEC0	D6	28D2< 20C2^ OUT
MODEC<1>	MODEC1	D4	28D4< 20C2^ OUT
DCEDTES	DCEDTES	S1	28D2<
RMIIMIIS	RMIIMIIS	C4	28C4<
SCAN ENABLE	SCANEN	E7	28B4<
SCAN MODE	SCANMOD	B3	28C4<
CKPHA	CKPHA	F6	28B4<

A<0> A1 ZADDR0 22B2<>
A<1> B1 ZADDR1 22B2<>
A<2> A2 ZADDR2 22A2<>
A<3> B2 3
A<4> C2 4
A<5> A3 5
A<6> B3 6
A<7> C3 7
A<8> A4 8
A<9> B4 9 — ADDR<9..0> IN 20D3^ 22B1<

D<0>/MOSI A5 ZMOSI 0
D<1>/MISO A6 ZMISO 1
D<2>/SPICK A7 ZSPISCK 2
D<3> B5 3
D<4> B6 4
D<5> B7 5
D<6> C5 6
D<7> C6 7 — DAT<7..0> IO 20D3^

2.7V

Y02

AT25160A_U

22C4<> ZMOSI	5	SI	
22C4<> ZMISO	2	SO	
22B4<> ZSPISCK	6	SCK	
22A6> ZSPICS	1	CS*	
VCC	8		V3_3
WP*	3	RB79 10K	V3_3
HOLD*	7	RB74 10K	V3_3
GND	4		

20D3^ 22C4<

SW04 SP3T
SW08 SP3T
SW18 SP3T

22D4< ZADDR0 — 0
22C4< ZADDR1 — 1
22C4< ZADDR2 — 2

V3_3 — IN — ADDR<9..0>

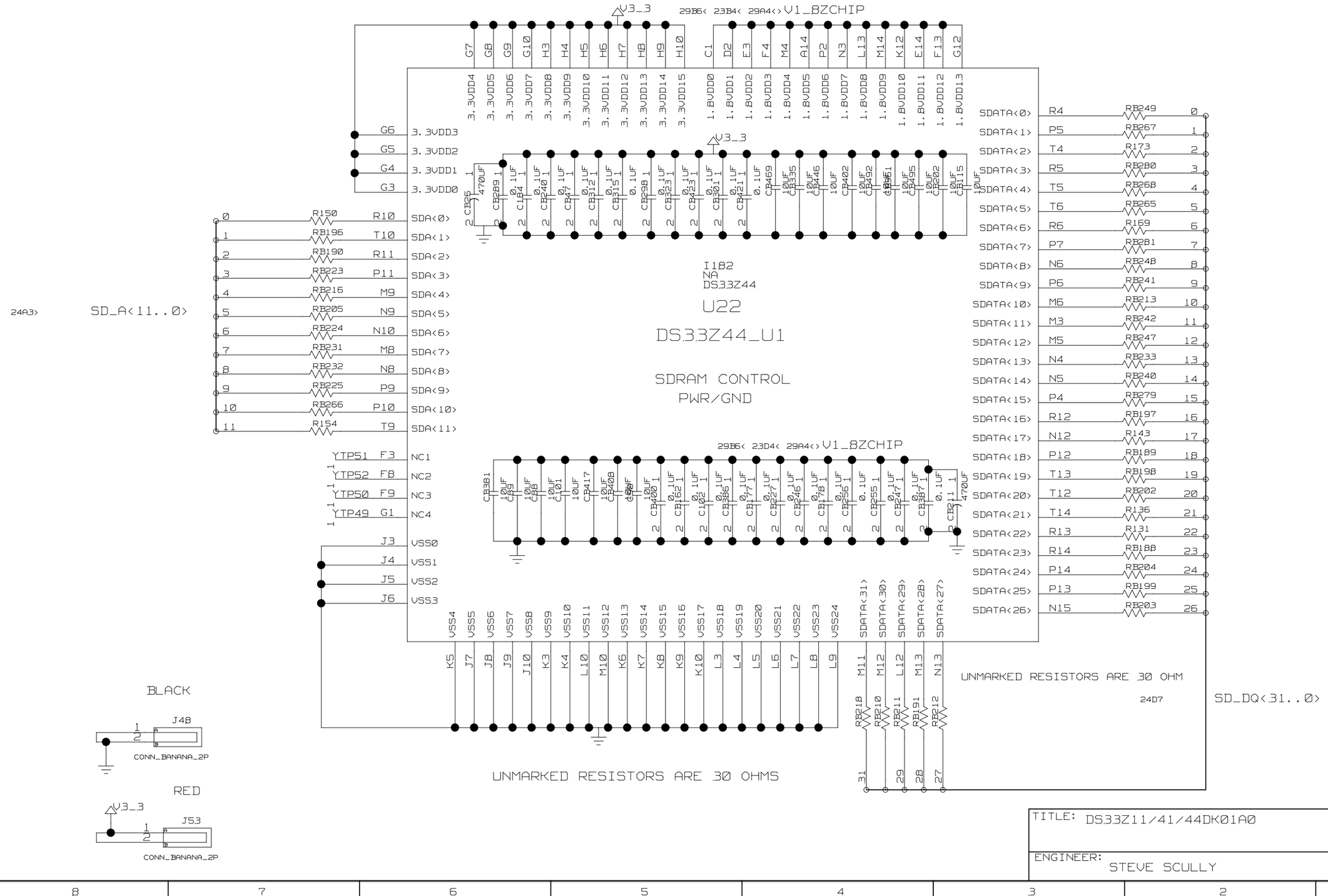
V3_3 — RB332 330 — RED DS42 — NC7SZ86_U BUFFER UXB07 — INT 22A7> 20D2^

J32 CONN_10P

22D6< JTCLK	1	2	TCK_NU
22D6< JTMS	3	4	TMS_NU
22D6<> JTDO	5	6	TDI_NU
22D6< JTDI	7	8	TDO_NU
22D6< JTRST	9	10	V3_3

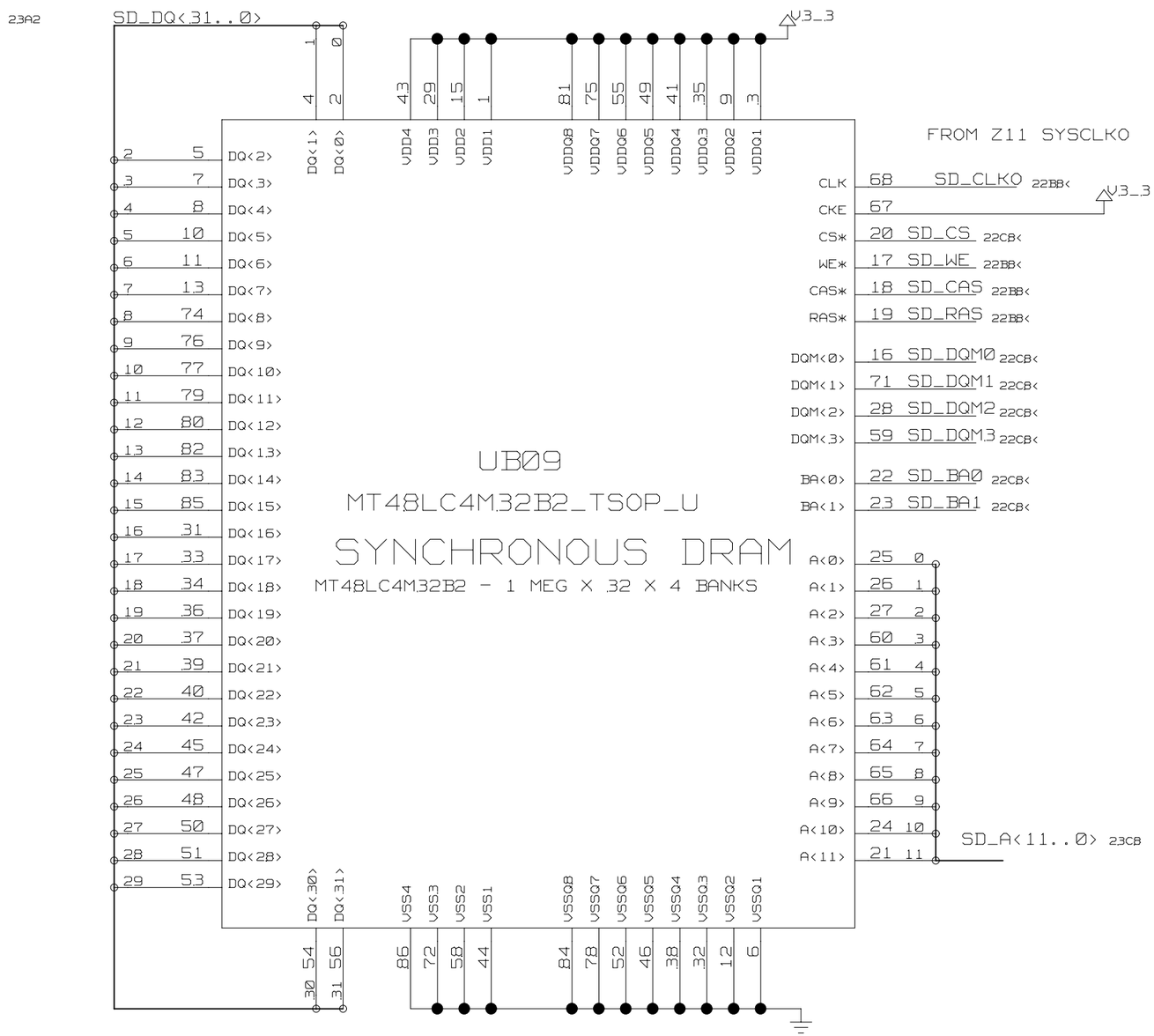
TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:1/8(BLOCK) 22/71(TOTAL)

CR-23 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_IB@_ZTOP_LIB\._Z44TOP_DN\(SCH_1):PAGE1_I2@_ZTOP_LIB\._Z44ANDLAN_DN\(SCH_1):PAGE2



TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:2/8(BLOCK) 23/71(TOTAL)

BLOCK NAME: _z44andlan_dn. PARENT BLOCK: _z44top_dn\



TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:3/8(BLOCK) 24/71(TOTAL)

CR-25 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_IB@_ZTOP_LIB\._Z44TOP_DN\(SCH_1):PAGE1_I2@_ZTOP_LIB\._Z44ANDLAN_DN\(SCH_1):PAGE4

REV01A0 SCHEMATIC SYMBOL (AND PCB) FOR Z44 HAD ERRORS
TXD/RXD PINS FOR PHY CONNECTION WERE INCORRECT
CORRECT PINOUT SHOWN AT BOTTOM OF PAGE

U22

PORT1 PIN G2

DS33Z44_U1

20D2^ IN	RCLKI<1> YTP57	G2	RCLKI	PORT	TCLKI	F1 YTP63	TCLKI<1>	IN 20D2^
20D2^ IN	RSER<1> YTP59	H1	RSER		TSER	F2 YTP65	RB335 30 TSER<1>	OUT 20D2^
20D2^ IN	RDEN<1> YTP58	H2	RDEN/RBSYNC		TDEN/TBSYNC	F5 YTP64	TDEN<1>	IO 20D2^
26D5>	RXD0<1>	B11	RXD0		TXD0	B9	R105 30 TXD0<1>	26DB<
26D5>	RXD1<1>	C11	RXD1		TXD1	C9	R122 30 TXD1<1>	26DB<
26D5>	RXD2<1>	D11	RXD2		TXD2	D9	R96 30 TXD2<1>	26DB<
26D5>	RXD3<1>	E11	RXD3		TXD3	E9	R115 30 TXD3<1>	26DB<
26C5>	RXDV<1>	D10	RXDV		TX_EN	E10	R98 30 TX_EN<1>	26CB<
26C5>	RX_CRS<1>	D12	RX_CRS/CRS_DV		TX_CLK	A9	TX_CLK<1>	26DB<
26C5>	RX_ERR<1>	E12	RX_ERR		RX_CLK	A11	RX_CLK<1>	26D5>
					QOVF	C7	QOVF<1>	29DB<>
26C5>	COL_DET<1>	D13	COL_DET		H10S	B10	H10S<1>	29C2<
29D2<	FULLDS<1>	A10	FULLDS		AFCS	C10	AFCS<1>	29D2<

U22

PORT2 PIN L2

DS33Z44_U1

20D2^ IN	RCLKI<2> YTP54	L2	RCLKI	PORT	TCLKI	J1 YTP60	TCLKI<2>	IN 20D2^
20D2^ IN	RSER<2> YTP56	K1	RSER		TSER	J2 YTP62	RB33930 TSER<2>	OUT 20D2^
20D2^ IN	RDEN<2> YTP55	L1	RDEN/RBSYNC		TDEN/TBSYNC	K2 YTP61	TDEN<2>	IO 20D2^
26D2>	RXD0<2>	K13	RXD0		TXD0	R15	RB164 TXD0<2>	26D5<
26D2>	RXD1<2>	K14	RXD1		TXD1	R16	RB165 30 TXD1<2>	26D5<
26D2>	RXD2<2>	H15	RXD2		TXD2	L15	RB180 30 TXD2<2>	26D5<
26D2>	RXD3<2>	K16	RXD3		TXD3	N14	RB121 30 TXD3<2>	26D5<
26C2>	RXDV<2>	K15	RXDV		TX_EN	L14	RB179 30 TX_EN<2>	26C5<
26C2>	RX_CRS<2>	N16	RX_CRS/CRS_DV		TX_CLK	M16	TX_CLK<2>	26D5<
26C2>	RX_ERR<2>	T16	RX_ERR		RX_CLK	L16	RX_CLK<2>	26D2>
					QOVF	C8	QOVF<2>	29DB<>
26C2>	COL_DET<2>	P16	COL_DET		H10S	L11	H10S<2>	29A2<
29B2<	FULLDS<2>	J15	FULLDS		AFCS	J16	AFCS<2>	29B2<

U22

PORT3 PIN N2

DS33Z44_U1

20D2^ IN	RCLKI<3>	N2	RCLKI	PORT	TCLKI	M1	TCLKI<3>	IN 20D2^
20D2^ IN	RSER<3>	P1	RSER		TSER	M2	RB311 30 TSER<3>	OUT 20D2^
20D2^ IN	RDEN<3>	N1	RDEN/RBSYNC		TDEN/TBSYNC	P3	TDEN<3>	IO 20D2^
27D5>	RXD0<3>	G15	RXD0		TXD0	F15	R97 30 TXD0<3>	27DB<
27D5>	RXD1<3>	J14	RXD1		TXD1	G14	R123 30 TXD1<3>	27DB<
27D5>	RXD2<3>	J13	RXD2		TXD2	H13	RB187 30 TXD2<3>	27DB<
27D5>	RXD3<3>	J12	RXD3		TXD3	H14	RB169 30 TXD3<3>	27DB<
27C5>	RXDV<3>	K11	RXDV		TX_EN	E15	RB170 30 TX_EN<3>	27CB<
27C5>	RX_CRS<3>	M15	RX_CRS/CRS_DV		TX_CLK	G16	TX_CLK<3>	27DB<
27C5>	RX_ERR<3>	G11	RX_ERR		RX_CLK	H16	RX_CLK<3>	27D5>
					QOVF	B8	QOVF<3>	29CB<>
27C5>	COL_DET<3>	H11	COL_DET		H10S	F12	H10S<3>	29C4<
29D4<	FULLDS<3>	H12	FULLDS		AFCS	J11	AFCS<3>	29C4<

U22

PORT4 PIN T3

DS33Z44_U1

20D2^ IN	RCLKI<4>	T3	RCLKI	PORT	TCLKI	R1	TCLKI<4>	IN 20D2^
20D2^ IN	RSER<4>	T2	RSER		TSER	R2	RB320 30 TSER<4>	OUT 20D2^
20D2^ IN	RDEN<4>	T1	RDEN/RBSYNC		TDEN/TBSYNC	R3	TDEN<4>	IO 20D2^
27D2>	RXD0<4>	B13	RXD0		TXD0	B16	R126 30 TXD0<4>	27D4<
27D2>	RXD1<4>	C13	RXD1		TXD1	C16	RB171 30 TXD1<4>	27D4<
27D2>	RXD2<4>	B14	RXD2		TXD2	D16	RB167 30 TXD2<4>	27D4<
27D2>	RXD3<4>	C14	RXD3		TXD3	E16	RB168 30 TXD3<4>	27D4<
27C2>	RXDV<4>	D15	RXDV		TX_EN	G13	R124 30 TX_EN<4>	27C4<
27C2>	RX_CRS<4>	F14	RX_CRS/CRS_DV		TX_CLK	A16	TX_CLK<4>	27D4<
27C2>	RX_ERR<4>	D14	RX_ERR		RX_CLK	A13	RX_CLK<4>	27D2>
					QOVF	A8	QOVF<4>	29CB<>
27C2>	COL_DET<4>	F16	COL_DET		H10S	B12	H10S<4>	29A4<
29B4<	FULLDS<4>	A12	FULLDS		AFCS	C12	AFCS<4>	29A4<

PORT1 TXD0--TXD3 B9, C9, D9, E9
PORT2 TXD0--TXD3 R15, R16, L15, N14
PORT3 TXD0--TXD3 F15, G14, H13, H14
PORT4 TXD0--TXD3 B16, C16, D16, E16

PORT1 RXD0--RXD3 B11, C11, D11, E11
PORT2 RXD0--RXD3 K13, K14, H15, K16
PORT3 RXD0--RXD3 G15, J14, J13, J12
PORT4 RXD0--RXD3 B13, C13, B14, C14

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 4/8 (BLOCK) 25/71 (TOTAL)

BLOCK NAME: _z44andlan_dn. PARENT BLOCK: _z44top_dn\

CR-26 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_IB@_ZTOP_LIB\._Z44TOP_DN\(SCH_1):PAGE1_I2@_ZTOP_LIB\._Z44ANDLAN_DN\(SCH_1):PAGE5

HIERARCHICAL BLOCK

_mii_wan_dn

PAGES 30-31

30A5v 25C5< TXD0<1> → TXD0
30A5v 25C5< TXD1<1> → TXD1
30A5v 25C5< TXD2<1> → TXD2
30A5v 25C5< TXD3<1> → TXD3
30A5v 25C5<> TX_CLK<1> → TX_CLK
30A5v 25C5< TX_EN<1> → TX_EN

LED_DPLX_A0<1> → LED_DPLX_ADD0
LED_COL_A1<1> → LED_COL_ADD1
LED_GDLINK_A2<1> → LED_GDLINK_ADD2
LED_TX_A3<1> → LED_TX_ADD3
LED_RX_A4<1> → LED_RX_ADD4

RXD0 → RXD0<1> 25C8< 30A7v
RXD1 → RXD1<1> 25C8< 30A7v
RXD2 → RXD2<1> 25C8< 30A7v
RXD3 → RXD3<1> 25C8< 30A7v
RX_CLK → RX_CLK<1> 25C5<> 30A7v
RX_CRS → RX_CRS<1> 25C8< 30A7v
RX_ERR → RX_ERR<1> 25C8< 30A7v
RXDV → RXDV<1> 25C8< 30A7v
COL_DET → COL_DET<1> 25C8< 30A7v

RESET_B → RESET_B
MDIO → MDIO
MDC → MDC
MII_CLK → MII_CLK<1>

MII_CLK<1> 26B3> 27B3> 28A4< 30C7v 26B3> 27B3> 27B6> 22C8< 32C5v 30C5v

HIERARCHICAL BLOCK

_mii_wan_dn

PAGES 32-33

32A5v 25B5< TXD0<2> → TXD0
32A5v 25A5< TXD1<2> → TXD1
32A5v 25A5< TXD2<2> → TXD2
32A5v 25A5< TXD3<2> → TXD3
32A5v 25A5<> TX_CLK<2> → TX_CLK
32A5v 25A5< TX_EN<2> → TX_EN

32C5v 26B4< LED_DPLX_A0<2> → LED_DPLX_ADD0
32C5v 26B4< LED_COL_A1<2> → LED_COL_ADD1
32C5v 26A4<> LED_GDLINK_A2<2> → LED_GDLINK_ADD2
32C5v 26A4<> LED_TX_A3<2> → LED_TX_ADD3
32C5v 26A4<> LED_RX_A4<2> → LED_RX_ADD4

RXD0 → RXD0<2> 25B8< 32A7v
RXD1 → RXD1<2> 25A8< 32A7v
RXD2 → RXD2<2> 25A8< 32A7v
RXD3 → RXD3<2> 25A8< 32A7v
RX_CLK → RX_CLK<2> 25A5<> 32A7v
RX_CRS → RX_CRS<2> 25A8< 32A7v
RX_ERR → RX_ERR<2> 25A8< 32A7v
RXDV → RXDV<2> 25A8< 32A7v
COL_DET → COL_DET<2> 25A8< 32A7v

RESET_B → RESET_B
MDIO → MDIO
MDC → MDC
MII_CLK → MII_CLK<2>

MII_CLK<2> 27C3> 27C7> 20C3^ 22A6< 26B7< 30C7v 32C7v

MII_CLK<2> 26B6> 27B3> 28A4< 32C7v 26B6> 27B3> 27B6> 22C8< 32C5v 30C5v

30C5v 26C8< LED_DPLX_A0<1> → RB75 5.1K → V3_3
30C5v 26C8< LED_COL_A1<1> → RB80 5.1K → V3_3

30C5v 26C8< LED_GDLINK_A2<1> → R19 5.1K → DS09 (1, 2) → RB58 330 → GREEN

30C5v 26C8< LED_TX_A3<1> → R13 5.1K → DS07 (1, 2) → RB49 330 → AMBER

30C5v 26C8< LED_RX_A4<1> → R23 5.1K → DS13 (1, 2) → RB71 330 → RED

32C5v 26C5< LED_DPLX_A0<2> → R22 5.1K

32C5v 26C5< LED_COL_A1<2> → R18 5.1K → V3_3

32C5v 26C5< LED_GDLINK_A2<2> → RB34 5.1K → DS02 (1, 2) → RB33 330 → GREEN

32C5v 26C5< LED_TX_A3<2> → RB15 5.1K → DS01 (1, 2) → RB14 330 → AMBER

32C5v 26C5< LED_RX_A4<2> → R14 5.1K → DS05 (1, 2) → RB42 330 → RED

1000100MZH

V3_3 → L01 (2, 1) → 1000100MZH → LB02 (2, 1) → CHASSIS GND FOR PHY

CB03 10UF
CB01 10UF
CB02 10UF
C04 0.1UF (1, 2)

CHASSIS

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:5/8<BLOCK> 26/71<TOTAL>

BLOCK NAME: _z44andlan_dn, PARENT BLOCK: _z44top_dn\

CR-27 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_IB@_ZTOP_LIB\._Z44TOP_DN\(SCH_1):PAGE1_I2@_ZTOP_LIB\._Z44ANDLAN_DN\(SCH_1):PAGE5

HIERARCHICAL BLOCK

_mii_wan_dn

PAGES 36-37

TXD0 ← TXD0<3> (36A5v 25C1<)
TXD1 ← TXD1<3> (36A5v 25C1<)
TXD2 ← TXD2<3> (36A5v 25C1<)
TXD3 ← TXD3<3> (36A5v 25C1<)
TX_CLK ← TX_CLK<3> (36A5v 25C1<>)
TX_EN ← TX_EN<3> (36A5v 25C1<)
LED_DPLX_ADD0 ← LED_DPLX_A0<3> (27B8< 36C5v)
LED_COL_ADD1 ← LED_COL_A1<3> (27B8< 36C5v)
LED_GDLINK_ADD2 ← LED_GDLINK_A2<3>
LED_TX_ADD3 ← LED_TX_A3<3>
LED_RX_ADD4 ← LED_RX_A4<3>
RESET_B
MDIO
MDC
MII_CLK

RXD0 → RXD0<3> (25C4< 36A7v)
RXD1 → RXD1<3> (25C4< 36A7v)
RXD2 → RXD2<3> (25C4< 36A7v)
RXD3 → RXD3<3> (25C4< 36A7v)
RX_CLK → RX_CLK<3> (25C1<> 36A7v)
RX_CRS → RX_CRS<3> (25C4< 36A7v)
RX_ERR → RX_ERR<3> (25C4< 36A7v)
RXDV → RXDV<3> (25C4< 36A7v)
COL_DET → COL_DET<3> (25C4< 36A7v)

RESET_B
MII_CLK<3> → 26B3> 26B6> 28A4< 36C7v 26B3> 26B6> 27B3> 22C8< 34C5v 36C5v
MDIO → MDIO
MDC → MDC

HIERARCHICAL BLOCK

_mii_wan_dn

PAGES 34-35

TXD0 ← TXD0<4> (34A5v 25B1<)
TXD1 ← TXD1<4> (34A5v 25B1<)
TXD2 ← TXD2<4> (34A5v 25A1<)
TXD3 ← TXD3<4> (34A5v 25A1<)
TX_CLK ← TX_CLK<4> (34A5v 25A1<>)
TX_EN ← TX_EN<4> (34A5v 25A1<)
LED_DPLX_ADD0 ← LED_DPLX_A0<4> (34C5v 27B4<)
LED_COL_ADD1 ← LED_COL_A1<4> (34C5v 27B4<)
LED_GDLINK_ADD2 ← LED_GDLINK_A2<4> (34C5v 27A4<>)
LED_TX_ADD3 ← LED_TX_A3<4> (34C5v 27A4<>)
LED_RX_ADD4 ← LED_RX_A4<4> (34C5v 27A4<>)
RESET_B
MDIO
MDC
MII_CLK

RXD0 → RXD0<4> (25B4< 34A7v)
RXD1 → RXD1<4> (25B4< 34A7v)
RXD2 → RXD2<4> (25A4< 34A7v)
RXD3 → RXD3<4> (25A4< 34A7v)
RX_CLK → RX_CLK<4> (25A1<> 34A7v)
RX_CRS → RX_CRS<4> (25A4< 34A7v)
RX_ERR → RX_ERR<4> (25A4< 34A7v)
RXDV → RXDV<4> (25A4< 34A7v)
COL_DET → COL_DET<4> (25A4< 34A7v)

RESET_B
MII_CLK<4> → 26B3> 27C7> 20C3^ 22A6< 26B7< 36C7v 34C7v
MDIO → MDIO
MDC → MDC

26B3> 26B6> 28A4< 34C7v 26B3> 26B6> 27B6> 22C8< 34C5v 36C5v
27B6> 22C8< 34C5v 36C5v

LED_DPLX_A0<3> (36C5v 27C8<) — RB82 5.1K — V3_3
LED_COL_A1<3> (36C5v 27C8<) — RB51 5.1K — V3_3

LED_GDLINK_A2<3> (36C5v 27C8<) — RB32 5.1K — DS03 (1, 2) — RB40 330 — GREEN

LED_TX_A3<3> (36C5v 27C8<) — RB62 5.1K — DS12 (1, 2) — RB77 330 — AMBER

LED_RX_A4<3> (36C5v 27C8<) — RB36 5.1K — DS04 (1, 2) — RB43 330 — RED

LED_DPLX_A0<4> (34C5v 27C5<) — R30 5.1K
LED_COL_A1<4> (34C5v 27C5<) — R29 5.1K

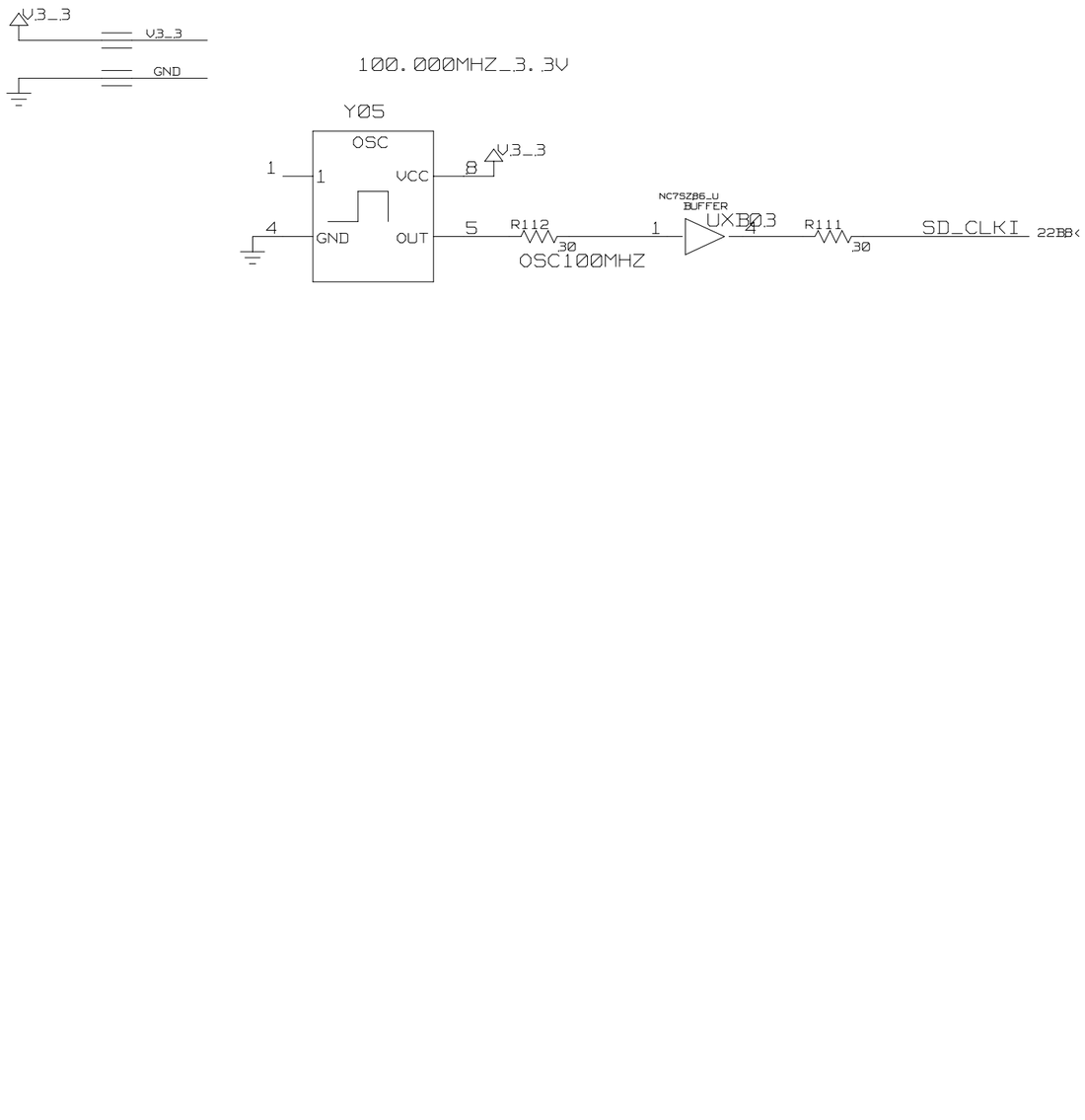
LED_GDLINK_A2<4> (34C5v 27C5<) — RB73 5.1K — V3_3 — GREEN — R24 330 — DS14 (2, 1)

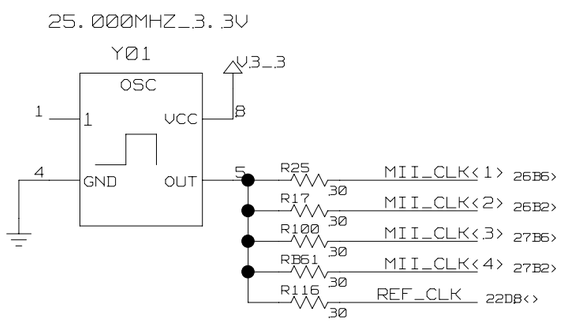
LED_TX_A3<4> (34C5v 27C5<) — R20 5.1K — DS10 (1, 2) — RB59 330 — AMBER

LED_RX_A4<4> (34C5v 27C5<) — R15 5.1K — DS08 (1, 2) — RB53 330 — RED

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:6/8(BLOCK) 27/71(TOTAL)

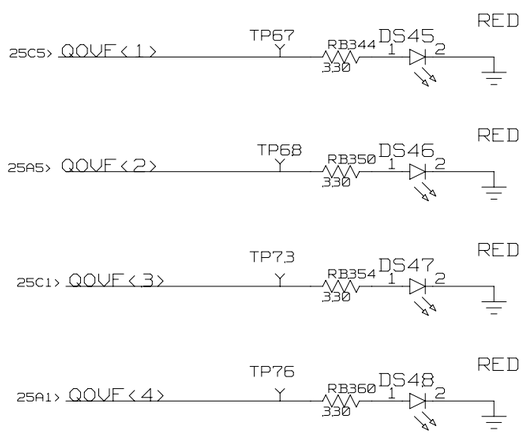
BLOCK NAME: _z44andlan_dn, PARENT BLOCK: _z44top_dn\

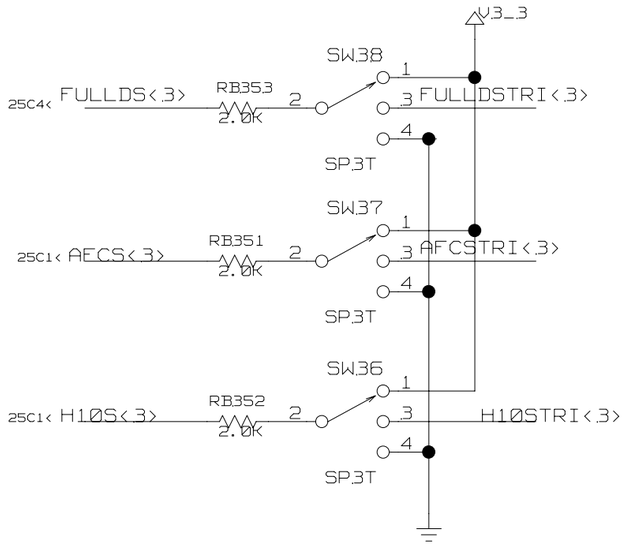


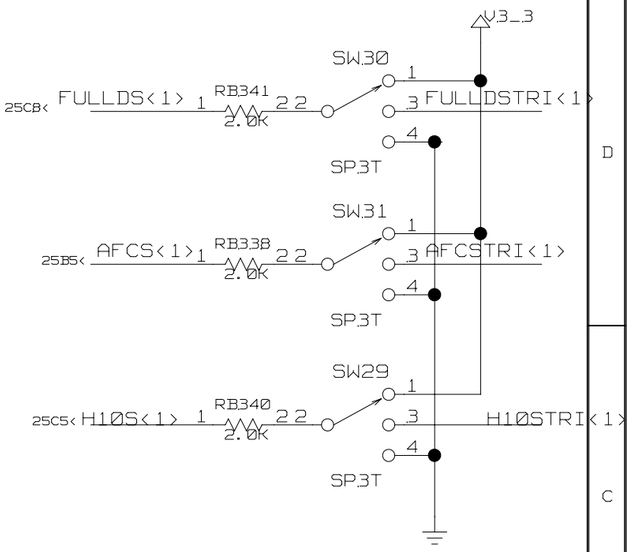


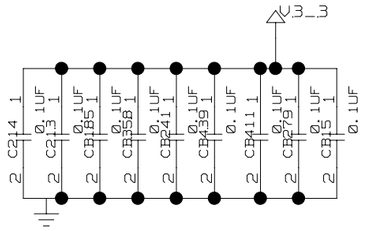
TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 7/8 (BLOCK) 28/71 (TOTAL)

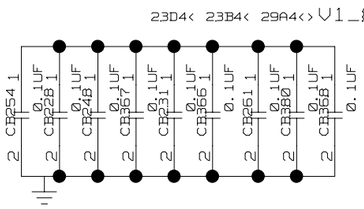
CR-29 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_IB@_ZTOP_LIB\._Z44TOP_DN\(SCH_1):PAGE1_I2@_ZTOP_LIB\._Z44ANDLAN_DN\(SCH_1):PAGE8

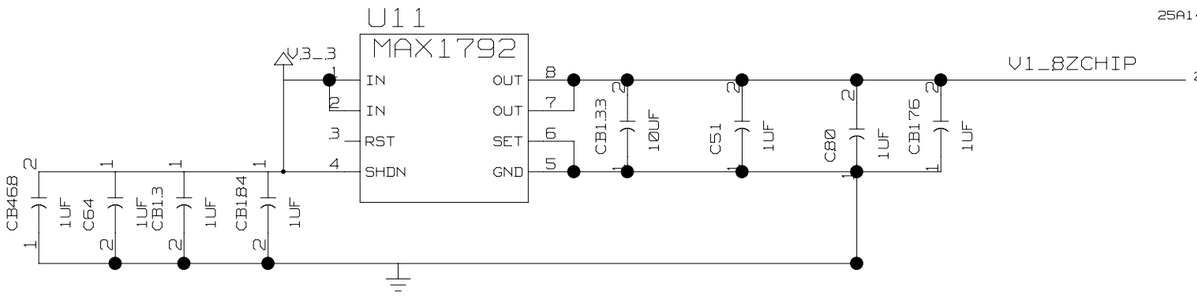


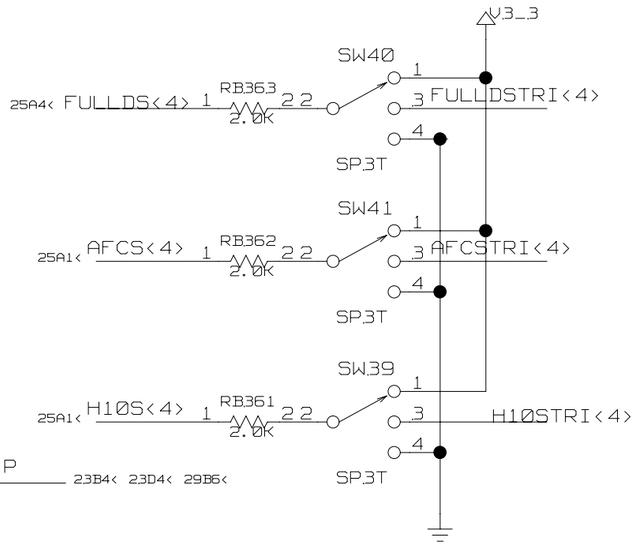


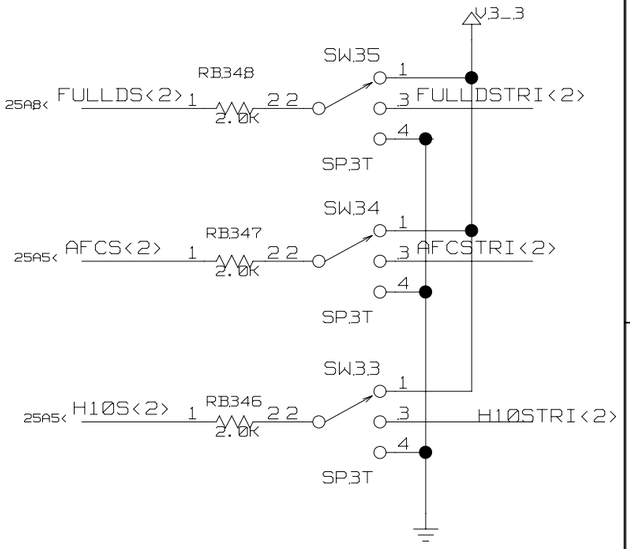












TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:8/8(BLOCK) 29/71(TOTAL)

BLOCK NAME: _z44andlan_dn. PARENT BLOCK: _z44top_dn\

CR-30 : @_ztop_lib\:_ztopdn_\(sch_1):page1_1B@_ztop_lib\:_z44top_dn\(sch_1):page1_12@_ztop_lib\:_z44anlan_dn\(sch_1):page5_154@_ztop_lib\:_mii_wan_dn\(sch_1):Page1

COMPONETS FOR
C1 AND RBIAS MUST
BE PLACED CLOSE TO PIN

C1PIN

C41 1 2 10UF
CB104 1 2 0.1UF

R06 10.0K RBIAS

26C6^ IN MII_CLK
26C7^ IN RESET_B

U02
DP83847_U1
CONTROL

RESERVED2
RESERVED1
C1
RBIAS
X1
RESET*
X2
RESERVED10
RESERVED11
RESERVED12
RESERVED13
RESERVED14
RESERVED15
RESERVED16
RESERVED17
RESERVED18
RESERVED3
RESERVED4
RESERVED5
RESERVED6
RESERVED7
RESERVED8
RESERVED9
VDD/IO_VDD1
VDD/IO_VDD2
VDD/ANA_VDD
VDD1
VDD2
VDD3
GND1
GND2
GND3
GND4
GND5

AN_V3_3
V3_3

MDC 25 R101 30 MDC IN 26C6^
MDIO 24 MDIO IO
LED_DPLX/PHYAD0 23 LED_DPLX_ADD0 IO
LED_COL/PHYAD1 22 LED_COL_ADD1 IO
LED_GDLNK/PHYAD2 21 LED_GDLINK_ADD2 IO
LED_TX/PHYAD3 20 LED_TX_ADD3 IO
LED_RX/PHYAD4 19 LED_RX_ADD4 IO
LED_SPEED 18 TP02
AN_EN 17 RB37 5.1K AN_EN
AN_1 16 RB30 5.1K AN1
AN_0 15 RB09 5.1K AN0

LEDS NEED TO BE ATTACHED
OUTSIDE OF MODULE DUE TO
STRAP ADAPTING OPTION OF DP83847

V3_3
JP01 JP07 JP12

J16

RXD0 1 2 RXDV
RXD1 3 4 RX_CRS
5 6 COL_DET
RXD2 7 8 RX_ERR
RXD3 9 9 10 RX_CLK

CONN_10P

J15

TX_CLK 1 2 TXD3
3 4 TXD2
5 6
7 8 TXD1
TX_EN 9 9 10 TXD0

CONN_10P

1000100MZH

L08

AN_V3_3

PLACEMENT NOTE:
TESTPOINTS (SHOWN ABOVE) MUST BE PLACED THE SAME FOR EACH PORT TO
ALLOW USE OF A DIFFERENT PHY CARD IF DESIRED. PLACEMENT SHOULD ALLOW
0.2 BETWEEN CONNECTORS.

ON Z44 CARD ALL 4 PORTS MUST BE PLACED WITH EQUAL SPACING AND A COMMON CENTER LINE

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 1/2(BLOCK) 30/71(TOTAL)

BLOCK NAME: _mii_wan_dn. PARENT BLOCK: _z44anlan_dn\

PRINTED Fri Oct 20 11:06:58 2006

U02

DP83847_U1

PORT

		35	TX_ER	RX_ER/PAUSE_EN*	33	RX_ERR	RB139 10K
TX_EN		37	TX_EN	RX_DV	31	RXDV	
TXD0		38	TXD<0>	RX_CLK	32		
TXD1		39	TXD<1>	TX_CLK	36		
TXD2		40	TXD<2>				
TXD3		41	TXD<3>				
RXD0	RB100 30	30	RXD<0>	CRS/LED_CFG*	45	RB127 30 RX_CRS	
RXD1	RB112 30	29	RXD<1>	COL	43	RB135 30 COL_DET	
RXD2	RB125 30	27	RXD<2>				
RXD3	R106 30	26	RXD<3>				
RD_P		7	RD+	TD+	10	TD_P	
RD_N		6	RD-	TD-	11	TD_N	

NC7SZ86_U BUFFER UX05: 1 → 4, RB105 30, RB84 DNP, RB113 DNP

NC7SZ86_U BUFFER UX10: 1 → 4, RB119 30

RX_CLK, TX_CLK

SYM_1

J01

CB32 .1UF

RB22 54.9	RD_P	1	P1
CB60 .1UF		4	P4
RB23 54.9	RD_N	2	P2
V3_3			
RB24 49.9	TD_P	3	P3
		5	P5
RB25 49.9	TD_N	6	P6
CB299 .1UF		8	P8

SH1 9 CHASSIS

J1, J2, J3, J6, J4,5, J7,8

SH2 10 CHASSIS

CONN_HFJ11_2450_U

CAPS FOR XFRM CENTER TAP
SHOULD BE PLACED CLOSE TO XFRM

RESISTORS FOR TD+-/RD+-
SHOULD BE PLACED CLOSE TO PHY

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 2/2 (BLOCK) 31/71 (TOTAL)

CR-32 : @_ztop_lib\:_ztopdn_\(sch_1):page1_1B@_ztop_lib\:_z44top_dn\(sch_1):page1_12@_ztop_lib\:_z44anflan_dn\(sch_1):page5_191@_ztop_lib\:_mii_wan_dn\(sch_1):Page1

COMPONETS FOR
C1 AND RBIAS MUST
BE PLACED CLOSE TO PIN

C1PIN

C37 10UF
C103 0.1UF

R05 10.0K RBIAS

26C3^ MII_CLK
26C3^ RESET_B

U05
DP83847_U1
CONTROL

RESERVED2
RESERVED1
C1
RBIAS
X1
RESET*
X2
RESERVED10
RESERVED11
RESERVED12
RESERVED13
RESERVED14
RESERVED15
RESERVED16
RESERVED17
RESERVED18

RESERVED3
RESERVED4
RESERVED5
RESERVED6
RESERVED7
RESERVED8
RESERVED9
VDD/IO_VDD1
VDD/IO_VDD2
VDD/ANA_VDD
VDD1
VDD2
VDD3
GND1
GND2
GND3
GND4
GND5

AN_V3_3
V3_3

MDC R117 30 MDC IN 26C3^
MDIO MDIO IO
LED_DPLX/PHYAD0 LED_DPLX_ADD0 IO
LED_COL/PHYAD1 LED_COL_ADD1 IO
LED_GDLNK/PHYAD2 LED_GDLINK_ADD2 IO
LED_TX/PHYAD3 LED_TX_ADD3 IO
LED_RX/PHYAD4 LED_RX_ADD4 IO
LED_SPEED TP04
AN_EN RB38 5.1K AN_EN
AN_1 RB31 5.1K AN1
AN_0 RB16 5.1K AN0

LEDS NEED TO BE ATTACHED
OUTSIDE OF MODULE DUE TO
STRAP ADAPTING OPTION OF DP83847

V3_3
JP03 JP06 JP11

J20
RXD0 RXD1 RXD2 RXD3
RXDV RX_CRS COL_DET RX_ERR RX_CLK
CONN_10P

J19
TX_CLK TX_EN
TXD3 TXD2 TXD1 TXD0
CONN_10P

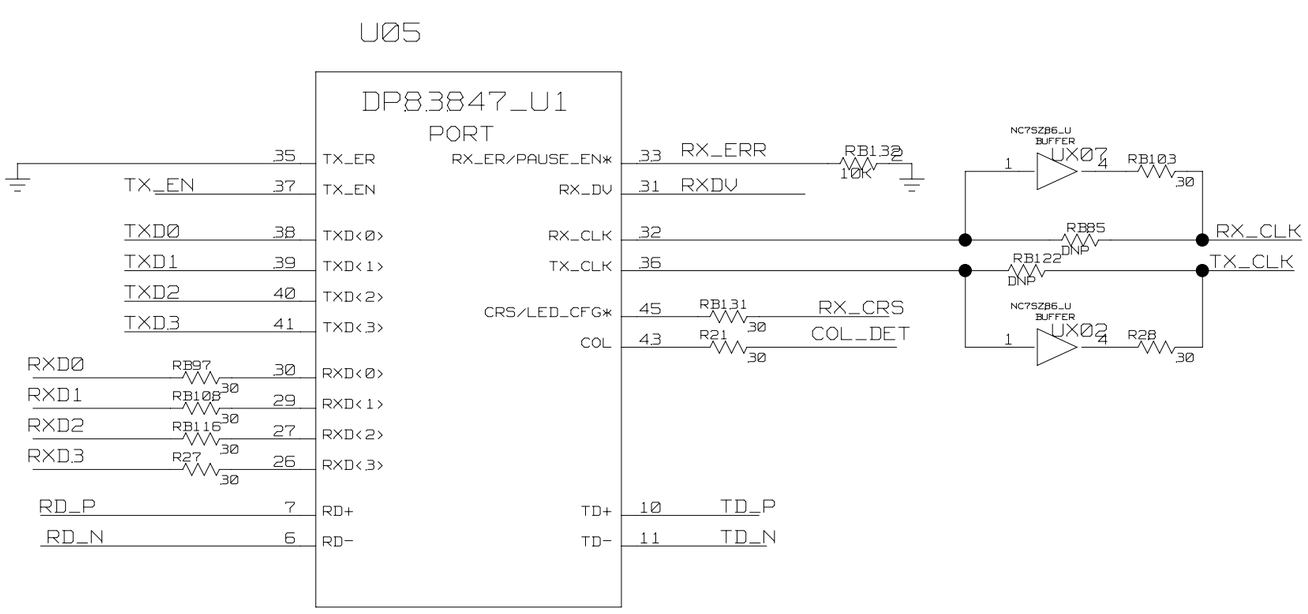
1000100MZH
L06
AN_V3_3

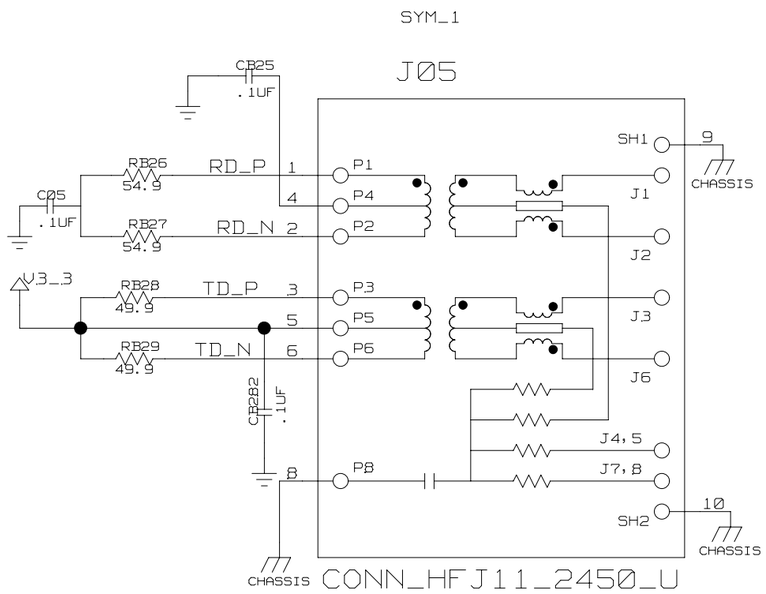
PLACEMENT NOTE:
TESTPOINTS (SHOWN ABOVE) MUST BE PLACED THE SAME FOR EACH PORT TO
ALLOW USE OF A DIFFERENT PHY CARD IF DESIRED. PLACEMENT SHOULD ALLOW
0.2 BETWEEN CONNECTORS.

ON Z44 CARD ALL 4 PORTS MUST BE PLACED WITH EQUAL SPACING AND A COMMON CENTER LINE

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 1/2(BLOCK) 32/71(TOTAL)

CR-33 : @_ztop_lib\._ztopdn_\(sch_1):page1_1B@_ztop_lib\._z44top_dn\(sch_1):page1_12@_ztop_lib\._z44andlan_dn\(sch_1):page5_191@_ztop_lib\._mii_wan_dn\(sch_1):Page2





CAPS FOR XFRM CENTER TAP
SHOULD BE PLACED CLOSE TO XFRM

RESISTORS FOR TD+-/RD+-
SHOULD BE PLACED CLOSE TO PHY

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 2/2 (BLOCK) 33/71 (TOTAL)

BLOCK NAME: _mii_wan_dn. PARENT BLOCK: _z44andlan_dn\

CR-34 : @_ztop_lib\:_ztopdn_\(sch_1):page1_1B@_ztop_lib\:_z44top_dn\(sch_1):page1_12@_ztop_lib\:_z44anflan_dn\(sch_1):page6_11@_ztop_lib\:_mii_wan_dn\(sch_1):Page1

COMPONETS FOR
C1 AND RBIAS MUST
BE PLACED CLOSE TO PIN

C1PIN

C35 2 1 10UF
C101 2 1 0.1UF

R09 10.0K RBIAS

27C3^ IN MII_CLK
27C3^ IN RESET_B

U06
DP83847_U1
CONTROL

RESERVED2
RESERVED1
C1
RBIAS
X1
RESET*
X2
RESERVED10
RESERVED11
RESERVED12
RESERVED13
RESERVED14
RESERVED15
RESERVED16
RESERVED17
RESERVED18

RESERVED3
RESERVED4
RESERVED5
RESERVED6
RESERVED7
RESERVED8
RESERVED9
VDD/IO_VDD1
VDD/IO_VDD2
VDD/ANA_VDD
VDD1
VDD2
VDD3
GND1
GND2
GND3
GND4
GND5

AN_V3_3
V3_3

MDC 25 R102 30 MDC IN 27C3^
MDIO 24 MDIO IO
LED_DPLX/PHYAD0 23 LED_DPLX_ADD0 IO
LED_COL/PHYAD1 22 LED_COL_ADD1 IO
LED_GDLNK/PHYAD2 21 LED_GDLINK_ADD2 IO
LED_TX/PHYAD3 20 LED_TX_ADD3 IO
LED_RX/PHYAD4 19 LED_RX_ADD4 IO
LED_SPEED 18 TP01
AN_EN 17 RB41 5.1K AN_EN
AN_1 16 RB35 5.1K AN1
AN_0 15 RB17 5.1K AN0

LEDS NEED TO BE ATTACHED
OUTSIDE OF MODULE DUE TO
STRAP ADAPTING OPTION OF DP83847

V3_3
JP04 JP08 JP13

J22
CONN_10P

35B8< 27D2^ OUT RXD0 1 2 RXDV OUT 27D4^ 35C4<
35B8< 27D2^ OUT RXD1 3 4 RX_CRS OUT 27C2^ 35C5<
V3_3 5 6 COL_DET OUT 27C2^ 35B5<
35B8< 27D2^ OUT RXD2 7 8 RX_ERR OUT 35C6<> 27C2^
35B8< 27D2^ OUT RXD3 9 10 RX_CLK OUT

J21
CONN_10P

27D4^ 35C4< OUT TX_CLK 1 2 TXD3 IN 27D4^ 35C8<
3 4 TXD2 IN V3_3 27D4^ 35C8<
5 6
27C4^ 35C8< IN TX_EN 7 8 TXD1 IN 27D4^ 35C8<
9 10 TXD0 IN 27D4^ 35C8<

1000100MZH

V3_3
L05
AN_V3_3
C167 2 1 0.1UF
C171 2 1 0.1UF
C174 2 1 0.1UF
C174 2 1 0.1UF
C196 2 1 0.1UF
C283 2 1 0.1UF
C357 2 1 10UF
C364 2 1 10UF
C128 2 1 10UF
C11 2 1 10UF
C238 2 1 0.1UF
C251 2 1 0.1UF

PLACEMENT NOTE:
TESTPOINTS (SHOWN ABOVE) MUST BE PLACED THE SAME FOR EACH PORT TO
ALLOW USE OF A DIFFERENT PHY CARD IF DESIRED. PLACEMENT SHOULD ALLOW
0.2 BETWEEN CONNECTORS.

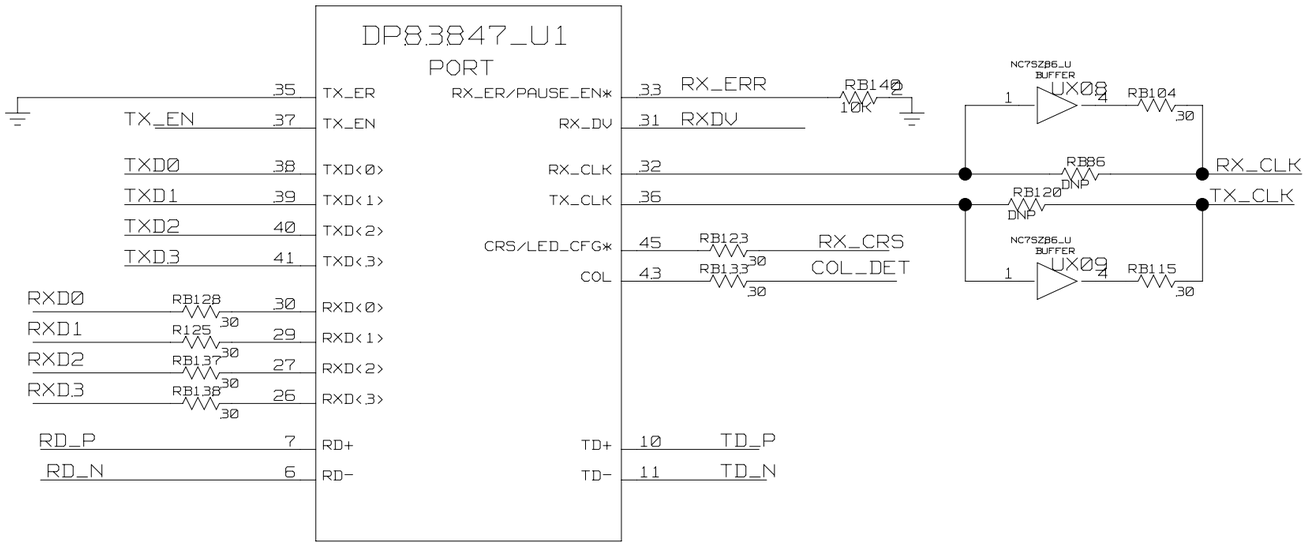
ON Z44 CARD ALL 4 PORTS MUST BE PLACED WITH EQUAL SPACING AND A COMMON CENTER LINE

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 1/2(BLOCK) 34/71(TOTAL)

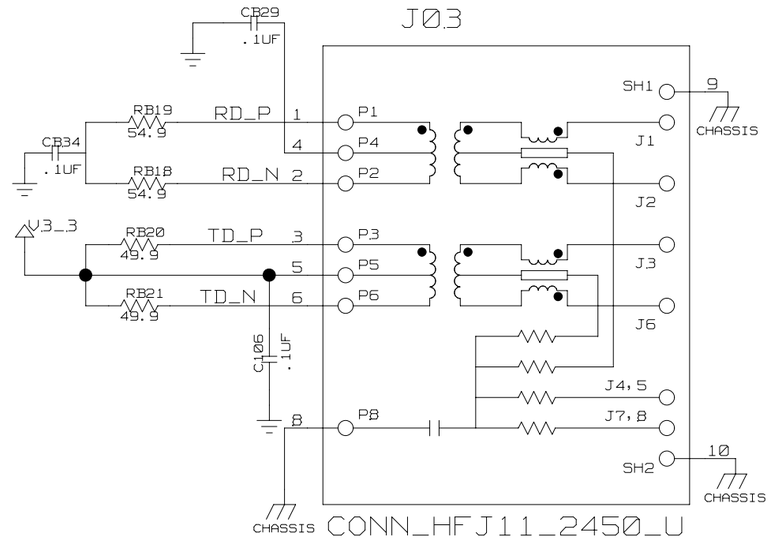
BLOCK NAME: _mii_wan_dn. PARENT BLOCK: _z44anflan_dn\

PRINTED Fri Oct 20 11:07:00 2006

U06



SYM_1



CAPS FOR XFRM CENTER TAP
SHOULD BE PLACED CLOSE TO XFRM

RESISTORS FOR TD+-/RD+-
SHOULD BE PLACED CLOSE TO PHY

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 2/2 (BLOCK) 35/71 (TOTAL)

CR-36 : @_ztop_lib\._ztopdn_\(sch_1):page1_1B@_ztop_lib\._z44top_dn\(sch_1):page1_12@_ztop_lib\._z44anflan_dn\(sch_1):page6_134@_ztop_lib\._mii_wan_dn\(sch_1):Page1

COMPONETS FOR
C1 AND RBIAS MUST
BE PLACED CLOSE TO PIN

C1PIN

C34 1 2 10UF
C28 1 2 0.1UF

R11 10.0K RBIAS

27C6^ IN MII_CLK
27C7^ IN RESET_B

U03
DP83847_U1
CONTROL

RESERVED2
RESERVED1
C1
RBIAS
X1
RESET*
X2
RESERVED10
RESERVED11
RESERVED12
RESERVED13
RESERVED14
RESERVED15
RESERVED16
RESERVED17
RESERVED18
RESERVED3
RESERVED4
RESERVED5
RESERVED6
RESERVED7
RESERVED8
RESERVED9
VDD/IO_VDD1
VDD/IO_VDD2
VDD/ANA_VDD
VDD1
VDD2
VDD3
GND1
GND2
GND3
GND4
GND5

AN_V3_3
V3_3

MDC 25 R26 30 MDC IN 27C6^
MDIO 24 MDIO IO
LED_DPLX/PHYAD0 23 LED_DPLX_ADD0 IO
LED_COL/PHYAD1 22 LED_COL_ADD1 IO
LED_GDLNK/PHYAD2 21 LED_GDLINK_ADD2 IO
LED_TX/PHYAD3 20 LED_TX_ADD3 IO
LED_RX/PHYAD4 19 LED_RX_ADD4 IO
LED_SPEED 18 TP05
AN_EN 17 RB01 5.1K AN_EN
AN_1 16 RB03 5.1K AN1
AN_0 15 RB50 5.1K AN0

LEDS NEED TO BE ATTACHED
OUTSIDE OF MODULE DUE TO
STRAP ADAPTING OPTION OF DP83847

V3_3
JP02 JP05 JP10

J18

RXD0 RXD1 RXD2 RXD3 RXDV RX_CRS COL_DET RX_ERR RX_CLK
CONN_10P

J17

TX_CLK TX_EN TXD3 TXD2 TXD1 TXD0
CONN_10P

1000100MZH

L07
AN_V3_3
C325 C326 C17 C24 C29 CR75 CR20 CR70 CR64 C31 CR83 CR77
0.1UF 10UF

PLACEMENT NOTE:
TESTPOINTS (SHOWN ABOVE) MUST BE PLACED THE SAME FOR EACH PORT TO
ALLOW USE OF A DIFFERENT PHY CARD IF DESIRED. PLACEMENT SHOULD ALLOW
0.2 BETWEEN CONNECTORS.

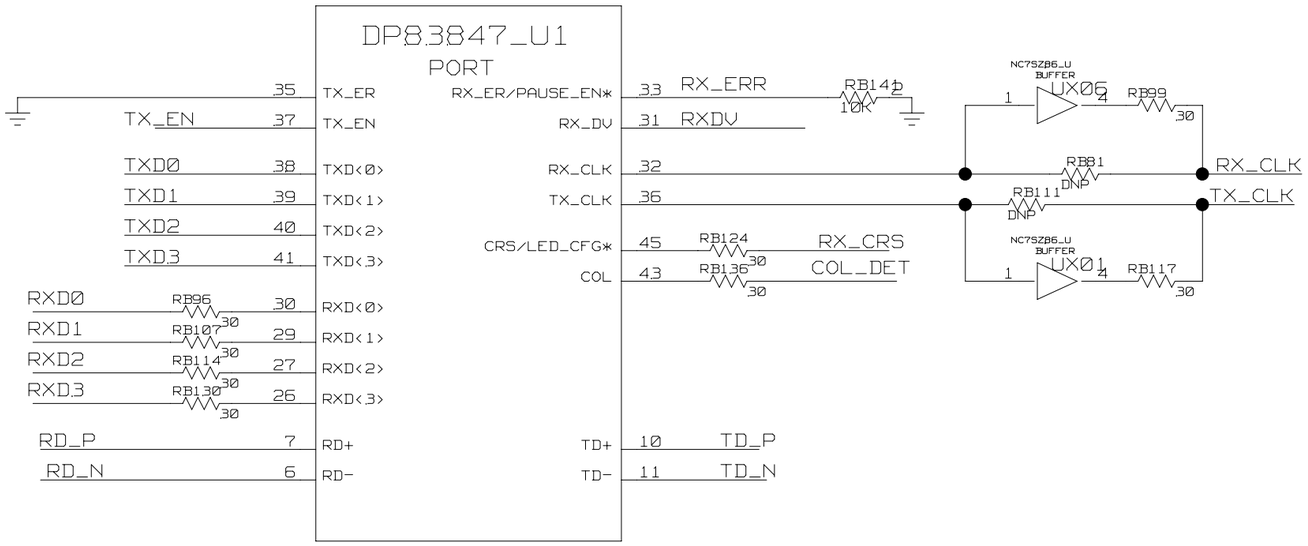
ON Z44 CARD ALL 4 PORTS MUST BE PLACED WITH EQUAL SPACING AND A COMMON CENTER LINE

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 1/2(BLOCK) 36/71(TOTAL)

BLOCK NAME: _mii_wan_dn. PARENT BLOCK: _z44anflan_dn\

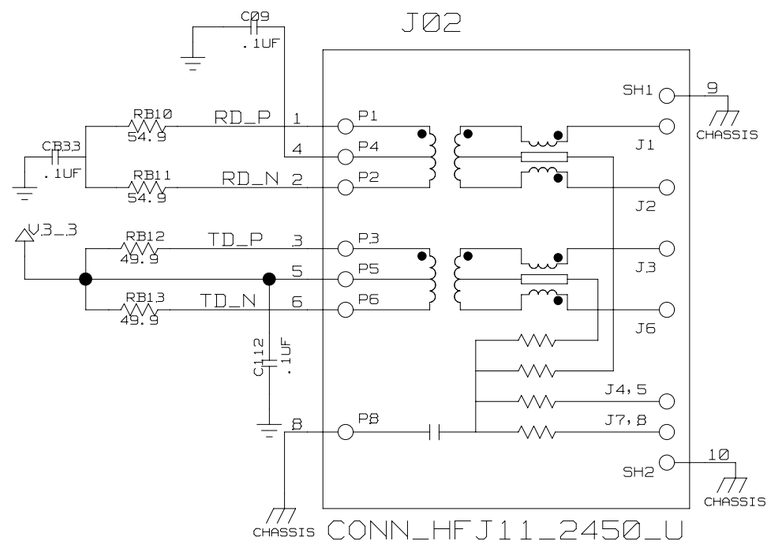
PRINTED Fri Oct 20 11:07:00 2006

U03



SYM_1

J02



CAPS FOR XFRM CENTER TAP
SHOULD BE PLACED CLOSE TO XFRM

RESISTORS FOR TD+-/RD+-
SHOULD BE PLACED CLOSE TO PHY

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 2/2 (BLOCK) 37/71 (TOTAL)

TQFP
NZA
MMC2107

I69

U19

88 TIM_16H_8L
96 EB3
98 EB2
100 EB1
101 EB0
104 PQB3
105 PQB2
106 PQB1
107 PQB0
108 PQA4
109 PQA3
110 PQA1
111 PQA0
133 ONCE_TDI
135 2107_TDO

INT6* EB3* EB2* EB1* EB0* PQB3 PQB2 PQB1 PQB0 PQA4 PQA3 PQA1 PQA0 TDI TDO

ICOC23 52 ICOC23
ICOC22 53 ICOC22
ICOC21 54 ICOC21
ICOC20 55 ICOC20
ICOC13 56 ICOC13
ICOC12 57 ICOC12
ICOC11 58 ICOC11
ICOC10 61 ICOC10

I68
GND TEST 63 TEST

SCI2_OUT 66 TXD2
SCI2_IN 68 RXD2
SCI1_OUT 69 TXD1
SCI1_IN 70 RXD1

MMC2107
CONTROL

CSE1 60 CSE1
CSE0 62 CSE0
TC2 67 TC2
TC1 78 TC1
CS3* 81 CS3
CS2* 83 CS2
CS1* 85 CS1
CS0* 86 CS0
RESET* 118 RESET_B
CLKOUT 128 CPUCLK_OUT
RSTOUT* 120 PROC_RESET_OUT
SCK 93 SCK
DE* 143 ONCE_DE_B
SS* 94 SS

INT7* INT5* INT4 INT3* INT2* INT1* INT0* YC0 MOSI MISO XTAL EXTAL TCLK TRST* TMS

89 USER_LED1
84 USER_LED2
82 INT3
79 INT4
75 RUN_KIT_USR
72 TIM_STATUS
71 INT2
80 YC0
90 MOSI
91 MISO
124 XTAL
125 OSC_MCU
130 ONCE_TCLK
142 ONCE_TRST_B
138 ONCE_TMS

SOT143
2.93V
MAX811SEUS-T
I70
UB01

I64
SW07

MAX811_U
MR* 3
GND 1
VCC 4 V3_3
RESET* 2 RESET_B

TQFP
NZA
MMC2107
I51
U19

59 RW
95 OE*
97 RCON
99 TA*
102 TEA*
92 VSTBY
113 VRH
112 VRL
87 VPP
115 VDDA
74 VDDF
103 VDDH
123 VDDSYN
141 VDD8
129 VDD7
77 VDD6
65 VDD5
45 VDD4
33 VDD3
19 VDD2
9 VDD1

RW OE* RCON TA* TEA* VRH FLASH_VPP

VDDSYN
RB159 2 0.0 1
C87 2 .1UF 1
V3_3

MMC2107
PORT

31 144 D31
30 1 D30
29 2 D29
28 3 D28
27 4 D27
26 5 D26
25 7 D25
24 10 D24
23 12 D23
22 15 D22
21 16 D21
20 17 D20
19 20 D19
18 21 D18
17 22 D17
16 25 D16
15 27 D15
14 30 D14
13 31 D13
12 34 D12
11 35 D11

A22 116 22
A21 117 21
A20 119 20
A19 121 19
A18 122 18
A17 131 17
A16 132 16
A15 134 15
A14 136 14
A13 137 13
A12 139 12
A11 6 11
A10 11 10
A9 13 9
A8 14 8
A7 23 7
A6 24 6
A5 26 5
A4 28 4
A3 29 3
A2 47 2
A1 49 1
A0 50 0

PA<22..0>

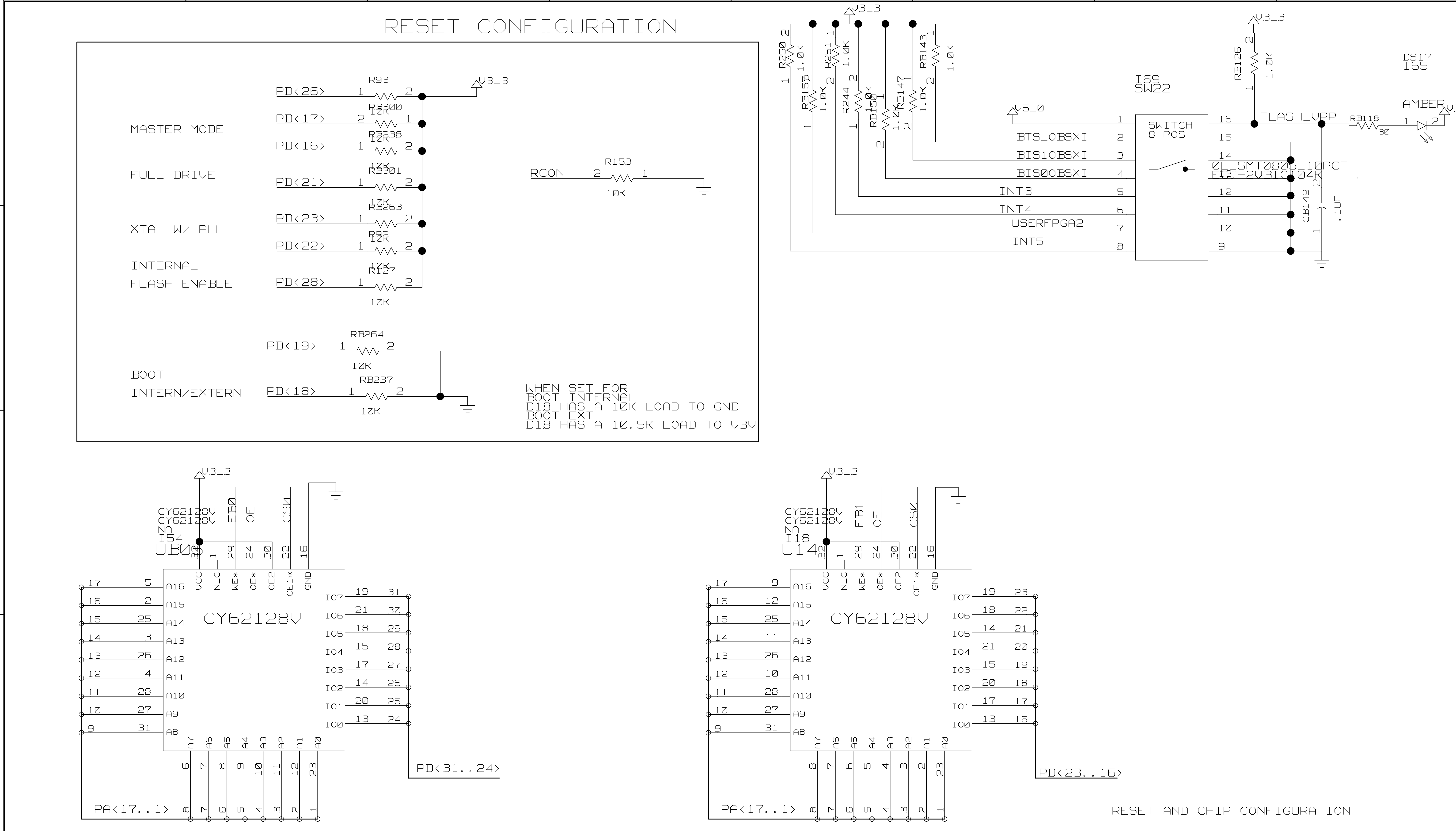
D10 36 10
D9 37 9
D8 38 8
D7 39 7
D6 40 6
D5 41 5
D4 42 4
D3 43 3
D2 45 2
D1 48 1
D0 51 0

PD<31..0>

VSSA 114
VSSF 73
VSSSYN 126
VSS8 140
VSS7 127
VSS6 76
VSS5 64
VSS4 44
VSS3 32
VSS2 18
VSS1 8

MMC2107
PROCESSOR RESOURCE CARD

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 1/7 (BLOCK) 38/71 (TOTAL)



TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 2/7 (BLOCK) 39/71 (TOTAL)

X02
I47
8.0MHZ
OSC_MCU
R90
1.0M
PLACE PADS FOR CAP
BUT DO NOT POPULATE
XTAL

V3_3
R10B 10K
R11B 10K
J41
CON14P
CON14P
NAD
I1
CON14P
ONCE_TDI
2107_TDO
ONCE_TCLK
RESET_B
ALIGN KEY
ONCE_TMS
ONCE_DE_B
ONCE_TRST_B
R91
10K
I11

V5_0
C43 1UF
C47 10UF
CB114
C39 1UF
R78 330
C35 68UF
U09
MAX1675
OUT
LX
GND
SHDN
FB
LBI
LBO*
REF
CB148 .1UF
I10
L09 22.0UH
C104 68UF

MAX3233E
MAX3233E
NAD
I31
UB07
MAX3233E
SCI1_OUT
SCI1_IN
PRT1_OUT
PRT1_IN
R2OUT
INVALID*
T2IN
T1IN
FORCEON
R1OUT
T1OUT
R1IN
VCC
FORCEOFF*
R2IN
T2OUT
GND
V-
C2-
C2+
C1-
C1+
V+2
V+1

SMT1206_5PCT
ERJ-8GEYJ5R6V
R107 5.6
C118 1UF
C91 1UF
CB3 1UF
CB4 1UF
CB35 1UF
CB262 1UF
CB466 1UF
CB484 1UF
CB199 1UF
VDDSYN

V3_3
RB287 10K
RB286 10K
RB200 10K
I35
J36
PRT1_OUT
PRT1_IN
CONN_DB9P

JTAG CONFIGURATION
ONCETDI PIN
MMC2107
ONCETDO PIN
TDI
...FPGA+FLASH...

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 3/7 (BLOCK) 40/71 (TOTAL)

J25

CONN_10P

SPARE_B<5..0>

BANK 1

BANK 0

BANK 2

BANK 3

U16

XC2S50_BGA

TIM_INTERUPT_IND

TIM_INTERUPT

PROC_RESET_OUT

USER_LED1

USER_LED2

CFG_DIN

PA<16..0>

PD<31..16>

X_INIT

RB193 330

R194 330

R195 330

RB145 330

DS27 RED

DS37 RED

DS40 RED

DS19 GREEN

V3_3

RED

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:4/7(BLOCK) 41/71(TOTAL)

BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _z44top_dn\

I34
CONN_THRU-HOLE
NOVALUE

J26
CONN_10P

SPARE_A<10..1>

D_DUT<7..0>

CPUCLK_OUT

BANK 5

BANK 4

BANK 6

I46
U16
XC2S50_BGA

BANK 7

XA<11..0>

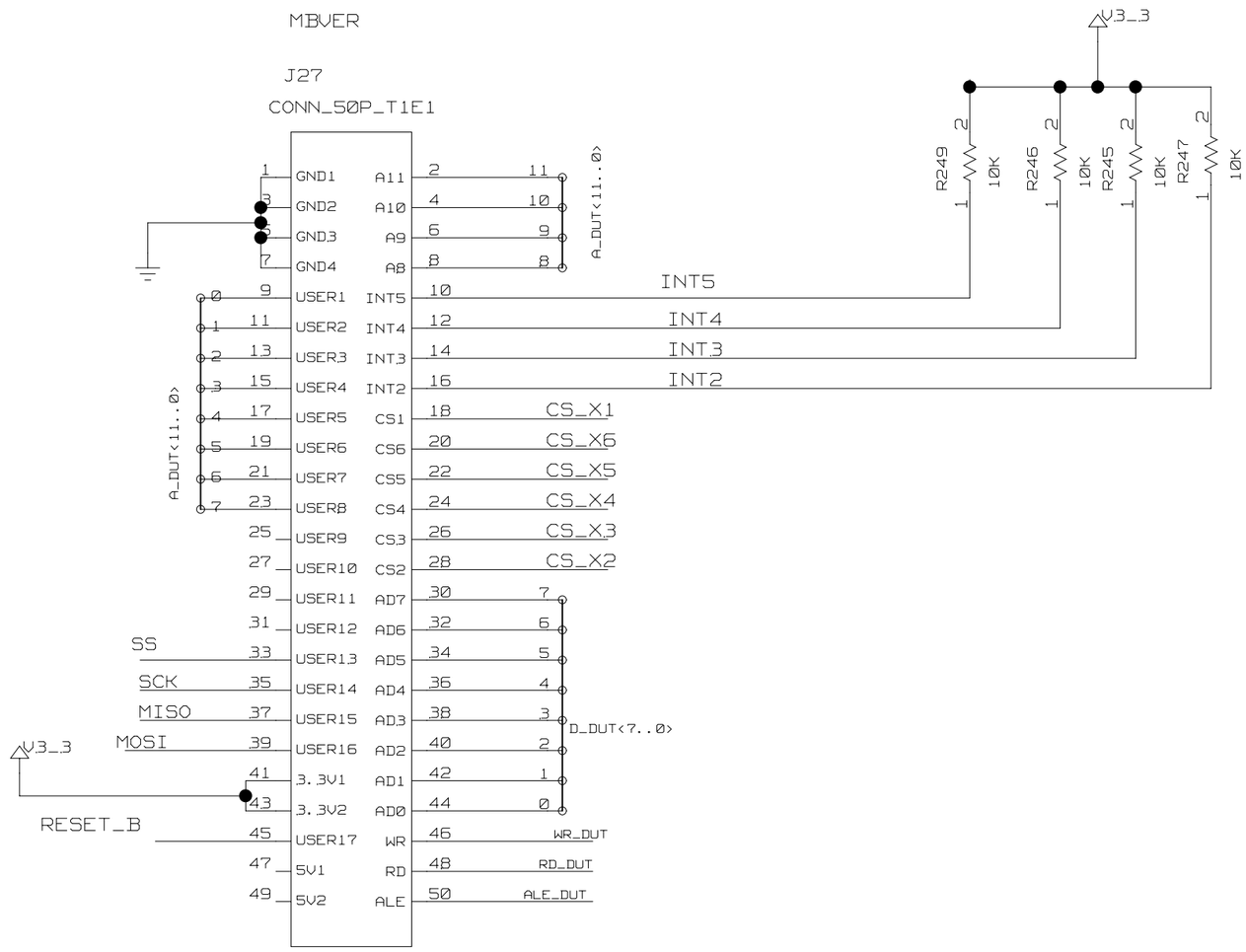
XD<7..0>

A_DUT<11..0>

BUS MODE
DETECTION (DUT AT CS_X2)

WE ALSO FUNCTIONS AS ALT_WR_RW
RW ALSO FUNCTIONS AS ALT_RD_DS

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 5/7 (BLOCK) 42/71 (TOTAL)



IN INT5 39C3<> 42A6<> 43C6<> 21C7^
IN INT4 3BA7<> 39C3<> 43C6<> 21C7^
IN INT3 3BA7<> 39D3<> 43C6<> 21C7^
IN INT2 3BA7<> 43C6<> 21C7^

RESET_B OUT 3BA4> 3BB5<> 40C3<> 21C5^ 43A7< 44B1<

IN BTS_DUT 42C3<> 21B7^
IN BIS0_DUT 42C3<> 21B7^
IN BIS1_DUT 42C3<> 21B7^

TDO_NU OUT 44A6<> 21B6^
IN TCK_NU 44A6<> 21B6^
IN TDI_NU 44A6<> 21B6^
IN TMS_NU 44A6<> 21B6^

CS_X4 OUT 42A4<> 43B6<> 21C5^
CS_X5 OUT 42A4<> 43B6<> 21C5^
CS_X1 OUT 42B3<> 43B6<> 21C5^
CS_X2 OUT 42B3<> 43B6<> 21C5^
CS_X3 OUT 42A4<> 43B6<> 21C5^
WR OUT 42B3<> 21B5^
RW_X OUT 42B3<> 21B5^
WR_DUT OUT 42C3<> 43A6<> 21B5^
RD_DUT OUT 42C3<> 43A6<> 21B7^
A_DUT<11..0> OUT 21B7^ 42A6 43B7 43C6
42B7 21B5^XA<15..0> OUT
D_DUT<7..0> IO
XD<7..0> IO

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 6/7 (BLOCK) 43/71 (TOTAL)

BLOCK NAME: _motprocrescard_dn, PARENT BLOCK: _z44top_dn\

U12

XILINX_XCF01S

UB11

MAX1792

U16

XC2S50_BGA

CONTROL

J43

CONN_10P

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 7/7 (BLOCK) 44/71 (TOTAL)

DS21458 WAN INTERFACE BLOCK

I73
2.048MHZ_3.3V
YB02
OSC
V3_3
RB160 30 MCLK 46C7<
RB184 30 MCLK2FPGA 53B6<>

U20
DS21458_U
CONTROL

JTRST K14
JTMS J15 XI_TMS 52C1< 52C8<> 52A7<>
JTCLK K16 ONCE_TCK 52C1< 52C8<> 52A7<>
JTDI C10 JTD_FLASH_TDO 52C6<>
JTDO K13 JTDO0458 52A7<>
INT* H5 WAN_INT 55D5> 46A4<> OUT
LIUC D9 LIUC 51D7<
MCLK1 H4 MCLK 46D7<
MCLK2 J12
RCLKI H9
RNEGI H10
RPOSI G8
TEST1 J14
TEST2 J13
TSTRST K15 RESET_AH 46A1<> IN
CS* M8 CS 55A4< IN
RD* A10 RD 55A2<> 54C7<> IN
WR* C9 WR 55A3<> 54C7<> IN

DVSS11 N4
DVSS12 N5
DVSS13 N6
DVSS21 D11
DVSS22 D12
DVSS23 D13

DVDD11 P4
DVDD12 P5
DVDD13 P6
DVDD21 C11
DVDD22 C12
DVDD23 C13
DVDD31 D3
DVDD32 E3
DVDD33 F3
DVDD41 L14
DVDD42 M14
DVDD43 N14
RVDD1 H1
RVDD2 J16
RVDD3 A9
RVDD4 T8
TVDD11 R6
TVDD12 T6
TVDD21 A11
TVDD22 B11
TVDD31 F1
TVDD32 F2
TVDD41 L15
TVDD42 L16

DVSS31 D4
DVSS32 E4
DVSS33 F4
DVSS41 L13
DVSS42 M13
DVSS43 N13
RVSS11 N1
RVSS12 J1
RVSS13 M1
RVSS21 E16
RVSS22 H16
RVSS23 D16
RVSS31 A5
RVSS32 A8
RVSS33 A4
RVSS41 T12
RVSS42 T13
RVSS43 T9
TVSS11 R5
TVSS12 T5
TVSS21 A12
TVSS22 B12
TVSS31 E1
TVSS32 E2
TVSS41 M15
TVSS42 M16
NC1 K9
NC2 P3
NC3 E9

C42 10UF
C48 10UF
CR236 10UF
CR126 10UF
CR154 10UF
C103 10UF
C151 10UF
CR340 10UF
CR112 10UF

CR179 1 0.1UF 2
CR144 1 0.1UF 2
CR161 1 0.1UF 2
CR160 1 0.1UF 2
CR156 1 0.1UF 2
CR120 2 0.1UF
CR204 1 0.1UF 2
CR138 1 0.1UF 2
CR155 2 0.1UF 1
CR155 2 0.1UF 1
CR127 2 0.1UF 1
CR201 1 0.1UF 2
CR201 1 0.1UF 2

ADDR<9..0> IN 54C7 55A5 55A7
A<0> H2 0
A<1> E10 1
A<2> H3 2
A<3> G4 3
A<4> N7 4
A<5> B9 5
A<6> T7 6
A<7>/ALE_A5 G2 7
A<8> H6 8
A<9> J11 9

DAT<7..0> IO 54C3 55A2 55A4
AD<0> P8 0
AD<1> D10 1
AD<2> N8 2
AD<3> P7 3
AD<4> M7 4
AD<5> R7 5
AD<6> G1 6
AD<7> G3 7

BTS B10 BTS 51C7<
MUX R8 MUX 51B7<
ESIBRD H8 ESIBRD 51C7<
ESIBS<0> J8 ESIBR0 51C7<
ESIBS<1> J9 ESIBR1 51C7<

I41
NA
NC7SZ86
NC7SZB5_U
UXB05
RESET_B 1
4 RESET_AH 46B7<
INVERTER
52B1< 55D6<>

I37
NA
NC7SZ86

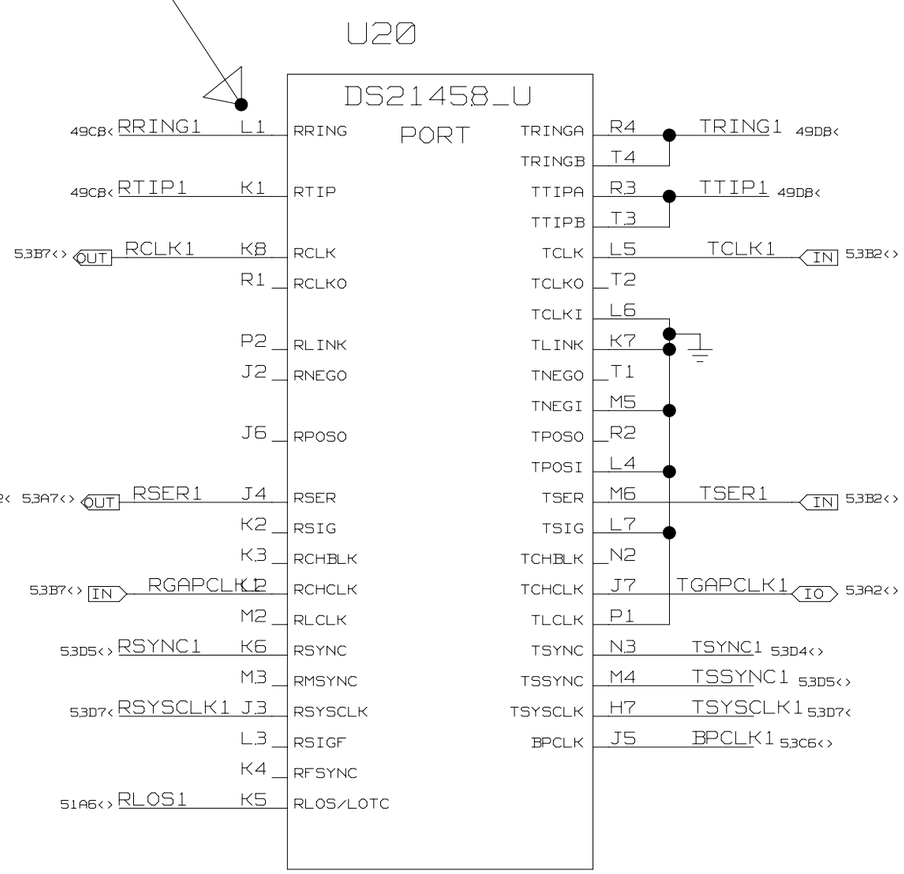
V3_3
RED
DS25
R1142 330
NC7SZB6_U
BUFFER
UX11
WAN_INT 46C7> 55D5>

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 46/71<TOTAL>

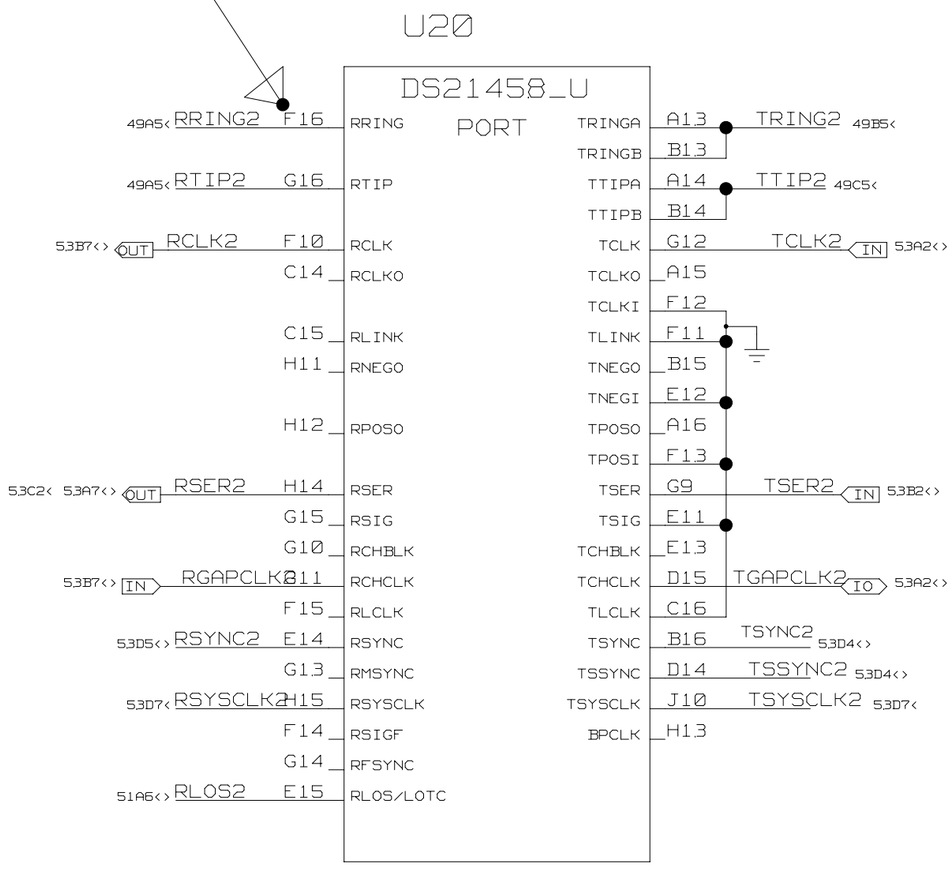
BLOCK NAME: _quadte1wan_dn. PARENT BLOCK: _wan4z44_dn\

PRINTED Fri Oct 20 11:07:03 2006

PORT1_RRING = PIN L1



PORT2_RRING = PIN F16



TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 2/10 (BLOCK) 47/71 (TOTAL)

CR-4B : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_T11@_ZTOP_LIB\._WAN4Z44_DN\(SCH_1):PAGE1_T1@_ZTOP_LIB\._QUADTE1WAN_DN\(SCH_1):PAGE3

PORT3_RRING = PIN A6

U20

DS21458_U

PORT

50C8<	RRING3	A6	RRING	TRINGA	D1	TRING3	50D8<
				TRINGB	D2		
50C8<	RTIP3	A7	RTIP	TTIPA	C1	TTIP3	50D8<
				TTIPB	C2		
53B7<> OUT	RCLK3	G5	RCLK	TCLK	F6	TCLK3 IN	53A2<>
		A2	RCLKO	TCLKO	B2		
				TCLKI	F7		
		C3	RLINK	TLINK	G7		
		F8	RNEGO	TNEGO	A1		
				TNEGI	E5		
		F9	RPOSO	TPOSO	B1		
				TPOSI	D5		
53C2< 53A7<> OUT	RSER3	C8	RSER	TSER	G6	TSER3 IN	53B2<>
		B7	RSIG	TSIG	F5		
		C7	RCHBLK	TCHBLK	C5		
53B7<> IN	RGAPCLK3	D7	RCHCLK	TCHCLK	B4	TGAPCLK3 IO	53A2<>
		B6	RLCLK	TLCLK	C4		
53D4<>	RSYNC3	B5	RSYNC	TSYNC	B3	TSYNC3	53D4<>
		E6	RMSYNC	TSSYNC	A3	TSSYNC3	53D4<>
53D7<	RSYSCLK3	B8	RSYSCLK	TSYSCLK	D8	TSYSCLK3	53C7<
		E7	RSIGF	BPCLK	E8		
		C6	RFSYNC				
51A6<>	RLOS3	D6	RLOS/LOTC				

PORT4_RRING = PIN T11

U20

DS21458_U

PORT

50A5<	RRING4	T11	RRING	TRINGA	N15	TRING4	50B5<
				TRINGB	N16		
50A5<	RTIP4	T10	RTIP	TTIPA	P15	TTIP4	50C5<
				TTIPB	P16		
53B7<> OUT	RCLK4	K12	RCLK	TCLK	L9	TCLK4 IN	53A2<>
		P14	RCLKO	TCLKO	R16		
				TCLKI	L11		
		T15	RLINK	TLINK	L12		
		P10	RNEGO	TNEGO	T16		
				TNEGI	M12		
		N10	RPOSO	TPOSO	R15		
				TPOSI	L10		
53C2< 53A7<> OUT	RSER4	P9	RSER	TSER	K10	TSER4 IN	53B2<>
		R10	RSIG	TSIG	K11		
		R11	RCHBLK	TCHBLK	R13		
53B7<> IN	RGAPCLK4	M9	RCHCLK	TCHCLK	P13	TGAPCLK4 IO	53A2<>
		R12	RLCLK	TLCLK	T14		
53D4<>	RSYNC4	N12	RSYNC	TSYNC	R14	TSYNC4	53D4<>
		M10	RMSYNC	TSSYNC	M11	TSSYNC4	53D4<>
53D7<	RSYSCLK4	R9	RSYSCLK	TSYSCLK	L8	TSYSCLK4	53C7<
		N11	RSIGF	BPCLK	N9		
		P11	RFSYNC				
51A6<>	RLOS4	P12	RLOS/LOTC				

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:3/10(BLOCK) 48/71(TOTAL)

BLOCK NAME: _quadte1wan_dn. PARENT BLOCK: _wan4z44_dn\

CR-49 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_I11@_ZTOP_LIB\._WAN4Z44_DN\(SCH_1):PAGE1_I1@_ZTOP_LIB\._QUADTE1WAN_DN\(SCH_1):PAGE4

TTIP1 R2082 C176 1UF XMIT L10

TRING1 R2072

I13 RJ45_4PORT JB12 RJ45

RTIP1 RB3202 RCV

RRING1 RB3272

RB313 2.61K RB315 2.61K CB395 0.1UF

47C2 TTIP2 R2042 C173 1UF XMIT L10

47C2 TRING2 R2032

I25 RJ45_4PORT JB12 RJ45

47C4 RTIP2 RB3222 RCV

47C4 RRING2 RB3212

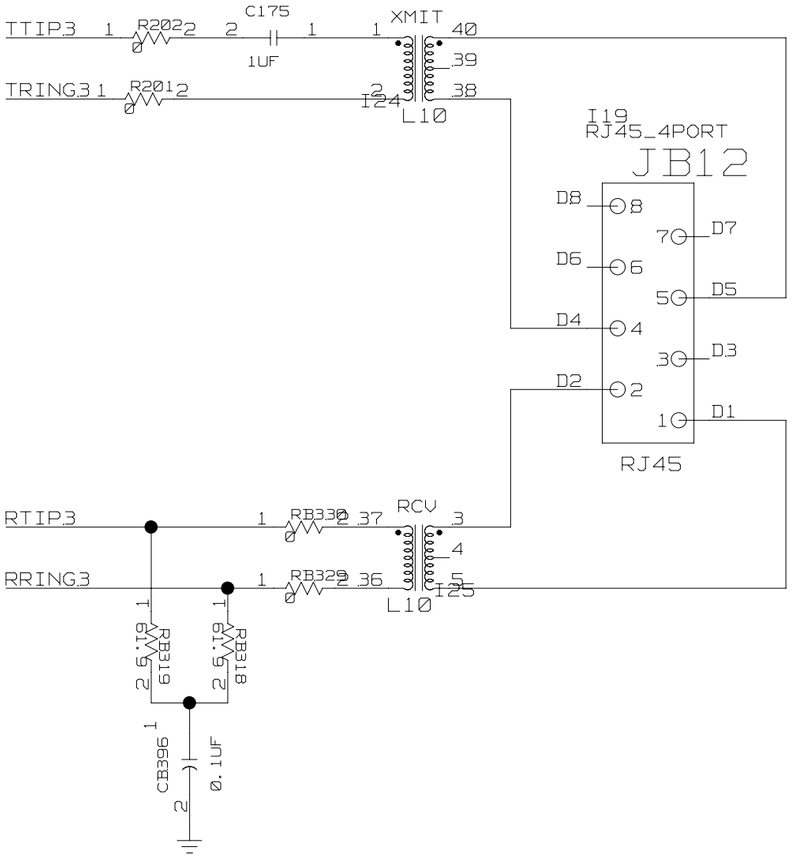
RB313 2.61K RB312 2.61K CB390 0.1UF

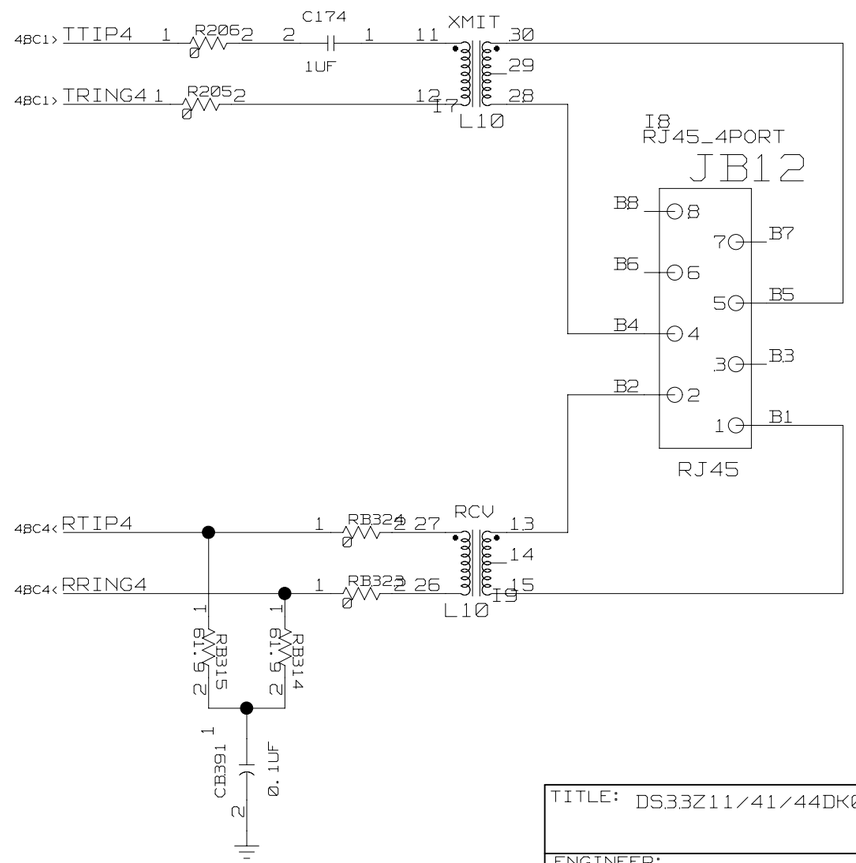
THE PCB LAYOUT INCORRECTLY USES PINS 38-40, 33-35, 28-30 AND 23-25
AS THE TX PRIMARY. THIS HAS BEEN CORRECTED IN THE SCHEMATIC,
THE PCB / ASSEMBLY HAS BEEN MODIFIED TO ACCOMMODATE THIS.

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 4/10 (BLOCK) 49/71 (TOTAL)

BLOCK NAME: _quadte1wan_dn_ PARENT BLOCK: _wan4z44_dn\

CR-50 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_I11@_ZTOP_LIB\._WAN4Z44_DN\(SCH_1):PAGE1_I1I@_ZTOP_LIB\._QUADTE1WAN_DN\(SCH_1):PAGE5





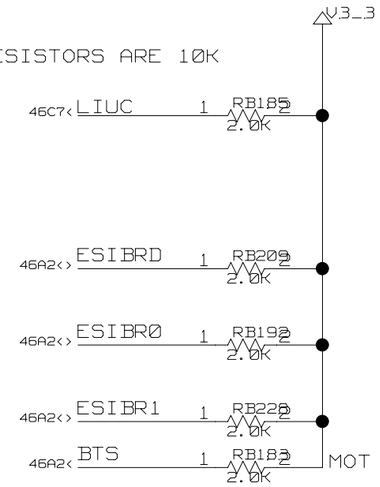
THE PCB LAYOUT INCORRECTLY USES PINS 38-40, 33-35, 28-30 AND 23-25 AS THE TX PRIMARY. THIS HAS BEEN CORRECTED IN THE SCHEMATIC, THE PCB / ASSEMBLY HAS BEEN MODIFIED TO ACCOMMODATE THIS.

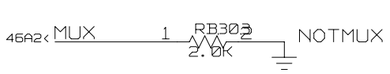
TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 5/10(BLOCK) 50/71(TOTAL)

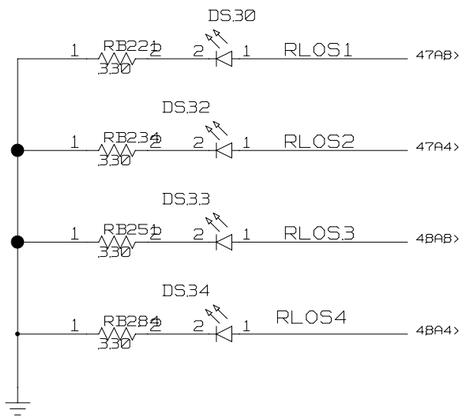
BLOCK NAME: _quadte1wan_dn, PARENT BLOCK: _wan4z44_dn\

CR-51 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_T11@_ZTOP_LIB\._WAN4Z44_DN\(SCH_1):PAGE1_T1@_ZTOP_LIB\._QUADTE1WAN_DN\(SCH_1):PAGE5

ALL UNMARKED BIAS RESISTORS ARE 10K



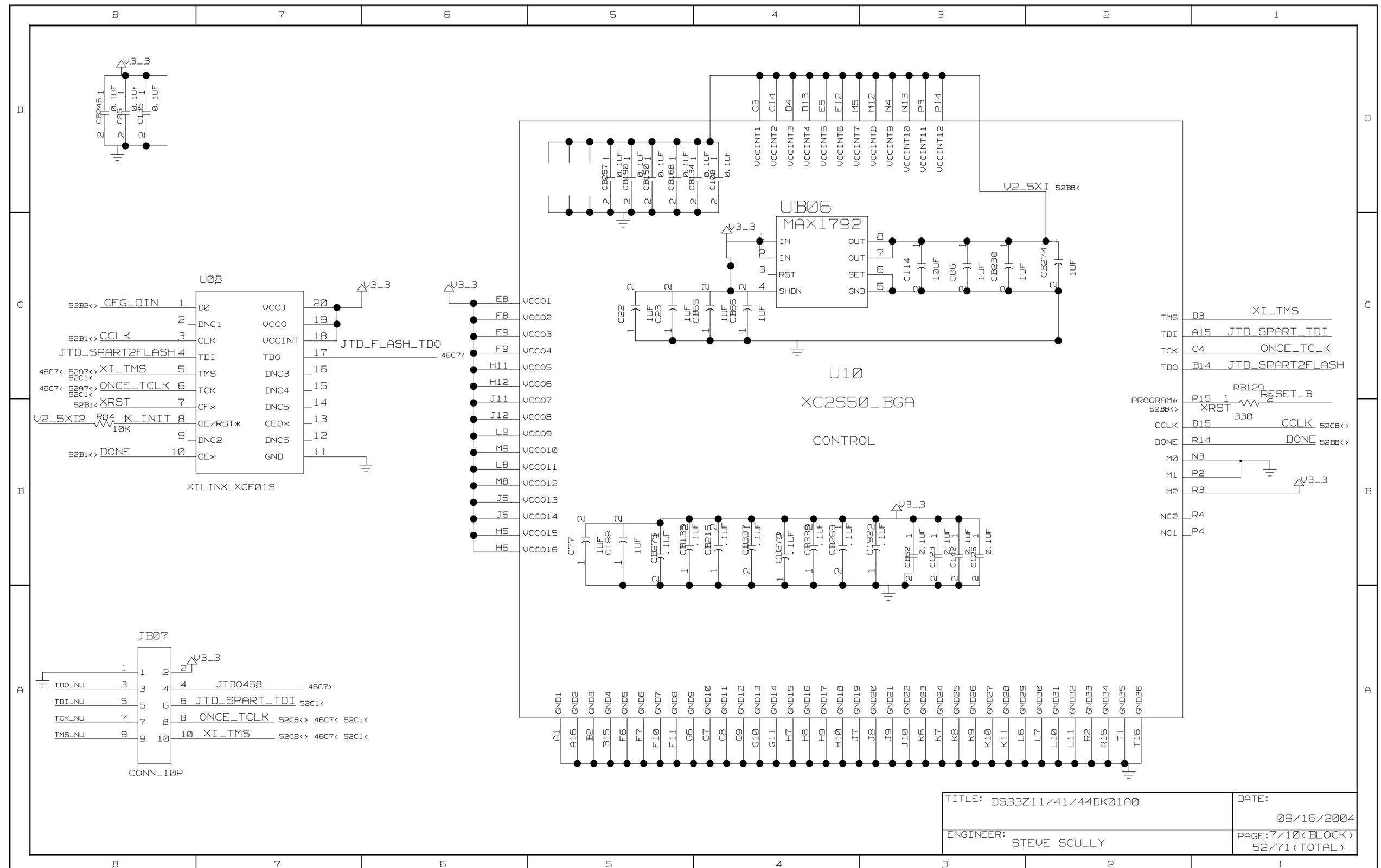




TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:6/10(BLOCK) 51/71(TOTAL)

BLOCK NAME: _quadte1wan_dn. PARENT BLOCK: _wan4z44_dn\

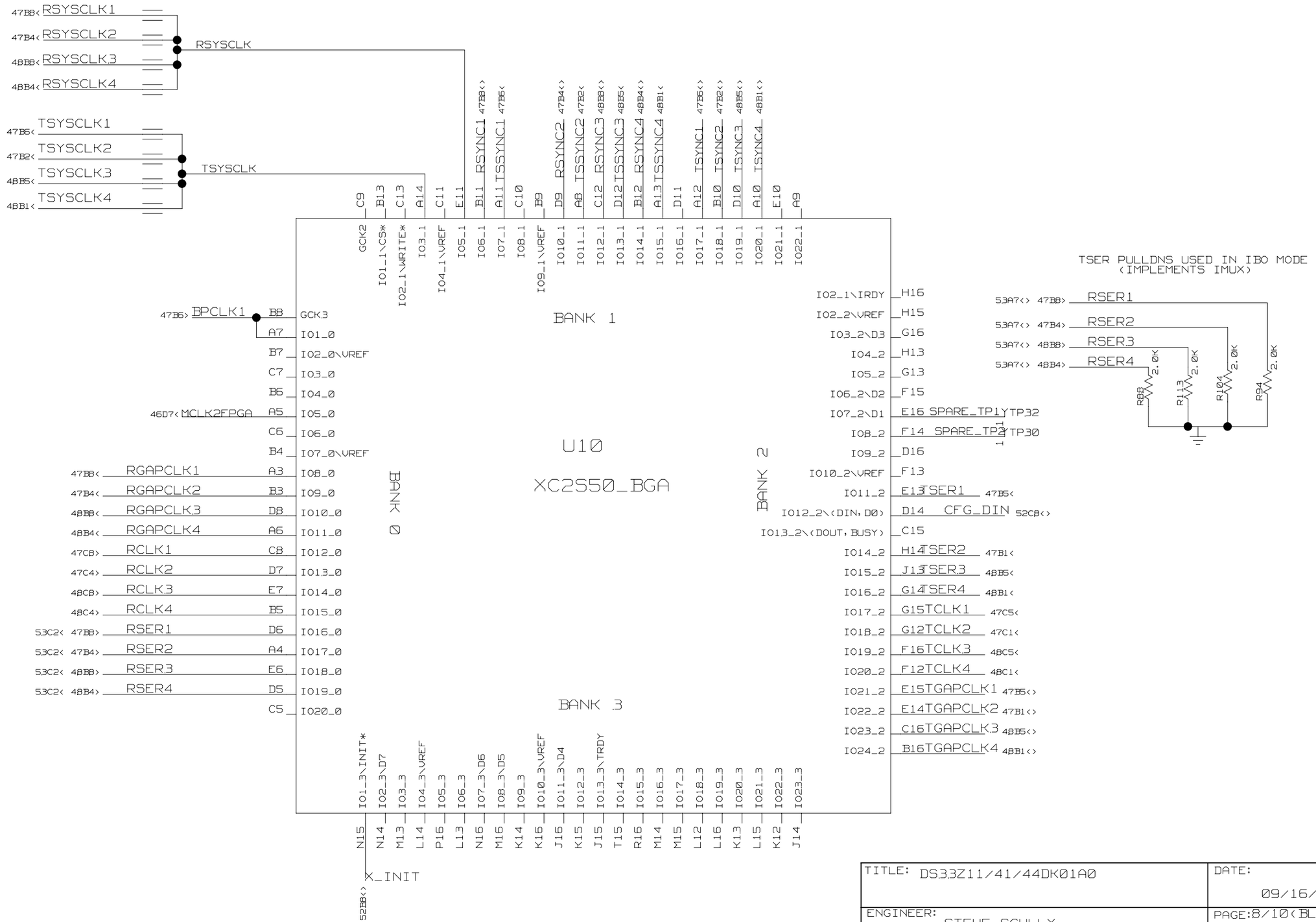
CR-52 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_T11@_ZTOP_LIB\._WAN4Z44_DN\(SCH_1):PAGE1_T1@_ZTOP_LIB\._QUADTE1WAN_DN\(SCH_1):PAGE7



TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 7/10(BLOCK) 52/71(TOTAL)

BLOCK NAME: _quadte1wan_dn, PARENT BLOCK: _wan4z44_dn\

CR-53 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_T11@_ZTOP_LIB\._WAN4Z44_DN\(SCH_1):PAGE1_T1@_ZTOP_LIB\._QUADTE1WAN_DN\(SCH_1):PAGE8



TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 8/10 (BLOCK) 53/71 (TOTAL)

BLOCK NAME: _quadte1wan_dn. PARENT BLOCK: _wan4z44_dn\

CR-54 : @_ZTOP_LIB._ZTOPDN_\(SCH_1):PAGE1_T11@_ZTOP_LIB._WAN4Z44_DN\(SCH_1):PAGE1_T1@_ZTOP_LIB._QUADTE1WAN_DN\(SCH_1):PAGE9

U10

XC2S50_BGA

BANK 5

BANK 4

BANK 6

BANK 7

ADDR<9..0>

55A7 55A5 46C2<

55D2<> CS_X4

55C6<> Z41TSYNC

55C6<> Z41RSYNC

46B7< 55A3<> WR

46B7< 55A2<> RD

55C6<> Z44_TDEN<1>

55CB<> Z44_RDEN<1>

55C6<> Z44_TCLK<1>

55CB<> Z44_RCLK<1>

55D6<> Z44_TSER<1>

55DB<> Z44_RSFR<1>

55C6<> Z44_TDEN<2>

55CB<> Z44_RDEN<2>

55C6<> Z44_TCLK<2>

55CB<> Z44_RCLK<2>

55C6<> Z44_TSER<2>

55CB<> Z44_RSFR<2>

DAT<7..0>

55A4 55A2

46B1<>

Z44_RSFR<3> 55C4<>

Z44_TSER<3> 55C1<>

Z44_RCLK<3> 55B4<>

Z44_TCLK<3> 55B1<>

Z44_RDEN<3> 55C4<>

Z44_TDEN<3> 55C1<>

Z44_RSFR<4> 55B4<>

Z44_TSER<4> 55B1<>

Z44_RCLK<4> 55B4<>

Z44_TCLK<4> 55B1<>

Z44_RDEN<4> 55B4<>

Z44_TDEN<4> 55B1<>

55D6<> 54A6<> T3ENH_T1ENLPRT1

55C6<> 54A5<> T3ENH_T1ENLPRT2

55C2<> 54A5<> T3ENH_T1ENLPRT3

55B2<> 54A5<> T3ENH_T1ENLPRT4

PORTS ARE ENABLED BY DEFAULT ON T1 BRD, AND ARE DISABLED USING JUMPERS ON T3 BRD

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:9/10(BLOCK) 54/71(TOTAL)

BLOCK NAME: _quadte1wan_dn. PARENT BLOCK: _wan4z44_dn\

CR-55 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_I11@_ZTOP_LIB\._WAN4Z44_DN\(SCH_1):PAGE1_I1@_ZTOP_LIB\._QUADTE1WAN_DN\(SCH_1):PAGE10

V3_3
V3_3
GND

RECEPTACLE
P2 CONNECTOR (RECEPTICAL)

J12

VDD

	GND	71	1		
		72	2	INT3	I28 WAN_INT 46A4<> 46C7>
	INT5	73	3		
55D6<>	INT2	74	4	GND	
	GND	75	5	INT2 55D7<>	
		76	6	RESET_B 46A2<> 52B1<	
		77	7	GND	
	V3_3	78	8	T3ENH_T1ENLPRT1	54A6<> 54AB<
54BB<	Z44_RSER<1>	79	9	Z44_TSER<1>	54BB<>
	GND	80	10	GND	
54BB<	Z44_RDEN<1>	81	11	SIG_RETURN	55A1> 55B2<> 55C6<>
		82	12	Z44_TDEN<1>	54BB<
		83	13		
	GND	84	14		
54BB<	Z44_RCLK<1>	85	15	Z44_TCLK<1>	54BB<
		86	16	GND	
	GND	87	17	Z41RSYNC	54C7<
		88	18	Z41TSYNC	54C7<
		89	19	GND	
	V3_3	90	20	T3ENH_T1ENLPRT2	
		91	21		54A5<> 54AB<
		92	22	GND	
	GND	93	23	SIG_RETURN	55A1> 55B2<> 55C6<>
54AB<	Z44_RSER<2>	94	24	Z44_TSER<2>	54BB<>
		95	25		
	GND	96	26		
54BB<	Z44_RDEN<2>	97	27	Z44_TDEN<2>	54BB<
		98	28	GND	
	GND	99	29		
54BB<	Z44_RCLK<2>	100	30	Z44_TCLK<2>	54BB<
		101	31	GND	
	V3_3	102	32		
		103	33		
		104	34	GND	
	GND	105	35		
		106	36		
	GND	107	37		
		108	38		
		109	39		
		110	40	GND	
	GND	111	41		
		112	42		
		113	43	GND	
	V3_3	114	44		
		115	45		
		116	46	GND	
	GND	117	47		
		118	48		
		119	49		
	GND	120	50		
		121	51		
		122	52	GND	
	GND	123	53	TDO_NU	52AB<>
52AB<>	TDI_NU	124	54	TCK_NU	52AB<>
52AB<>	TMS_NU	125	55	GND	
	V3_3	126	56		
		127	57		
		128	58	GND	
	GND	129	59		
		130	60		
		131	61		
	GND	132	62		
		133	63		
		134	64	GND	
	GND	135	65		
46C2< 54C7		136	66		
55A5		137	67	GND	
	V3_3	138	68		
	OSC2_NU	139	69	OSC3_NU	
	OSC4_NU	140	70	GND	

ADDR<9..0>

0		127	57		1
2		128	58	GND	
	GND	129	59		3
4		130	60		5
		131	61		
	GND	132	62		6
7		133	63		8
9		134	64	GND	

ADDR<9..0>

46C2< 54C7 55A7

55A2 54C3 46B1<>

P1 CONNECTOR (RECEPTICAL)
RECEPTACLE

J09

	GND	71	1		
CS_X5		72	2	ALE	
		73	3	CS_X4	54C7<>
	GND	74	4	GND	
		75	5		
		76	6		
	V3_3	77	7	GND	
		78	8		
		79	9		
	GND	80	10	GND	
		81	11		
		82	12		
		83	13		
	GND	84	14		
		85	15		
		86	16	GND	
	GND	87	17		
		88	18		
		89	19	GND	
	V3_3	90	20		
		91	21		
		92	22	GND	
	GND	93	23		
		94	24		
		95	25	T3ENH_T1ENLPRT3	
54B1<	Z44_RSER<3>	96	26		54A5<> 54AB<
		97	27	Z44_TSER<3>	54B1<>
	GND	98	28	GND	
54B1<	Z44_RDEN<3>	99	29		
		100	30	Z44_TDEN<3>	54B1<
	V3_3	101	31	GND	
54B1<	Z44_RCLK<3>	102	32		
		103	33	Z44_TCLK<3>	54B1<
	GND	104	34	GND	
		105	35		
		106	36		
	GND	107	37		
		108	38		
		109	39		
	GND	110	40	GND	
54B1<	Z44_RSER<4>	111	41	T3ENH_T1ENLPRT4	
		112	42		54A5<> 54AB<
		113	43	Z44_TSER<4>	54B1<>
	V3_3	114	44	GND	
54B1<	Z44_RDEN<4>	115	45		
		116	46	Z44_TDEN<4>	54A1<
	GND	117	47	GND	
54B1<	Z44_RCLK<4>	118	48	SIG_RETURN	55A1> 55C6<>
		119	49	Z44_TCLK<4>	54B1<
	GND	120	50		
		121	51		
		122	52	GND	
	GND	123	53		
		124	54		
		125	55	GND	
	V3_3	126	56		
		127	57		
		128	58	GND	
	GND	129	59		
	OSC1_NU	130	60		0
		131	61		55A4
DAT<7..0>	GND	132	62	54C3 46B1<>	1
2		133	63		3
4		134	64	GND	
	GND	135	65		5
6 I29		136	66		7
46B7< CS	CS_X2	137	67	GND	
	V3_3	138	68		
	CS_X3	139	69	RD	54C7<> 46B7<
46B7< 54C7<>	WR	140	70	GND	

DAT<7..0>

NOTE 3184 IS ON CS3 WHILE 21455 IS ON CS2/CS4

WAN R.C. CONNECTOR TO MOTHERBOARD

I27
GND SIG_RETURN

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:10/10(BLOCK) 55/71(TOTAL)

BLOCK NAME: _quadte1wan_dn. PARENT BLOCK: _wan4z44_dn\

CR-55 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_I11@_ZTOP_LIB\._WAN4Z44_DN\(SCH_1):PAGE1_I2@_ZTOP_LIB\._QUADTE3WAN_DN\(SCH_1):PAGE1

DS3184 WAN INTERFACE BLOCK

J39

V3_3

60D2< 56C7< 61D2< RB250 10K JTCLK
60C2< 56C7< 61C2< RB309 10K JTMS
56C7< JTDI
61C2< JTDOCPLD
56C7< RB308 10K JTRST

1 2 TCK_NU 62B6<> 63B6<>
3 4 TMS_NU 62B7<> 63B7<>
5 6 TDI_NU 62B7<> 63B7<>
7 8 TDO_NU 62B6<> 63B6<>
9 10

CONN_10P

V3_3

H8 H7 H6 G8 G7 G6 F8 F7 F6 A2 R8 R7 R6 P8 P7 P6 N8 N7 N6 W1 R15 R14 R13 P15 P14 P13 N15
VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9 VDD10 VDD11 VDD12 VDD13 VDD14 VDD15 VDD16 VDD17 VDD18 VDD19 VDD20 VDD21 VDD22 VDD23 VDD24 VDD25 VDD26 VDD27

UB08

DS3184

CONTROL

61D2< 60D2< 56DB<> JTCLK F3 JTCLK
61C2< 60C2< 56DB<> JTMS F4 JTMS
56DB<> JTDI J3 JTDI
60C2< JTDO84 G4 JTDO
56DB<> JTRST E4 JTRST*

60B1< 56B4< 56B8<> V3_3 CLKB J20 TSCLK
A17 TPRTY
A19 TEN
W16 TSOX
V15 TEOP
Y16 TSX
Y17 TERR

B17 TMOD<0>
B18 TMOD<1>

R20 RADR<0>
R19 RADR<1>
R18 RADR<2>
T20 RADR<3>
T19 RADR<4>

V3_3 63A5< 62A5< IN CS L3 CS*
63A3> 62A3> IN RD K3 RD*
62A4<> IN 63A4<> WR K4 WR*
R144 0.0 B1 MODE
RB224 0.0 L5 WIDTH
R145 0.0 M3 TEST*
V3_3 10K R3 HIZ*
62D6<> IN 63D6<> RESET_B GND RB228 B16 RST*

60B1< CLKA K1 CLKA
60B1< 56C7< 56B4< CLKB L1 CLKB
L2 CLKC

L17 RSOX
L16 REOP
K18 RVAL
J19 RERR
L18 RMOD<0>
L19 RMOD<1>
K2 RDY*
63D5> 62D5> 56A6<> OUT T3_INT L4 INT*

VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34 VSS35
K10 K9 K8 J10 J9 J8 M7 M6 L7 L6 K7 K6 J7 J6 A1 N10 N9 M10 M9 M8 L10 L9 L8 R12 R11 R10 R9 P12 P11 P10 P9 Y1 N12 N11 M13

ADDR<10..0> IN 62A6 62A7 63A6 63A7

A<0>/BSWAP H1 0
A<1> E1 1
A<2> H2 2
A<3> G2 3
A<4> F2 4
A<5> D2 5
A<6> H3 6
A<7> G3 7
A<8> E3 8
A<9> D3 9
A<10> C3 10
ALE N2

V3_3 R142 0.0

DAT<7..0> IO 62A3 62A5 63A3 63A5

D<0> P1 0
D<1> U1 1
D<2> P2 2
D<3> T2 3
D<4> U2 4
D<5> W2 5
D<6> N3 6
D<7> P3 7
D<8> T3
D<9> U3
D<10> V3
D<11> N4
D<12> P4
D<13> R4
D<14> T4
D<15> J5

V3_3 R15 RB222 R146 RB186 R135 RB229 RB206 R121

VALUE NOT SHOWN FOR 10K RES

TDXA<1>/TPXA K17
TDXA<2> D20
TDXA<3> E19
TDXA<4> D19
TSPA K16

RPRTY* K20
RDXA1/RPXA K19
RDXA<2> F19
RDXA<3> F18
RDXA<4> E20

REN* G18
RSCLK M20 CLKB 56B8<> 56C7< 60B1<

V3_3

DS41

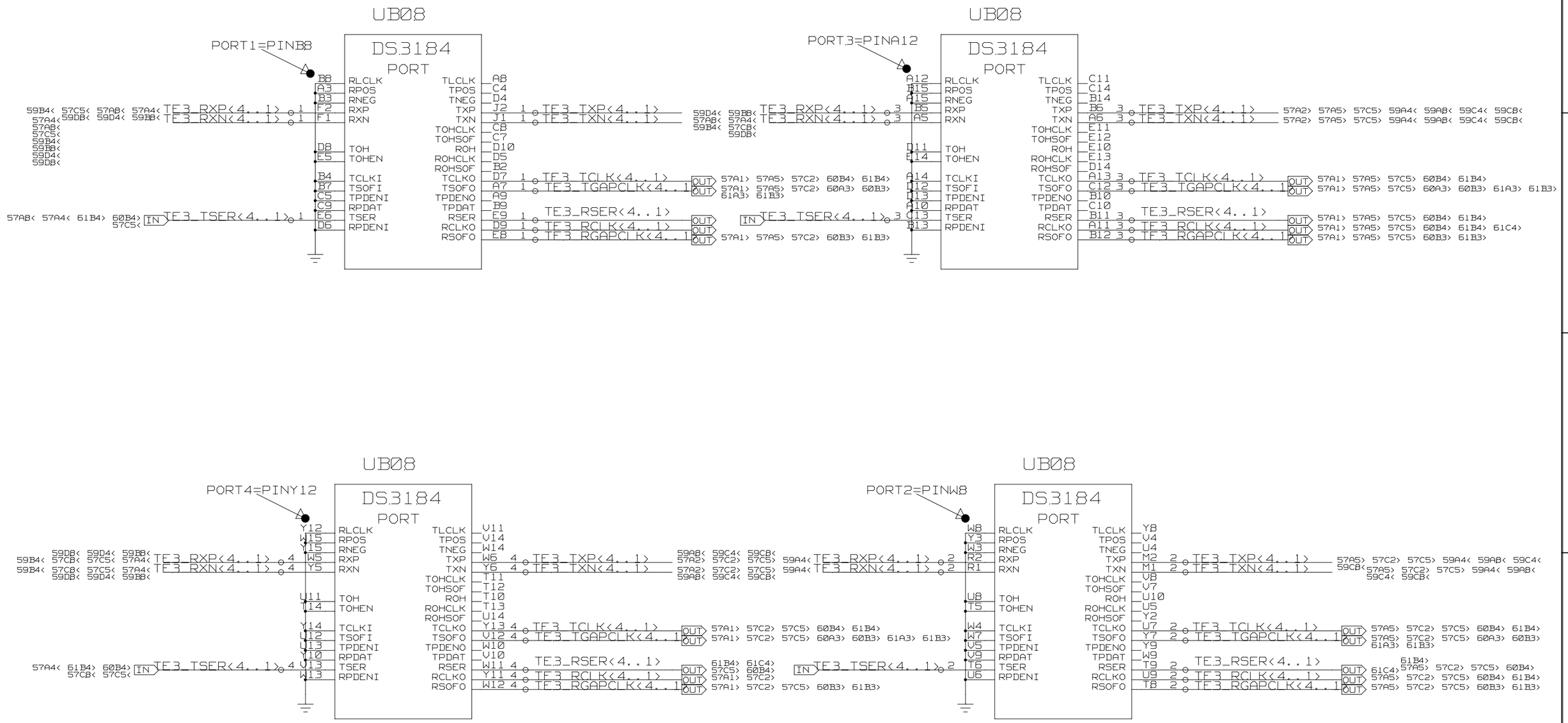
V3_3 RED RB331 330 NC7SZ86_U UX12 4 YTP66 T3_INT 56B8<> 62D5> 63D5>

TITLE: DS3,3Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:1/8(BLOCK) 56/71(TOTAL)

BLOCK NAME: _quadte3wan_dn. PARENT BLOCK: _wan4z44_dn\

PRINTED Fri Oct 20 11:07:05 2006

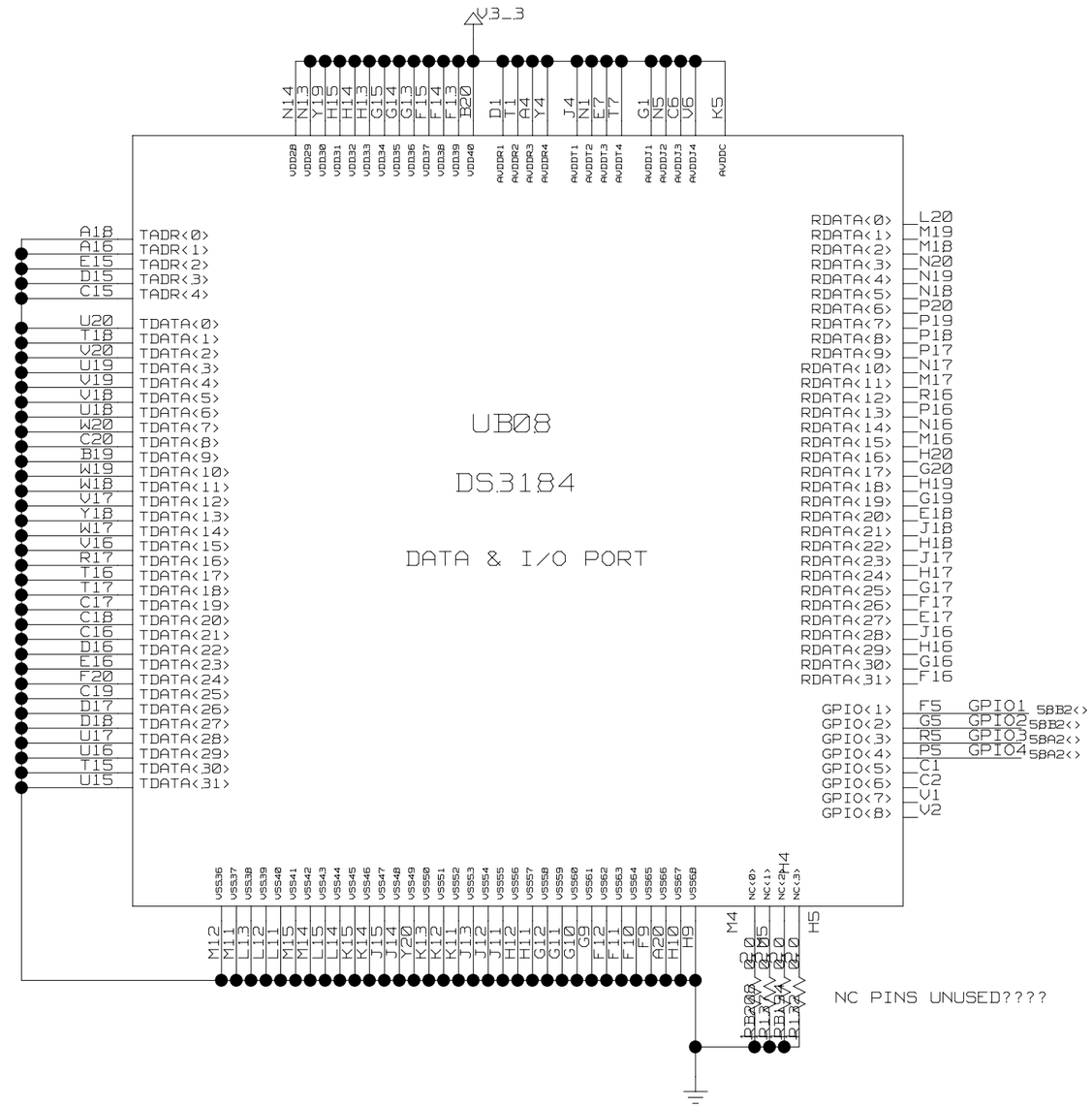
CR-57 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_I11@_ZTOP_LIB\._WAN4Z44_DN\(SCH_1):PAGE1_I2@_ZTOP_LIB\._QUADTE3WAN_DN\(SCH_1):PAGE2



TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:2/8(BLOCK) 57/71(TOTAL)

BLOCK NAME: _quadte3wan_dn. PARENT BLOCK: _wan4z44_dn\

CR-5B : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_I11@_ZTOP_LIB\._WAN4Z44_DN\(SCH_1):PAGE1_I2@_ZTOP_LIB\._QUADTE3WAN_DN\(SCH_1):PAGE3

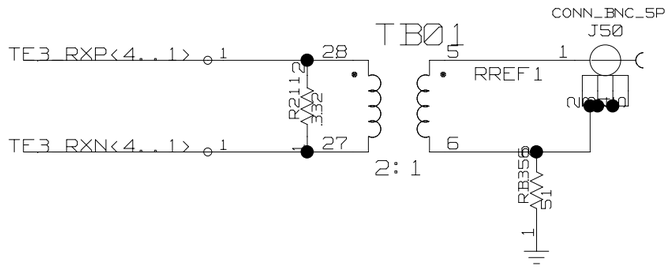


TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 3/8 (BLOCK) 58/71 (TOTAL)

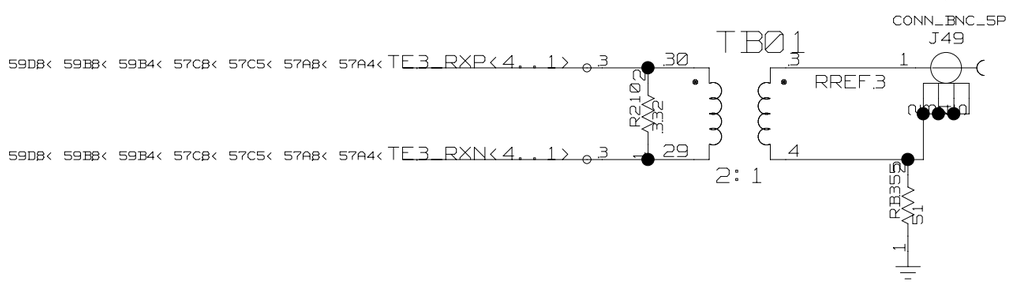
BLOCK NAME: _quadte3wan_dn, PARENT BLOCK: _wan4z44_dn\

CR-59 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_I11@_ZTOP_LIB\._WAN4Z44_DN\(SCH_1):PAGE1_I2@_ZTOP_LIB\._QUADTE3WAN_DN\(SCH_1):PAGE4

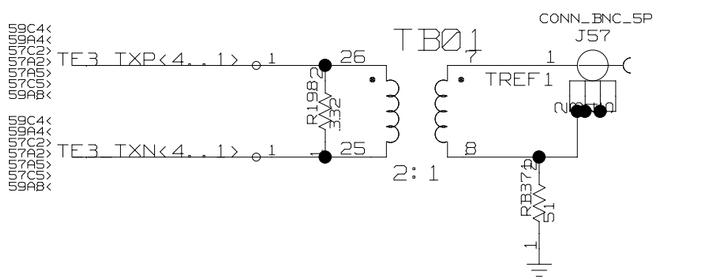
75 OHM VERT



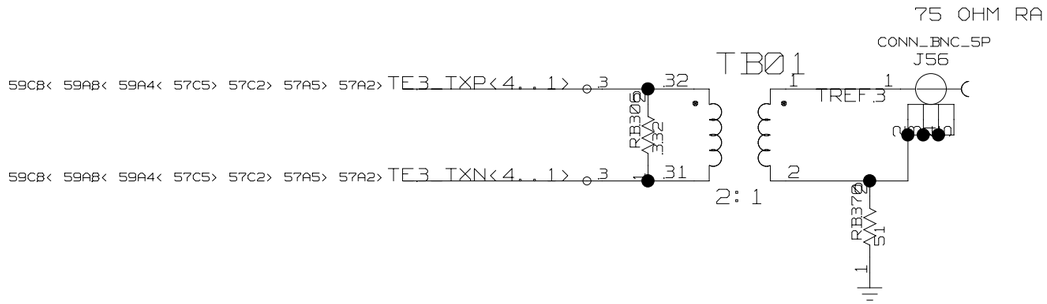
75 OHM VERT



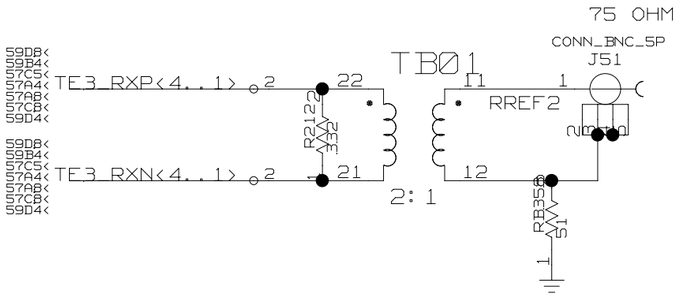
75 OHM RA



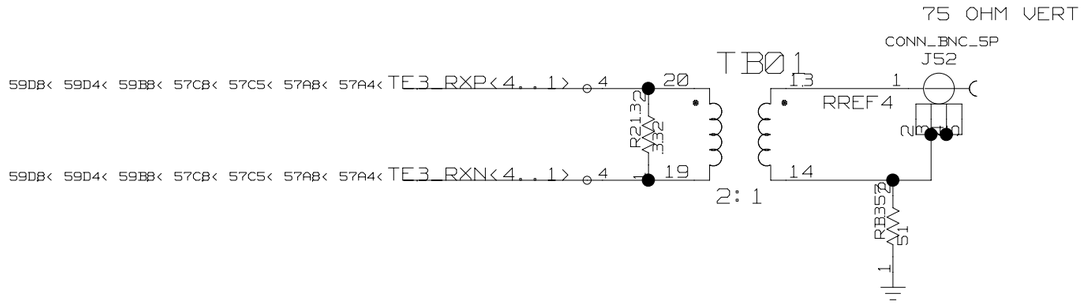
75 OHM RA



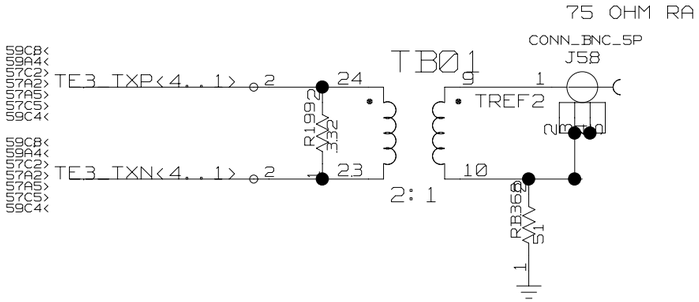
75 OHM VERT



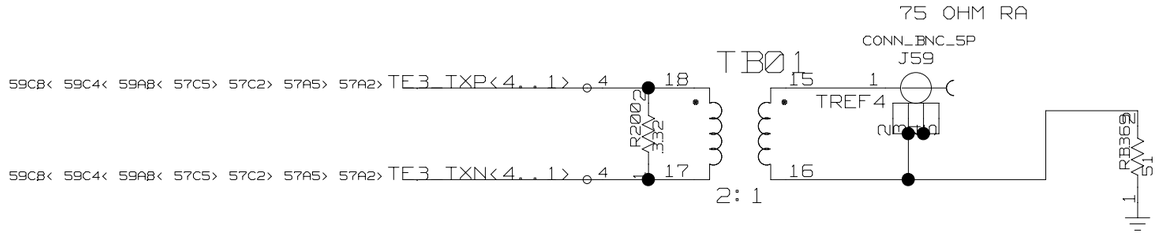
75 OHM VERT



75 OHM RA



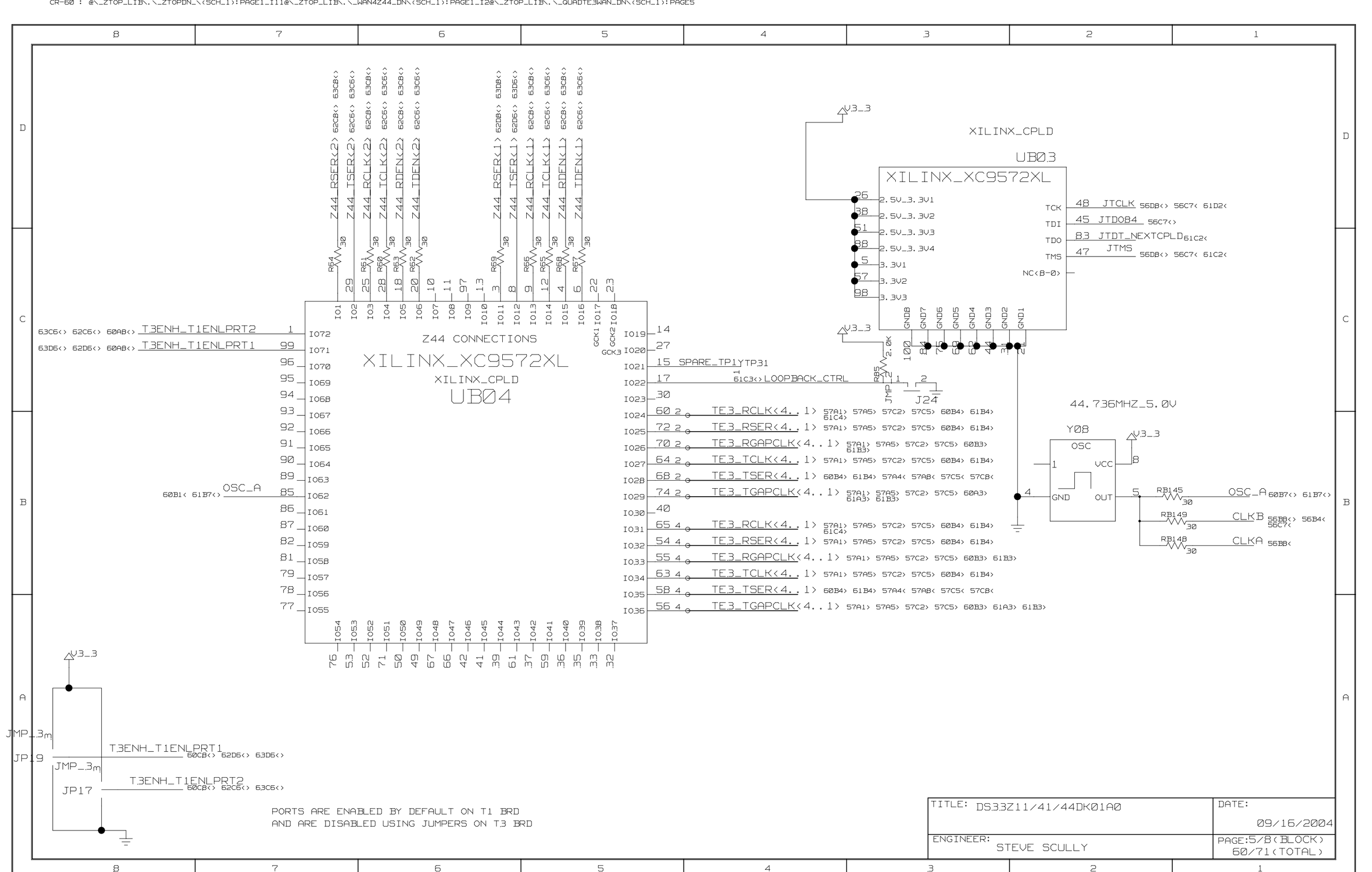
75 OHM RA



TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:4/8(BLOCK) 59/71(TOTAL)

BLOCK NAME: _quadte3wan_dn. PARENT BLOCK: _wan4z44_dn\

CR-60 : @_ZTOP_LIB\,_ZTOPDN_\(SCH_1):PAGE1_I11@_ZTOP_LIB\,_WAN4Z44_DN\(SCH_1):PAGE1_I12@_ZTOP_LIB\,_QUADTE3WAN_DN\(SCH_1):PAGE5



TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:5/8<BLOCK> 60/71<TOTAL>

BLOCK NAME: _quadte3wan_dn, PARENT BLOCK: _wan4z44_dn\

CR-61 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_I11@_ZTOP_LIB\._WAN4Z44_DN\(SCH_1):PAGE1_I12@_ZTOP_LIB\._QUADTE3WAN_DN\(SCH_1):PAGE6

Z44 CONNECTIONS

XILINX_XC9572XL

XILINX_CPLD

UB03

Z44_RSER<4> 62B2<>
Z44_RCLK<4>
Z44_TCLK<4>
Z44_RDEN<4>
Z44_TDEN<4>
Z44_TSER<4> 62B2<>
Z44_RSER<3> 62C2<>
Z44_RCLK<3>
Z44_TCLK<3>
Z44_RDEN<3>
Z44_TDEN<3>
Z44_TSER<3> 62C2<>

63B2<> 62B2<> 61A8<> T3ENH_T1ENLPRT4
63C2<> 62C2<> 61A8<> T3ENH_T1ENLPRT3
60B1< 60B7<> OSC_A

LOOPBACK_CTRL 60C4<>

TE3_RCLK<4..1> 57A1> 57A5> 57C2> 57C5> 60B4> 61B4>
TE3_RSER<4..1> 57A1> 57A5> 57C2> 57C5> 60B4> 61B4>
TE3_RGAPCLK<4..1> 57A1> 57A5> 57C2> 57C5> 60B3> 61B3>
TE3_TCLK<4..1> 57A1> 57A5> 57C2> 57C5> 60B4> 61B4>
TE3_TSER<4..1> 60B4> 61B4> 57A4< 57A8< 57C5< 57C8<
TE3_TGAPCLK<4..1> 57A1> 57A5> 57C2> 57C5> 60A3> 60B3> 61A3>
TE3_RCLK<4..1> 57A1> 57A5> 57C2> 57C5> 60B4> 61C4>
TE3_RSER<4..1> 57A1> 57A5> 57C2> 57C5> 60B4> 61B4>
TE3_RGAPCLK<4..1> 57A1> 57A5> 57C2> 57C5> 60B3> 61B3>
TE3_TCLK<4..1> 57A1> 57A5> 57C2> 57C5> 60B4> 61B4>
TE3_TSER<4..1> 60B4> 61B4> 57A4< 57A8< 57C5< 57C8<
TE3_TGAPCLK<4..1> 57A1> 57A5> 57C2> 57C5> 60A3> 60B3> 61A3>

I79 TINYTESTPOINT

SPARE_TP3

XILINX_CPLD

UB04

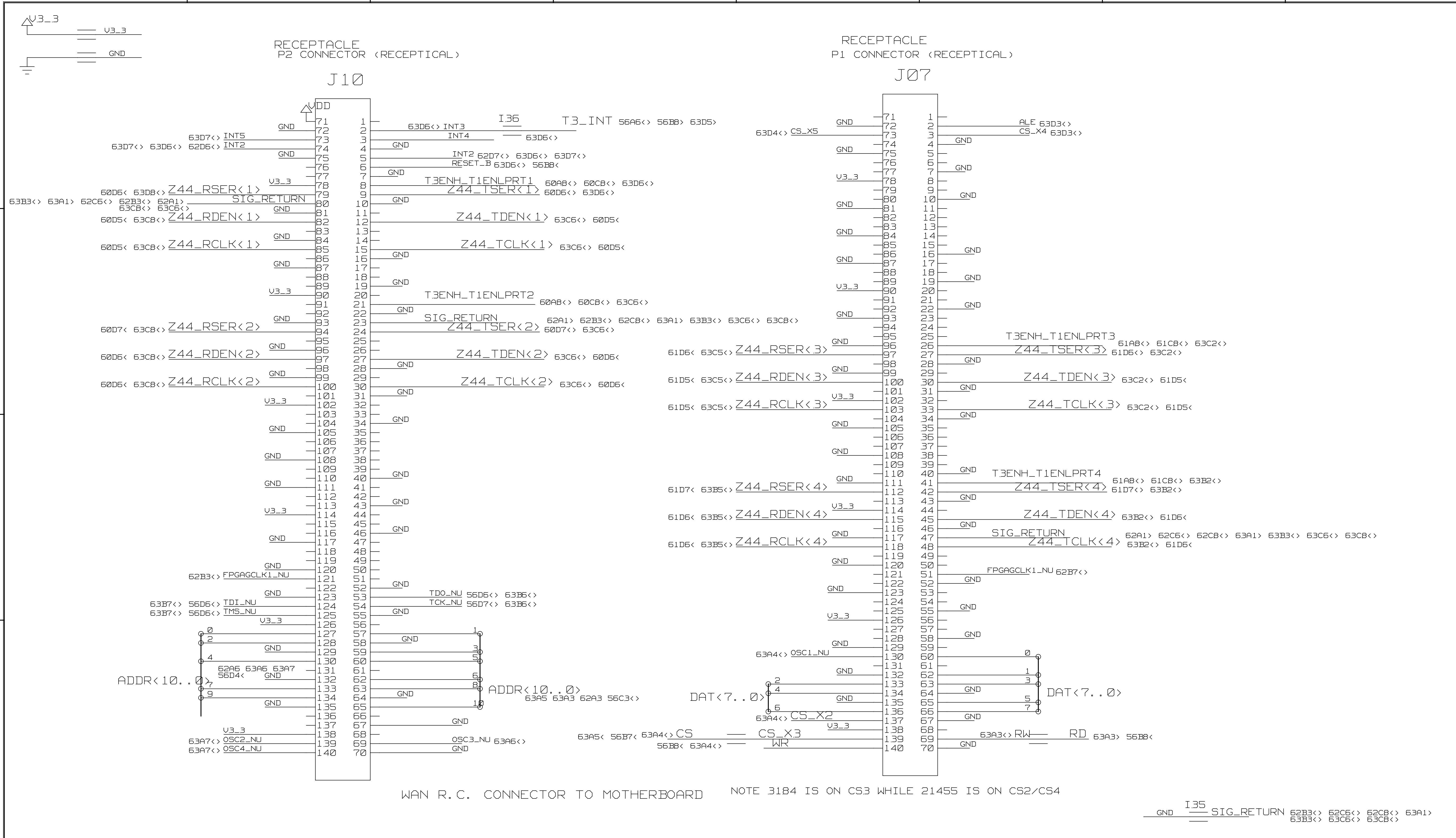
XILINX_XC9572XL

JTCLK 56D8<> 56C7< 60D2<
JTDI_NEXTCPLD 60C2<
JTDO_CPLD 56D8<>
JTMS 56D8<> 56C7< 60C2<

JMP_3M
JP18 T3ENH_T1ENLPRT3 61C8<> 62C2<> 63C2<>
JMP_3M
JP16 T3ENH_T1ENLPRT4 61C8<> 62B2<> 63B2<>

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:6/8(BLOCK) 61/71(TOTAL)

BLOCK NAME: _quadte3wan_dn. PARENT BLOCK: _wan4z44_dn\



TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 7/8(BLOCK) 62/71(TOTAL)

V3_3 I15 V3_3

I17 GND

I25
PLUG
P2 CONNECTOR (PLUG)

JB06

PLUG STYLE CONNECTORS GO ON BOTTOM OF T3E3 WAN CARD
DS21458 CONNECTS TO MOTHERBOARD BY STACKING ONTO T3E3 BRD

I8
PLUG
P1 CONNECTOR (PLUG)

JB05

VDD

I14 T3_INT 56A6<> 56B8> 62D5>

62D6<> INT3
INT4 62D6<>
INT2 62D6<> 62D7<> 63D7<>
RESET_B 62D6<> 56B8<
T3ENH_T1ENLPRT1 60A8<> 60C8<> 62D6<>
Z44_TSER<1> 60D6<> 62D6<>
Z44_TDEN<1> 62C6<> 60D5<
Z44_TCLK<1> 62C6<> 60D5<
T3ENH_T1ENLPRT2 60A8<> 60C8<> 62C6<>
SIG_RETURN 62A1> 62B3<> 62C6<> 62C8<> 63A1> 63B3<> 63C8<>
Z44_TSER<2> 60D7<> 62C6<>
Z44_TDEN<2> 62C6<> 60D6<
Z44_TCLK<2> 62C6<> 60D6<

62D7<> INT5
63D6<> 62D7<> 62D6<> INT2
60D6< 62D8<> Z44_RSER<1>
63A1> 62C8<> 62C6<> 62B3<> 62A1> SIG_RETURN
63C6<> 63B3<>
60D5< 62C8<> Z44_RDEN<1>
60D5< 62C8<> Z44_RCLK<1>
60D7< 62C8<> Z44_RSER<2>
60D6< 62C8<> Z44_RDEN<2>
60D6< 62C8<> Z44_RCLK<2>

TDO_NU 56D6<> 62B6<>
TCK_NU 56D7<> 62B6<>
62B7<> 56D6<> TDI_NU
62B7<> 56D6<> TMS_NU
62A7<> OSC2_NU
62A7<> OSC4_NU
OSC3_NU 62A6<>

ADDR<10..0>
62A6 62A7
56D4< 63A6
ADDR<10..0> 63A3 62A5 62A3 56C3<>

61D6< 62C5<> Z44_RSER<3>
61D5< 62C5<> Z44_RDEN<3>
61D5< 62C5<> Z44_RCLK<3>
61D7< 62B5<> Z44_RSER<4>
61D6< 62B5<> Z44_RDEN<4>
61D6< 62B5<> Z44_RCLK<4>

62D4<> CS_X5
ALE 62D3<>
CS_X4 62D3<>
T3ENH_T1ENLPRT3 61A8<> 61C8<> 62C2<>
Z44_TSER<3> 61D6<> 62C2<>
Z44_TDEN<3> 62C2<> 61D5<
Z44_TCLK<3> 62C2<> 61D5<
T3ENH_T1ENLPRT4 61A8<> 61C8<> 62B2<>
Z44_TSER<4> 61D7<> 62B2<>
Z44_TDEN<4> 62B2<> 61D6<
SIG_RETURN 62A1> 62B3<> 62C6<> 62C8<> 63A1> 63C6<> 63C8<>
Z44_TCLK<4> 62B2<> 61D6<

DAT<7..0>
62A4<> OSC1_NU
62A4<> CS_X2
62A5< 56B7< 62A4<> CS
56B8< 62A4<> WR
I13 CS_X3
I16 RW RD 62A3> 56B8<
62A3<>

DAT<7..0>

GND I7 SIG_RETURN 62A1> 62B3<> 62C6<> 62C8<> 63B3<> 63C6<> 63C8<>

WAN R.C. CONNECTOR TO MOTHERBOARD

NOTE 3184 IS ON CS3 WHILE 21455 IS ON CS2/CS4

TITLE: DS3_3Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 8/8 (BLOCK) 63/71 (TOTAL)

BLOCK NAME: _quadte3wan_dn. PARENT BLOCK: _wan4z44_dn\