5A Step-Down Converter with I²C Interface

General Description

The RT5735 device is a full featured 5.5V, 5A, synchronous step down constant-on-time (COT) current mode converter with two integrated MOSFETs. The RT5735 enables small designs by integrating the MOSFETs, implementing current mode control to reduce external component count, reducing inductor size by enabling up to 2.4MHz switching frequency, and minimizing the IC footprint with a small WL-CSP-20B 1.6x2 (BSC) package. The RT5735 provides accurate regulation for a variety of loads with an accurate ±1% Voltage Reference (VREF) over temperature. Efficiency is maximized through the integrated 34mΩ/18mΩ MOSFETs and 70μA typical quiescent current. Using the enable pin, shutdown supply current is less than 2μA by entering a shutdown mode.

The output voltage startup ramp is controlled by the slow start pin. An open-drain power good signal indicates the output is within 90% to 95% of its nominal voltage.

Marking Information

1ZW

1Z : Product Code
W : Date Code

Features

- **2.5V to 5.5V Input Supply Voltage**
- **Current Mode COT Control Loop Design**
- **Fast Transient Response**
- **Internal 34mΩ and 18mΩ Synchronous Rectifier**
- **Highly Accurate V_{OUT} Regulation Over Load/Line Range**
- **Robust Loop Stability with Low-ESR C_{OUT}**
- **Over-Temperature Protection**

Applications

- Distributed Power Systems
- Enterprise Servers, Ethernet Switches & Routers, and Global Storage Equipment
- Telecom & Industrial Equipment

Ordering Information

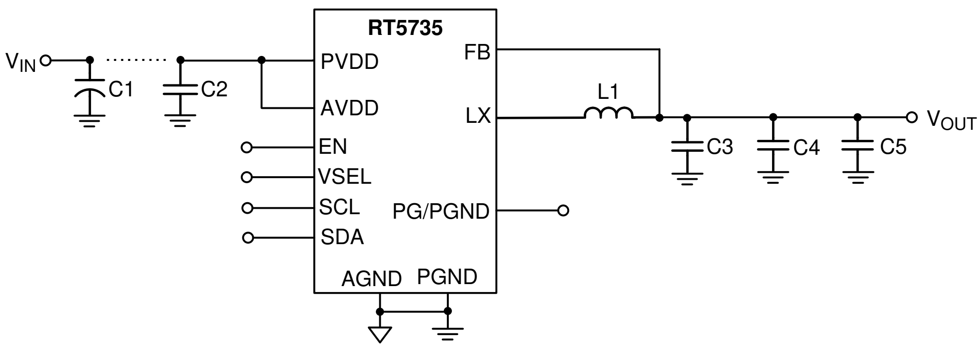
RT5735□
Package Type
WSC : WL-CSP-20B 1.6x2 (BSC)

Note :

Richtek products are :

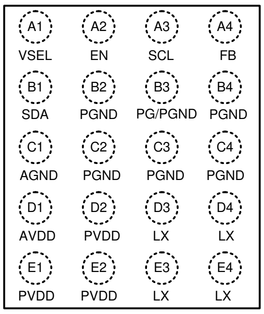
- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Simplified Application Circuit



Pin Configurations

(TOP VIEW)

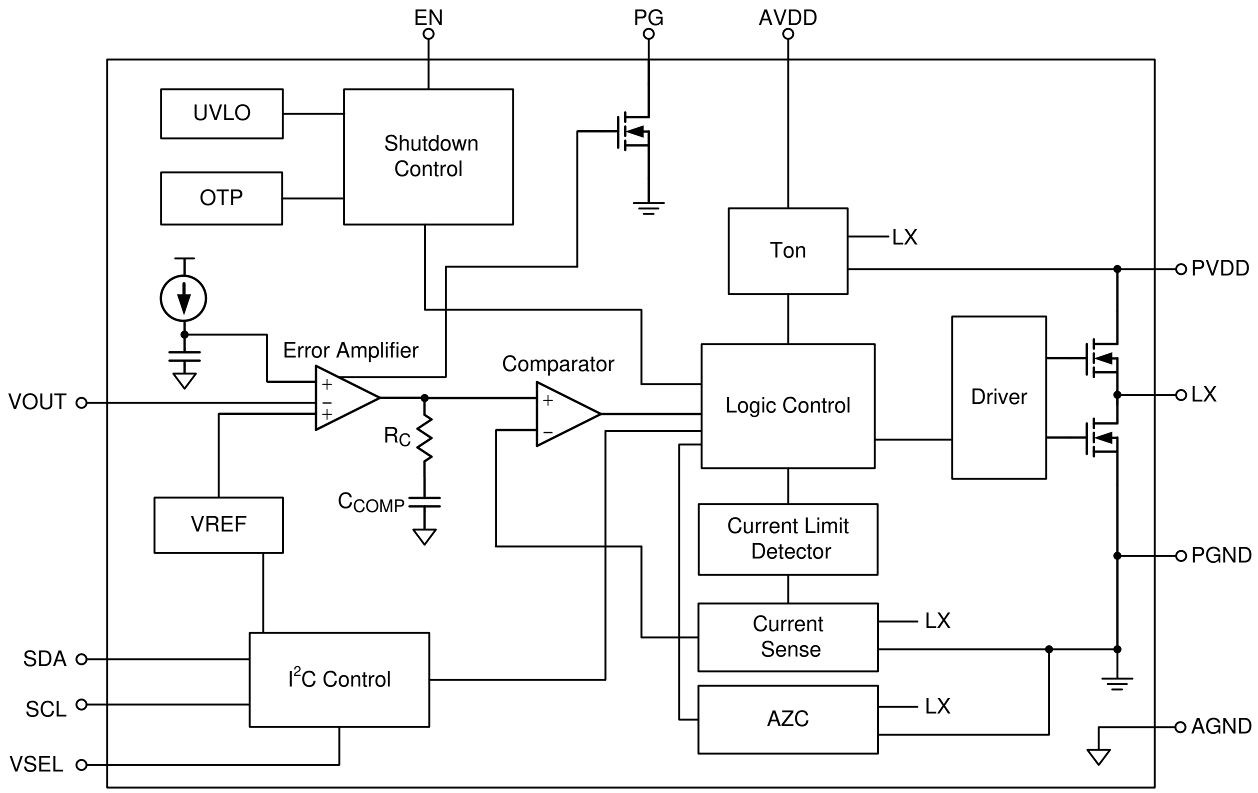


WL-CSP-20B 1.6x2 (BSC)

Functional Pin Description

Pin No.	Pin Name	Pin Function
A1	VSEL	Output Voltage/ Mode Selection. The level determines which of two programmable, configurations to utilize (operating mode / output voltage). There is an internal pull down resistor on this pin; could be left open if not used.
A2	EN	Enable Control Input. Active high will enable the part. There is an internal pull-down resistor on this pin.
A3	SCL	I^2C Clock Input.
A4	FB	Output Voltage Pin.
B1	SDA	I^2C Data Input.
B3	PG/PGND	Power Good Open-Drain Output. If not used, it has to be connected to ground plane.
B2, B4, C2, C3, C4	PGND	Power Ground.
C1	AGND	Analog Ground should be electrically connected to GND close to the device.
D1	AVDD	Analog Circuit Input Supply Voltage.
D2, E1, E2	PVDD	Input Supply Voltage, 2.5V to 5.5V.
D3, D4, E3, E4	LX	Switch Node. The source of the internal high-side power MOSFET, and drain of the internal low-side (synchronous) rectifier MOSFET.

Function Block Diagram



Operation

The RT5735 is a synchronous low voltage step-down converter that can support the input voltage range from 2.5V to 5.5Vand the output current can be up to 5A. The RT5735 uses a constant on-time, current mode architecture. In steady-state operation, the high-side N-MOSFET is turned on when the current feedback reaches COMP level which is the amplified difference between the reference voltage and the feedback voltage. The on time of high-side N-MOSFET is determined by on-time generator which is a function of input and output voltage. After on-time expires, high-side MOSFET is turned off and low-side MOSFET is turned on. Until the low-side current sensing signal reaches the COMP, the high-side MOSFET is turned on again. In this manner, the converter regulates the output voltage and keeps the frequency constant.

The switching frequency is 2.4MHz allows for efficiency and size optimization when selecting the output filter components.

The RT5735 reduces the external component count by integrating the boot recharge MOSFET.

The error amplifier EA adjusts COMP voltage by comparing the output voltage with the internal I^2C set reference voltage. When the load increases, it causes a drop in the output voltage relative to the reference, then the COMP voltage rises to allow higher inductor current to match the load current.

PWM Frequency and Adaptive On Time Control

The on-time can be roughly estimated by the equation :

$$T_{on} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{F_{SW}}$$ where F_{SW} is nominal 2.4MHz

Auto-Zero Current Detector

The auto-zero current detector circuit senses the LX waveform to adjust the zero current threshold voltage. When the current of low-side MOSFET decreases to the zero current threshold, the low-side MOSFET turns off to prevent negative inductor current. In this way, the zero current threshold can adjust for different condition to get better efficiency.

Protection Features

The RT5735 has many features to protect the device.

Under-Voltage Protection (UVLO)

The UVLO continuously monitors the voltage of AVDD to make sure the device works properly. When the AVDD is high enough to reach the high threshold voltage of UVLO, the step-down converter softly starts or pre-bias to its regulated output voltage. When the AVDD decreases to its low threshold (180mV hysteresis), the device will shut down.

Power Good

When the output voltage is higher than PG rising threshold, the PG flag is High.

Output Under-Voltage Protection (UVP)

When the output voltage is lower than 400mV after soft-start end is ok, the UVP is triggered. When UVP occurs, the device enters hiccup mode.

Over-Current Protection (OCP)

The RT5735 senses the current signal when low-side MOSFET turns on and uses a valley current limiting circuit. As a result, the OCP set point is the OCP DC limit minus half of the ripple current. The OCP is cycle-by-cycle limit. If the OCP occurs, the converter holds off the next on pulse until inductor current drops below the OCP limit. If the OCP keeps and the load current is larger than the current provided by the converter, the output voltage drops. When the output voltage triggers UVP, the converter enters hiccup mode.

Soft-Start

An internal current source charges an internal capacitor to build the soft-start ramp voltage. The typical soft-start time is 130μs.

Over-Temperature Protection (OTP)

The RT5735 has over-temperature protection. When the device triggers the OTP, the device shuts down.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{IN} ---------- –0.3V to 6V
- Other Pins ---------- –0.3V to V_{IN} + 0.3V
- Power Dissipation, P_D @ T_A = 25°C
  WL-CSP-1.6x2-20B ---------- 1.818W
- Package Thermal Resistance (Note 2)
  WL-CSP-1.6x2-20B (BSC), θ_{JA} ---------- 55°C/W
  WL-CSP-1.6x2-20B (BSC), θ_{JC} ---------- 7°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 2.5V to 5.5V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = 3.6V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current							
Operating Quiescent Current PWM		I_{Q_PWM}	PWM Mode IQ at I_{OUT} = 0A (Note 5)	--	10	20	mA
Operating Quiescent Current PFM		I_{Q_PFM}	PSM Mode IQ at I_{OUT} = 0A	--	70	--	μA
Product in Off Mode		I_{OFF}	EN, VSEL Low, V_{IN} = 2.5V to 5.5V	--	1	5	μA
DC/DC Converter							
Operation Input Voltage		V_{IN}		2.5	--	5.5	V
Output Voltage DC Error		ΔV_{OUT}	PWM Mode	–1	--	1	%
			PSM Mode	–1	--	2	
Switching Frequency		F_{SW}		2.16	2.4	2.64	MHz
R_{ON}	High-Side	R_{ON_H}	V_{IN} = 5V	--	34	--	mΩ
	Low-Side	R_{ON_L}	V_{IN} = 5V	--	18	--	
Valley Current Limit Level		$I_{LIM,Valley}$	I_{OC} = 00 Valley Current (Note 5)	--	4	--	A
			I_{OC} = 01 Valley Current (Note 5)	--	4.7	--	
			I_{OC} = 10 Valley Current (Note 5)	--	5.4	--	
			I_{OC} = 11 Valley Current	5.4	6.4	7.4	

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Load Regulation		ΔV_{LOAD}	I_{OUT} from 300mA to I_{OUTMAX} (Note 5)	--	0.2	--	%/A
Line Regulation		ΔV_{LINE}	$2.5V \leq V_{IN} \leq 5.5V$	--	0.3	--	%
Transient Load Response		AC_{LOAD}	tr = ts = 0.1μs Load Step 0 to 1.2A (Note 5)	--	±40	--	mV
Turn On Time		T_{start}	Time from EN Transition from Low to High to 90% of Output Voltage	--	70	--	μs
			Time from EN Transition from Low to High to V_{OUT}	--	130	--	
DC/DC Active Output Discharge		R_{DISCHG}	Force V_{OUT} = 1.15V, EN = Low	--	16	--	Ω
EN. VSEL							
Input Voltage	Logic-High	V_{IH}		1.05	--	--	V
	Logic-Low	V_{IL}		--	--	0.4	
PG							
Power Good High Hysteresis		V_{PGH}	Rising Edge as a Percentage of Nominal Output Voltage	90	94	98	%
Power Good Low Threshold		V_{PGL}	Falling Edge as a Percentage of Nominal Output Voltage	86	90	94	%
Power Good Reaction Time for DC/DC		T_{RT}	Falling	--	3.5	--	μs
			Rising	3.5	--	14	
Power Good Low Output Voltage		V_{PGL}	I_{PG} = 5mA	--	--	0.2	V
Power Good Leakage Current		PG_{LK}	3.6V at PG Pin when Power Good Valid	--	--	100	nA
Power Good High Output Voltage		V_{PGH}	Open-Drain	--	--	5.5	V
I²C							
High Level at SCL/SDA Line		V_{I2CINT}		1.7	--	5	V
SCL, SDA Input Voltage	Logic-High	V_{I2CIH}		1.7	--	--	V
	Logic-Low	V_{I2CIL}		--	--	0.5	
SDA Low Output Voltage		V_{I2COL}	I_{SINK} = 3mA	--	--	0.4	V
I²C Clock Frequency		F_{SCL}	(Note 5)	--	--	3.4	MHz
Total Device							
Under-Voltage Lockout Threshold		V_{UVLO}	V_{IN} Falling	--	2.15	2.34	V
V_{IN} POR		V_{POR}	V_{IN} Rising	--	2.3	2.45	V
Thermal Shutdown Protection		T_{SD}	(Note 5)	--	150	--	°C
Warning Rising Edge		$T_{WARNING}$	(Note 5)	--	135	--	°C
Pre-Warning Threshold		T_{PWTH}	For Default Setting (Note 5)	--	105	--	°C
Thermal Shutdown Hysteresis		T_{SDH}	(Note 5)	--	30	--	°C
Thermal Warning Hysteresis		$T_{WARNING\_HYS}$	(Note 5)	--	15	--	°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Pre−Warning Hysteresis	T_{PWTH_HYS}	(Note 5)	--	6	--	°C

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

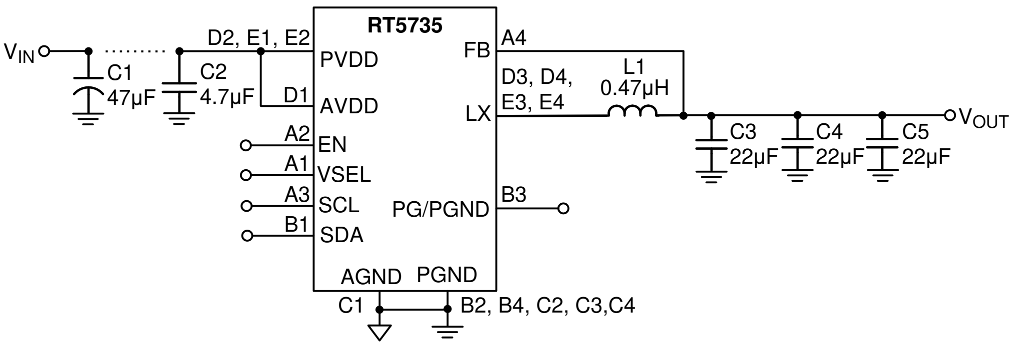
Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution recommended.

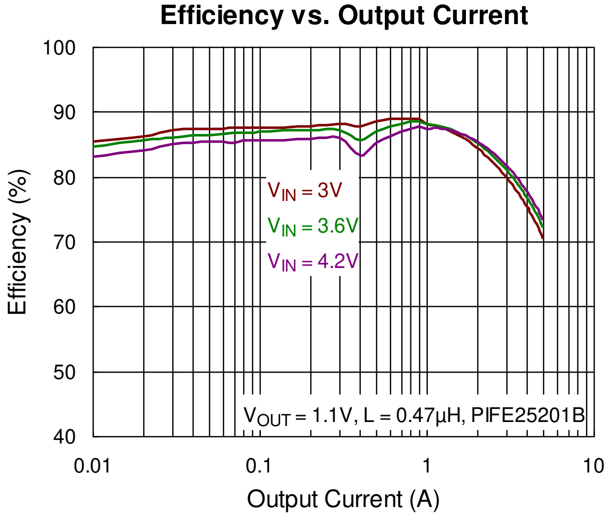
Note 4. The device is not guaranteed to function outside its operating conditions.

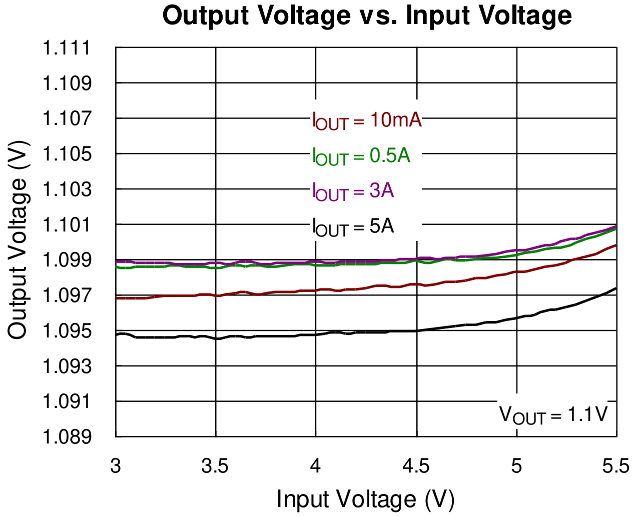
Note 5. Guaranteed by design and characterized.

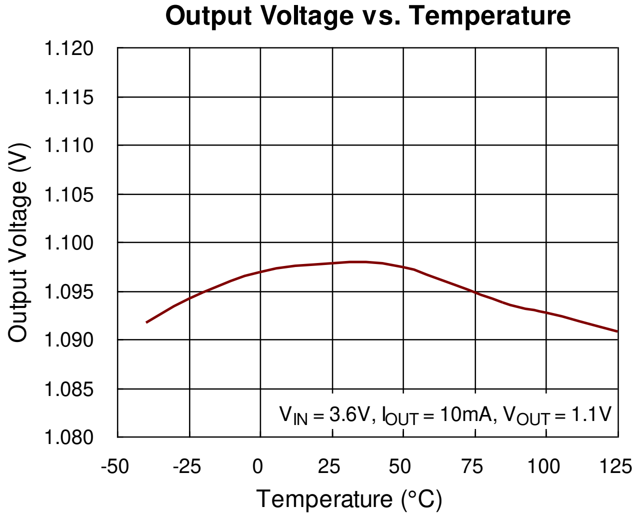
Typical Application Circuit

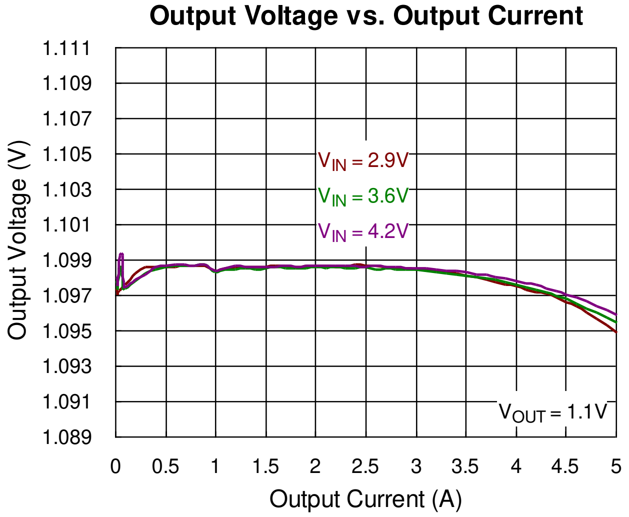


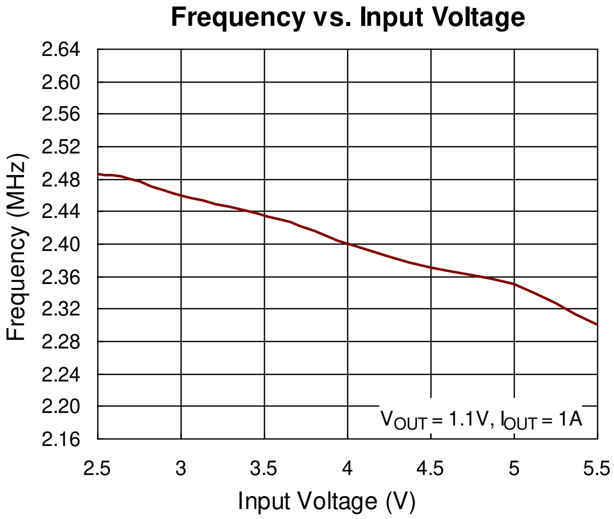
Typical Operating Characteristics

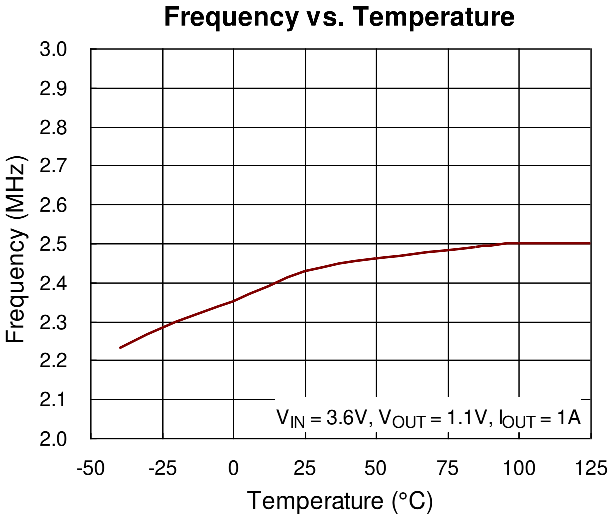




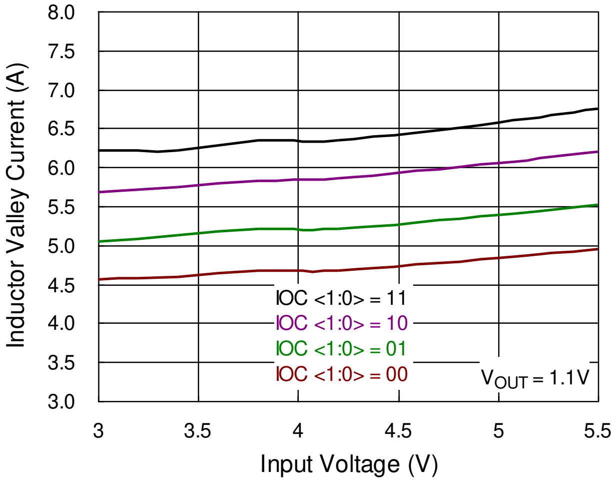




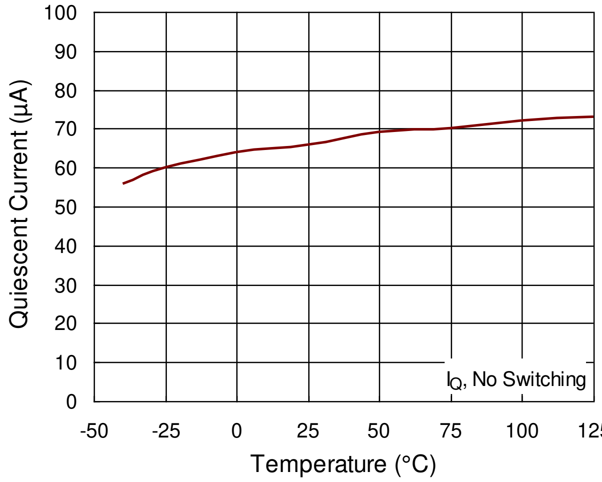




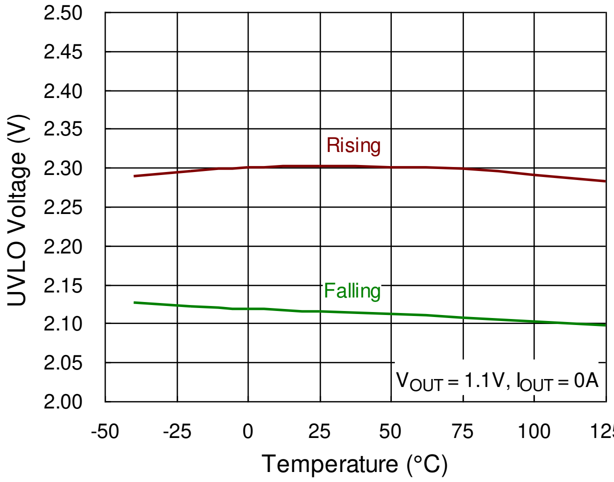
Current Limit vs. Input Voltage



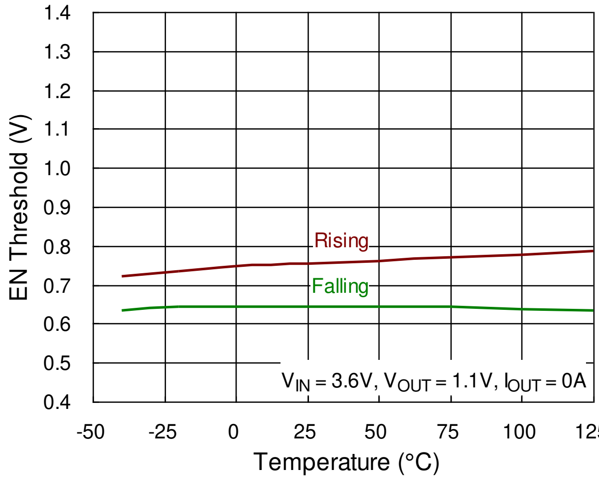
Quiescent Current vs. Temperature



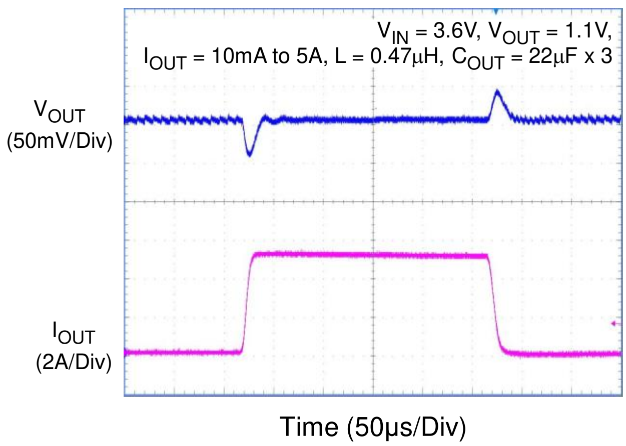
UVLO Voltage vs. Temperature



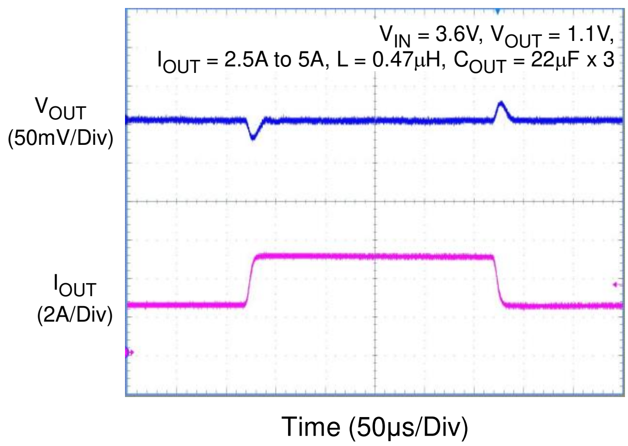
EN Threshold vs. Temperature



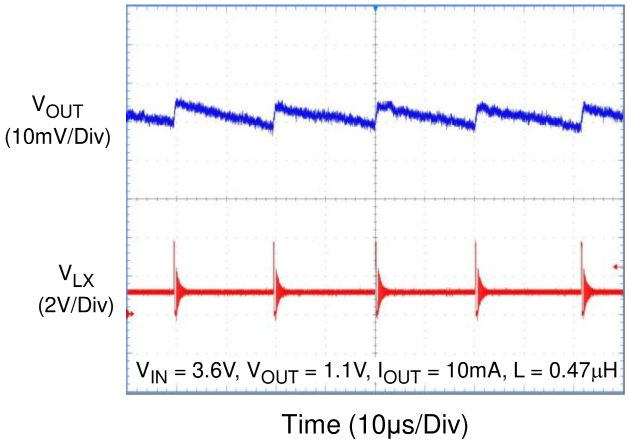
Load Transient Response



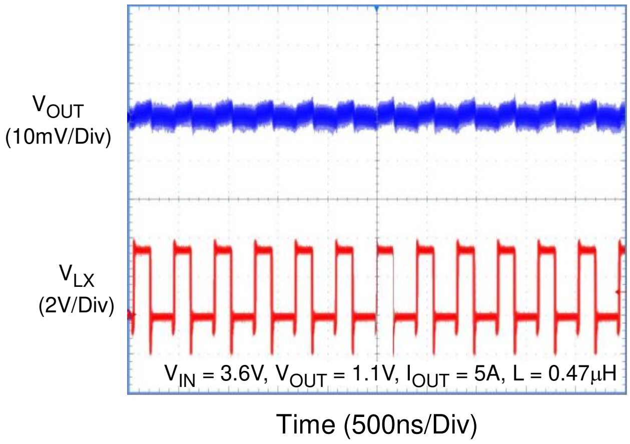
Load Transient Response



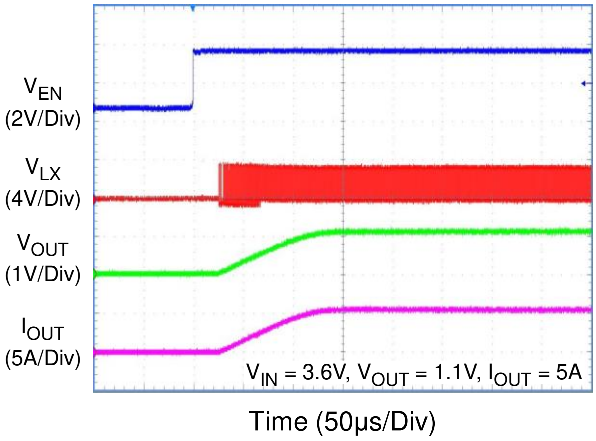
Output Ripple Voltage



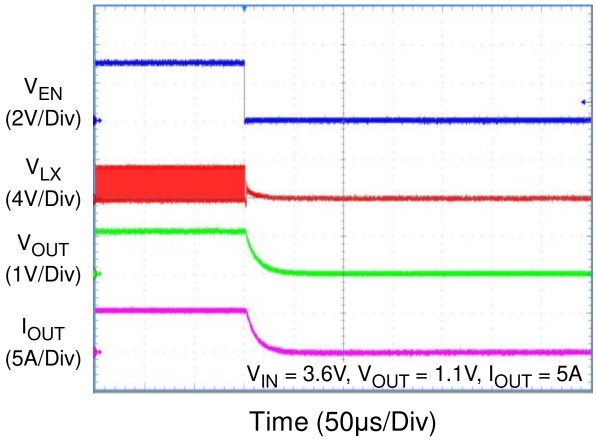
Output Ripple Voltage



Power On from EN



Power Off from EN



Application Information

The basic RT5735 application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by C_{IN} and C_{OUT}.

Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current, ΔI_L, increases with higher V_{IN} and decreases with higher inductance, as shown in equation below :

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

where f is the operating frequency and L is the inductance. Having a lower ripple current reduces not only the ESR losses in the output capacitors, but also the output voltage ripple. Higher operating frequency combined with smaller ripple current is necessary to achieve high efficiency. Thus, a large inductor is required to attain this goal. The largest ripple current occurs at the highest V_{IN}. A reasonable starting point for selecting the ripple current is $\Delta I_L = 0.3 \times I_{MAX}$ to $0.4 \times I_{MAX}$. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

The inductor's current rating (defined by a temperature rise from 25°C ambient to 40°C) should be greater than the maximum load current and its saturation current should be greater than the short-circuit peak current limit.

Input and Output Capacitor Selection

An input capacitor, C_{IN}, is needed to filter out the trapezoidal current at the source of the high-side MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT(MAX)} / 2$. This simple worst-case condition is commonly used for design. Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet the size or height requirements of the design. Ceramic capacitors have high ripple current, high voltage rating and low ESR, which makes them ideal for switching regulator applications. However, they can also have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can lead to significant ringing. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part. Thus, care must be taken to select a suitable input capacitor.

The selection of C_{OUT} is determined by the required ESR to minimize output voltage ripple. Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response. The output voltage ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \le \Delta I_L \left[ESR + \frac{1}{8 f_{OSC} C_{OUT}}\right]$$

where f_{OSC} is the switching frequency and ΔI_L is the inductor ripple current. The output voltage ripple will be the highest at the maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement. Ceramic capacitors have excellent low ESR characteristics, but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing. Nevertheless, high value, low cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications.

I^2C Interface Function

RT5735 can be used by I^2C interface to select V_{OUT} voltage level, over current limit level, thermal warning temperature level, PWM control mode, and so on. The register of each function can be found from the following register map and it also explains how to use these function.

V_{OUT} Selection : RT5735 has external VSEL pin to select PROGVSEL1(0X10) or PROGVSEL0(0X11) which can control V_{OUT} from 0.6V to 1393.75mV with 7bits resolution. Pull VSEL to high is for PROGVSEL1 and pull VSEL to low is for PROGVSEL0. If VSELGT bit in the COMMAND register is set to 0, V_{OUT} will only be controlled by PROGVSEL1.

Discharge Function : In the PGOOD register DISCHG bit is set to 1 can let V_{OUT} discharge by internal resistor when converter shuts down. If setting to 0 V_{OUT} will decrease depending on the loading.

Power Good Function : In the PGOOD register PGDCDC bit can control if external PG pin is active. After PG function is active if PGDVS pin is 0, PG will not change state during V_{OUT} changing. Once PGDVS pin is 1 PG will be low when V_{OUT} is much lower than V_{REF} during V_{OUT} changing.

Slew Rate Setting : RT5735 can control slew rate as V_{OUT} changing between two voltage levels for both up and down. In the time register DVS_UP bits can control up-speed when in the LIMCONF register DVS_DOWN can control down-speed. DVS_DOWN is valid only when converter is at PWM mode or DVSMODE bit is 1.

Force PWM Mode : In the COMMAND register PWMSEL0 and PWMSEL1 can decide converter is always at PWM mode or enters power saving mode at light load condition. During output voltage is changed from high to low at light load, setting DVSMODE bit to 1 will make transition operate at PWM mode and output voltage will decrease quickly. If setting to 0, the output voltage will decrease depending on the loading.

Over Current Level : RT5735 has four levels of over current limit to be selected. Using IOC bits in the LIMCONF register can change different inductor valley current limit level.

Thermal Shutdown Protection : The default REARM bit in the LIMCONF register is 1. RT5735 will shut down switching operation when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 30°C the IC will resume normal operation with a complete soft-start. When REARM bit is set to 0, once the device triggers the OTP, the system will be latched and the output voltage will no longer be regulated during OTP latched state. Re-start input voltage or EN pin can unlatch the protection state. Using I^2C to shutdown the system and then re-enable it will also unlatch UVP function.

The RT5735 default I^{2}C slave address = 7'b0011100. I^{2}C interface support fast mode (bit rate up to 400kb/s). The write or read bit stream (N≥1) is shown below :

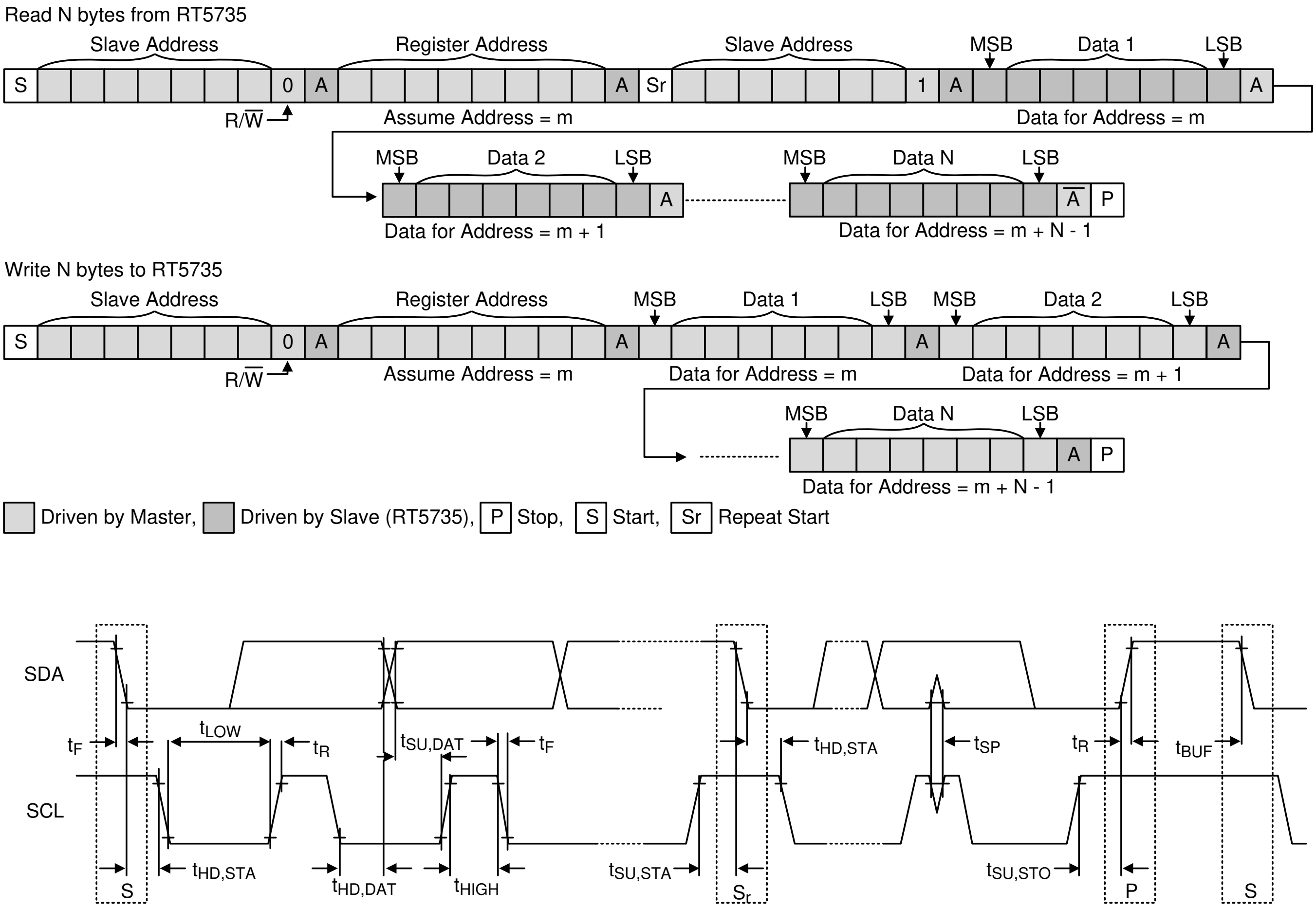


Figure 1. I^{2}C Read and Write Stream and Timing Diagram

RT5735 can also support High-speed mode(bit rate up to 3.4Mb/s) with access code 08H. Figure 2 and Figure 3 show detail transfer format. Hs-mode can only commence after the following conditions (all of which are in F/S-mode) :

- START condition (S)
- 8-bit master code (00001xxx)
- not-acknowledge bit ($\bar{A}$)

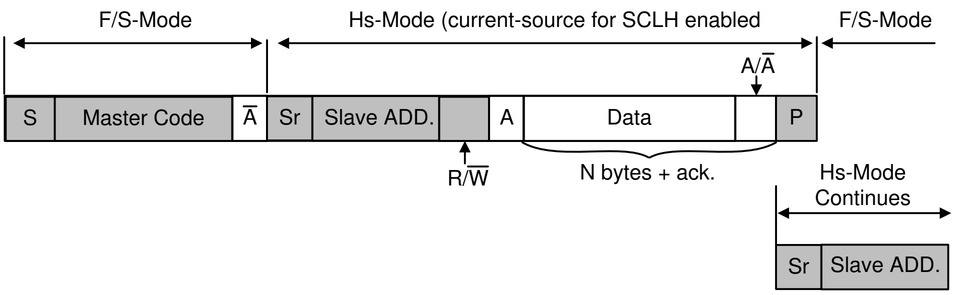


Figure 2. Data Transfer Format in Hs-mode

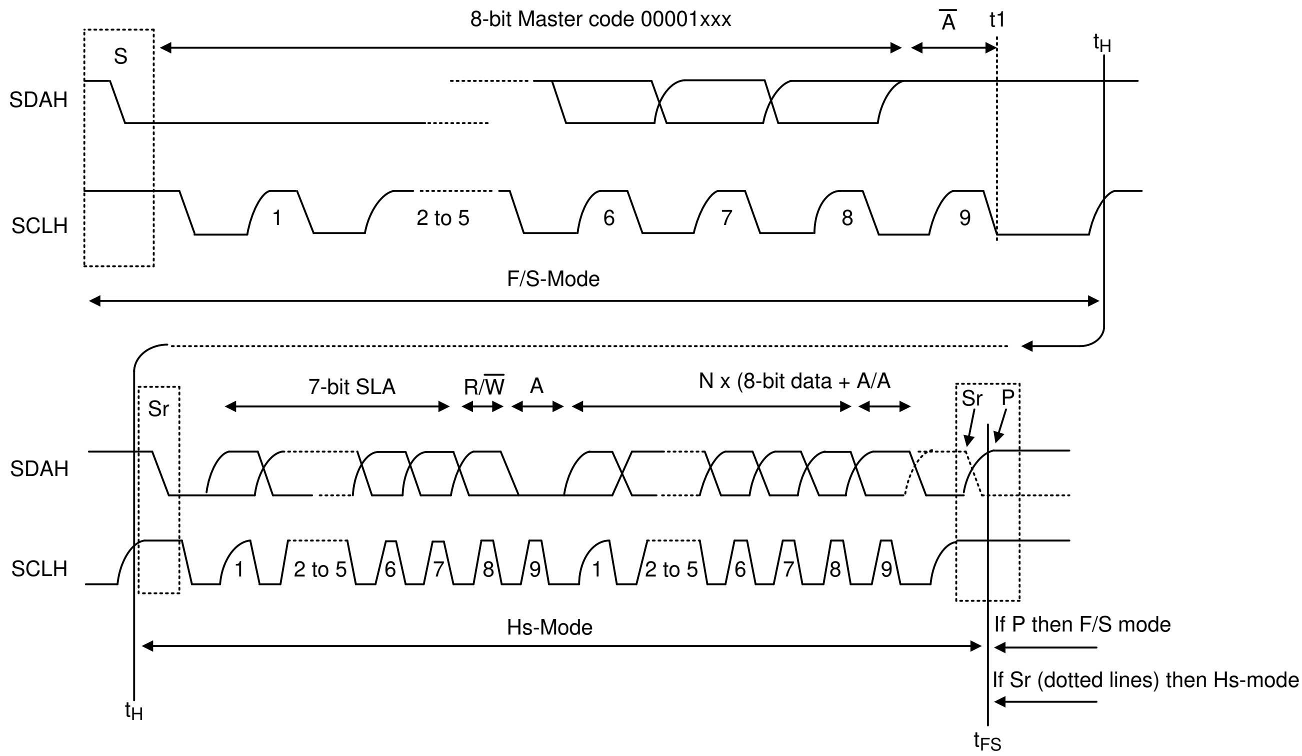


Figure 3. A Complete Hs-mode Transfer

Address Name	Register Address		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PRODUCT_ID	0x03	Meaning	PRODUCT_ID							
		Default	0	0	0	1	0	0	0	0
		Read/Write	R	R	R	R	R	R	R	R
REVISION_ID	0x04	Meaning	REVISION_ID							
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R	R	R	R	R	R
FEATURE_ID	0x05	Meaning	FEATURE_ID							
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R	R	R	R	R	R
VENDER ID	0x06	Meaning	VENDER_ID							
		Default	1	0	0	0	1	0	0	0
		Read/Write	R	R	R	R	R	R	R	R
PROGVSEL1	0x10	Meaning	ENVSEL1	Vout_VSEL1[6:0]						
		Default	1	1	0	1	0	0	0	0
		Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
PROGVSEL0	0x11	Meaning	ENVSEL0	Vout_VSEL0[6:0]						
		Default	1	0	0	1	0	0	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PGOOD	0x12	Meaning	RESV			DISCHG	RESV		PGDVS	PGDCDC
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R	R/W	R	R	R/W	R/W
TIME	0x13	Meaning	RESV			DVS_UP[2:0]			RESV	
		Default	0	0	0	1	1	0	0	1
		Read/Write	R	R	R	R/W	R/W	R/W	R	R
COMMAND	0x14	Meaning	PWMSEL0	PWMSEL1	DVSMODE	RESV				VSELGT
		Default	0	0	0	0	0	0	0	1
		Read/Write	R/W	R/W	R/W	R	R	R	R	R/W
LIMCONF	0x16	Meaning	IOC<1:0>		TPWTH<1:0>		RESV	DVS_DOWN<1:0>		REARM
		Default	0	1	1	0	0	0	1	1
		Read/Write	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
PRODUCT _ID	0x03	Meaning	PRODUCT_ID							
		Default	0	0	0	1	0	0	0	0
		Read/Write	R	R	R	R	R	R	R	R
PRODUCT_ID			PRODUCT_ID							

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
REVISION _ID	0x04	Meaning	REVISION_ID							
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R	R	R	R	R	R
REVISION_ID			REVISION_ID							

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
FEATURE_ ID	0x05	Meaning	FEATURE_ID							
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R	R	R	R	R	R
FEATURE_ID			FEATURE_ID							

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
VENDER ID	0x06	Meaning	RESV							
		Default	1	0	0	0	1	0	0	0
		Read/Write	R	R	R	R	R	R	R	R
VENDER ID			VENDER ID							

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
PROGVSE L1	0x10	Meaning	ENVSEL1	Vout_VSEL1[6:0]						
		Default	1	1	0	1	0	0	0	0
		Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
ENVSEL1			EN Pin Gating for VSEL internal signal = High 0 : Disabled 1 : Enabled							
Vout_VSEL1[6:0]			VID Table satisfy : SEL[6:0] = 1111111 : VOUT = 1393.75mV … SEL[6:0] = 1010000: VOUT = 1.1V (default) … SEL[6:0] = 0000000 :0.6V 6.25mV step for DCDC, VOUT = 600mV + 6.25mV x SEL							

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
PROGVSEL0	0x11	Meaning	ENVSEL0	Vout_VSEL0[6:0]						
		Default	1	0	0	1	0	0	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ENVSEL0			EN Pin Gating for VSEL internal signal= Low 0 : Disabled 1 : Enabled							
Vout_VSEL0[6:0]			VID Table satisfy : SEL[6:0] = 1111111 : VOUT = 1393.75mV … SEL[6:0] = 0010000 : VOUT = 0.7V (default) … SEL[6:0] = 0000000 : 0.6V 6.25mV step for DCDC, VOUT = 600mV + 6.25mV x SEL							

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
PGOOD	0x12	Meaning	RESV			DISCHG	RESV		PGDVS	PGDCDC
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R	R/W	R	R	R/W	R/W
RESV			Reserved bits							
DISCHG			Active discharge bit enabling 0 : Discharge path disabled 1 : Discharge path enabled							
RESV			Reserved bits							
PGDVS			Power good active on DVS 0 : Disabled 1 : Enabled							
PGDCDC			Power good enabling 0 : Disabled 1 : Enabled							

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
TIME	0x13	Meaning	Reserved			DVS_UP[2:0]			Reserved	
		Default	0	0	0	1	1	0	0	1
		Read/Write	R	R	R	R/W	R/W	R/W	R	R
RESV			Reserved bits							
DVS_UP[2:0]			DVS slew rate for up 000 : 64mV/μS 001 : 16mV/μS 010 : 32mV/μS 011 : 8mV/μS 100 : 4mV/μS 101 : 4mV/μS 110 : 32mV/μS 111 : 8mV/μS							
RESV			Reserved bits							

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
COMMAND	0x14	Meaning	PWMSEL0	PWMSEL1	DVSMODE	RESV				VSELGT
		Default	0	0	0	0	0	0	0	1
		Read/Write	R/W	R/W	R/W	R	R	R	R	R/W
PWMSEL0			Operation mode for VSEL internal signal = Low 0 : Auto 1 : Forced PWM							
PWMSEL1			Operation mode for VSEL internal signal = High 0 : Auto 1 : Forced PWM							
DVSMODE			DVS transition mode selection 0 : Auto 1 : Forced PWM							
RESV			Reserved bits							
VSELGT			VSEL Pin gating 0 : Disabled 1 : Enabled							

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
LIMCONF	0x16	Meaning	IOC<1:0>		TPWTH<1:0>		RESV	DVS_DOWN<1:0>		REARM
		Default	0	1	1	0	0	0	1	1
		Read/Write	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
IOC[1:0]			Inductor valley current settings 00 = 4A (typ.) 01 = 4.7A (typ.) 10 = 5.4A (typ.) 11 = 6.4A (typ.)							
TPWTH[1:0]			Thermal pre-warning threshold settings 00 = 83°C 01 = 94°C 10 = 105°C 11 = 116°C							
RESV			Reserved bits							
DVS_DOWN[1:0]			DVS slew rate for down 00 = 32mV/μs 01 = 4mV/μs 10 = 8mV/μs 11 = 16mV/μs							
REARM			Recovery of device after TSD 0 : No Recovery after TSD 1 : Recovery after TSD							

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WL-CSP-20B 1.6x2 (BSC) package, the thermal resistance, θ_{JA}, is 55°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (55°C/W) = 1.8W for WL-CSP-20B 1.6x2 (BSC) package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 4 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

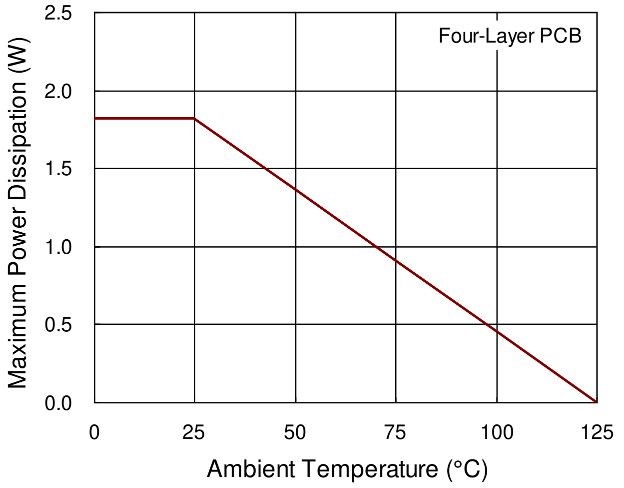


Figure 4. Derating Curve of Maximum Power Dissipation

Layout Considerations

For best performance of the RT5735, the following layout guidelines must be strictly followed.

- Input capacitor must be placed as close to the IC as possible.
- SW should be connected to inductor by wide and short trace. Keep sensitive components away from this trace.
- Keep every trace connected to pin as wide as possible for improving thermal dissipation.

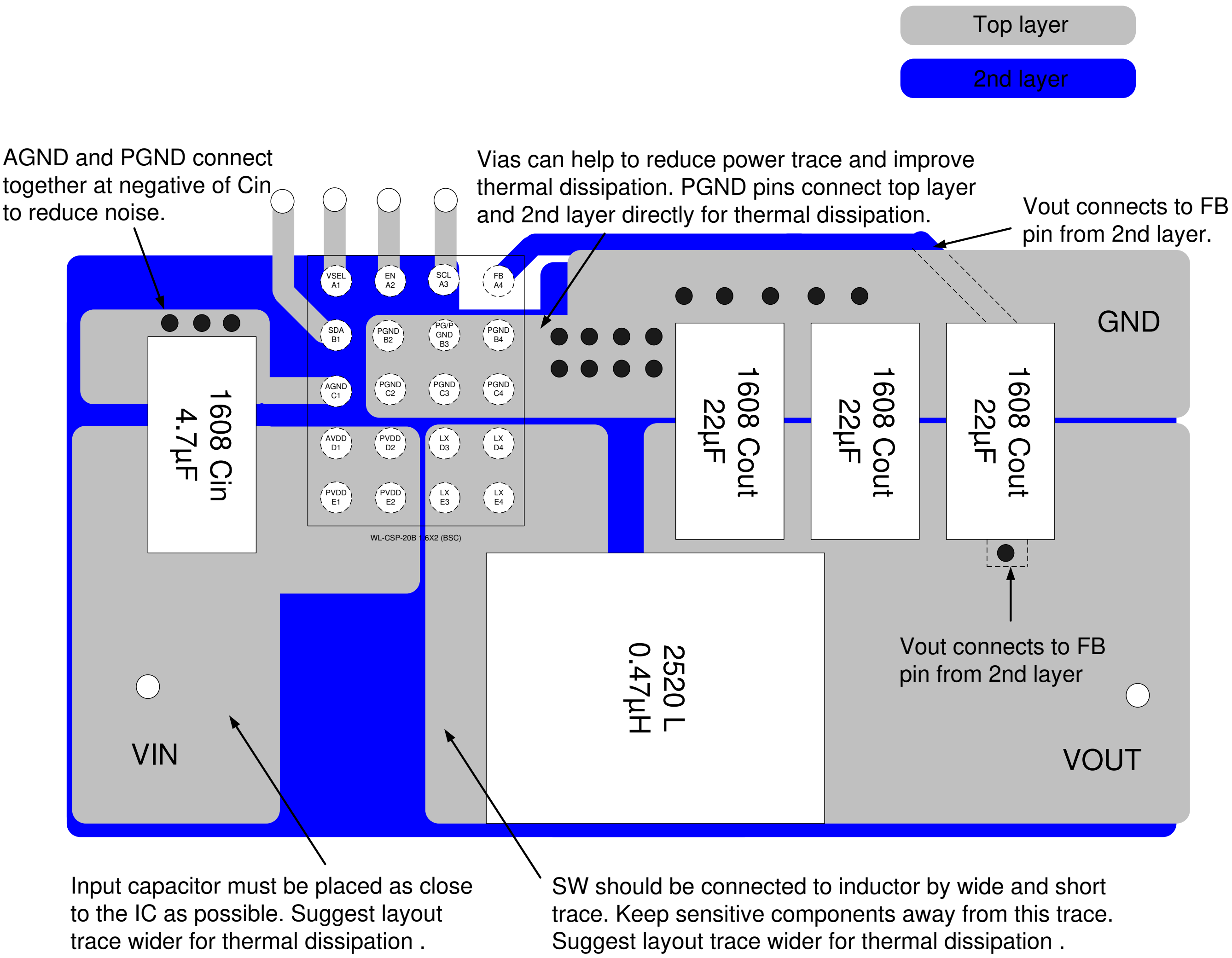
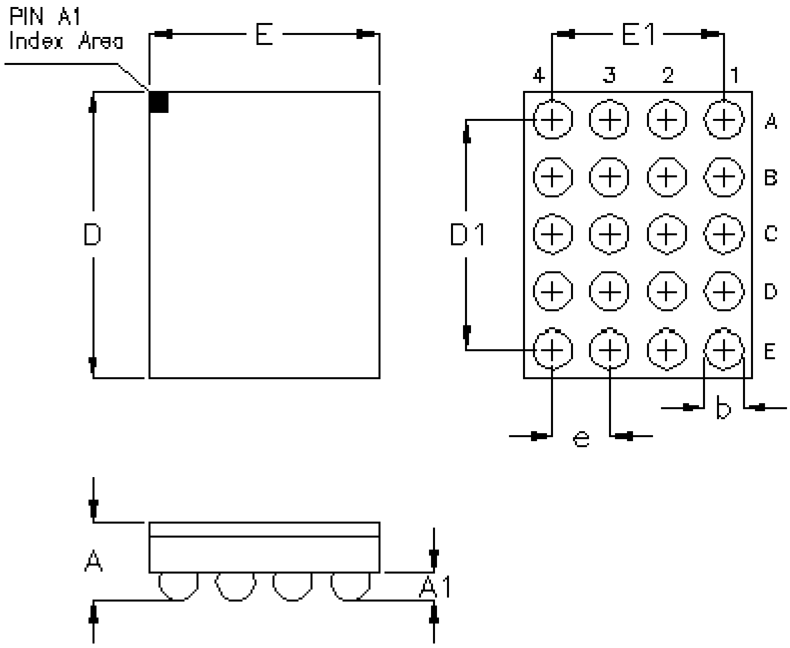


Figure 5. PCB Layout Guide

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	1.950	2.050	0.077	0.081
D1	1.600		0.063	
E	1.550	1.650	0.061	0.065
E1	1.200		0.047	
e	0.400		0.016	

20B WL-CSP 1.6x2 Package (BSC)

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