



# **MachXO5-NX Development Board**

## **Evaluation Board User Guide**

FPGA-EB-02052-1.1

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## Acronyms in This Document

A list of acronyms used in this document.

| Acronym          | Definition                              |
|------------------|-----------------------------------------|
| CMOS             | Complementary Metal-Oxide Semiconductor |
| DNI              | Do Not Install                          |
| FTDI             | Future Technology Devices International |
| GPIO             | General Purpose Input/Output            |
| I <sup>2</sup> C | Inter-Integrated Circuit                |
| LDO              | Low Dropout                             |
| LVDS             | Low-Voltage Differential Signaling      |
| SPI              | Serial Peripheral Interface             |

# 1. Introduction

The Lattice Semiconductor MachXO5™-NX Development Board allows you to investigate and experiment with the features of the MachXO5-25 device. The features of the MachXO5-NX Development Board can assist you with the rapid prototyping and testing of their specific designs.

The MachXO5-NX Development Board is part of the MachXO5-NX Development Kit, which includes the following:

- MachXO5-NX Development Board pre-loaded with the demo design
- 12 V AC/DC Power adapter
- Mini USB cable
- Quick Start Guide

The contents of this user guide include top-level functional descriptions of the various portions of the development board, descriptions of the onboard headers, diodes and switches, and a complete set of schematics.

## 1.1. MachXO5-NX Development Board

Along with the MachXO5-25 device, the MachXO5-NX Development Board also includes features to expand the usability of the MachXO5-25 with Arduino, Raspberry, FX12, Versa, and Aardvark headers.

Figure 1.1 shows the top view of the MachXO5-NX Development Board.

Figure 1.2 shows the bottom view of this board.

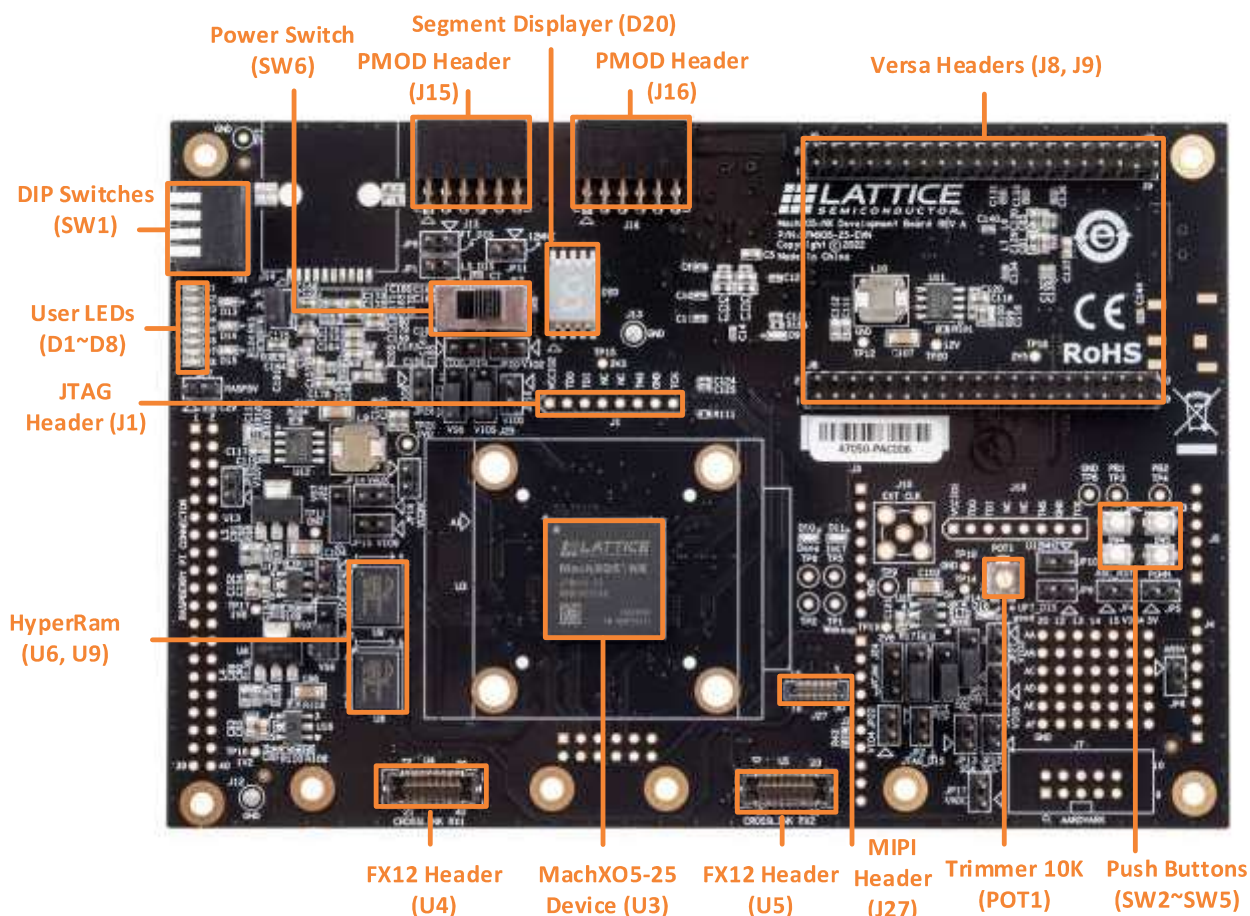


Figure 1.1. Top View of MachXO5-NX Development Board

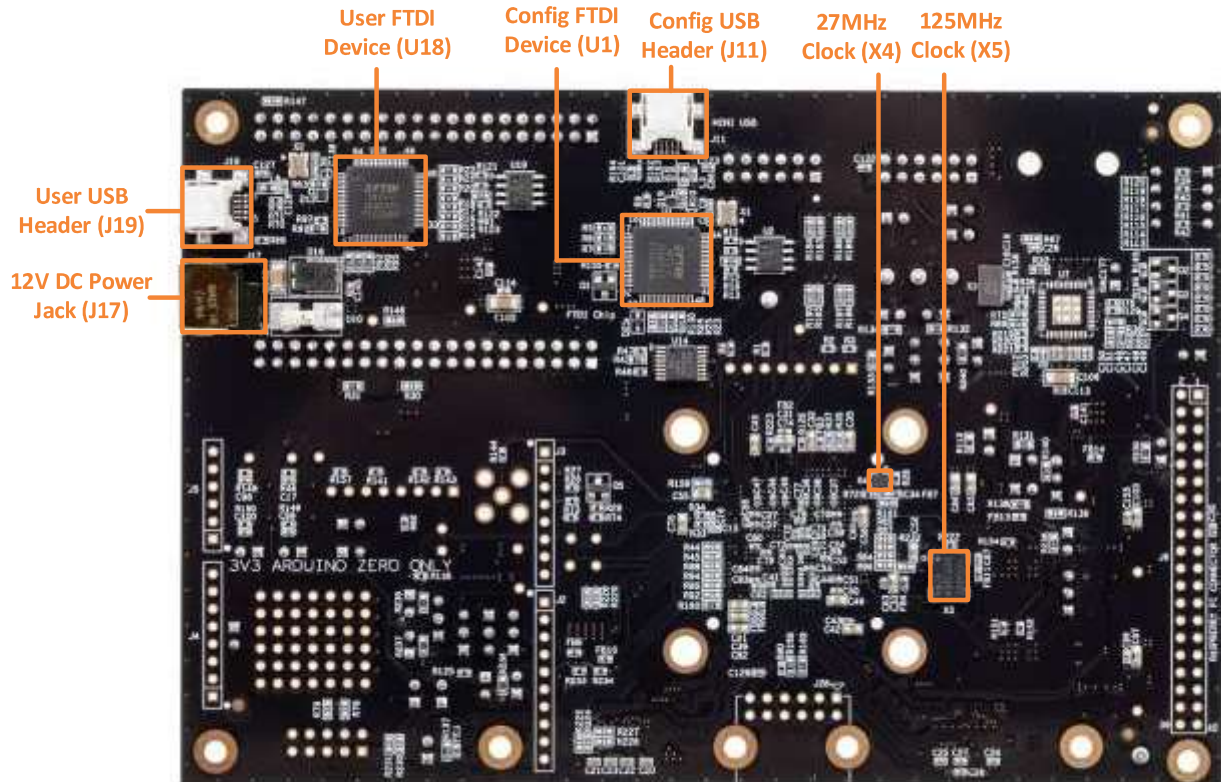


Figure 1.2. Bottom View of MachXO5-NX Development Board

## 1.2. Features

- On board MachXO5-25 Device
- Optional SGMII, Gbe PHY RJ45 connector (Check Appendix D for the board revision information)
- HyperRAM upto 166MHz, x16 bits
- Versa Headers bridge with Lattice ASC Demo Board to support L-ASC10
- General Purpose Input/Output (GPIO) interface with PMOD, Arduino and Raspberry Pi boards
- USB-B connection for device programming with JTAG and Inter-Integrated Circuit (I<sup>2</sup>C) utility
- Additional USB-B connection for user with Soft JTAG and UART utility
- 7-Segment Blue LED, 4-position DIP Switches, 4 push buttons, and 8 red LEDs for demo purposes
- ADC interface with 10K POT
- Two Hirose FX12-40 headers
- Multiple reference clock sources
- Optional Aardvark header
- Lattice Radiant<sup>®</sup> programming support

**Note:** DNI stands for “Do NOT Install” parts and DI stands for “Do Install” parts for assembly.

**Caution:** The MachXO5-NX Development Board contains ESD-sensitive components. ESD safe practices should be followed while handling and using the development board.

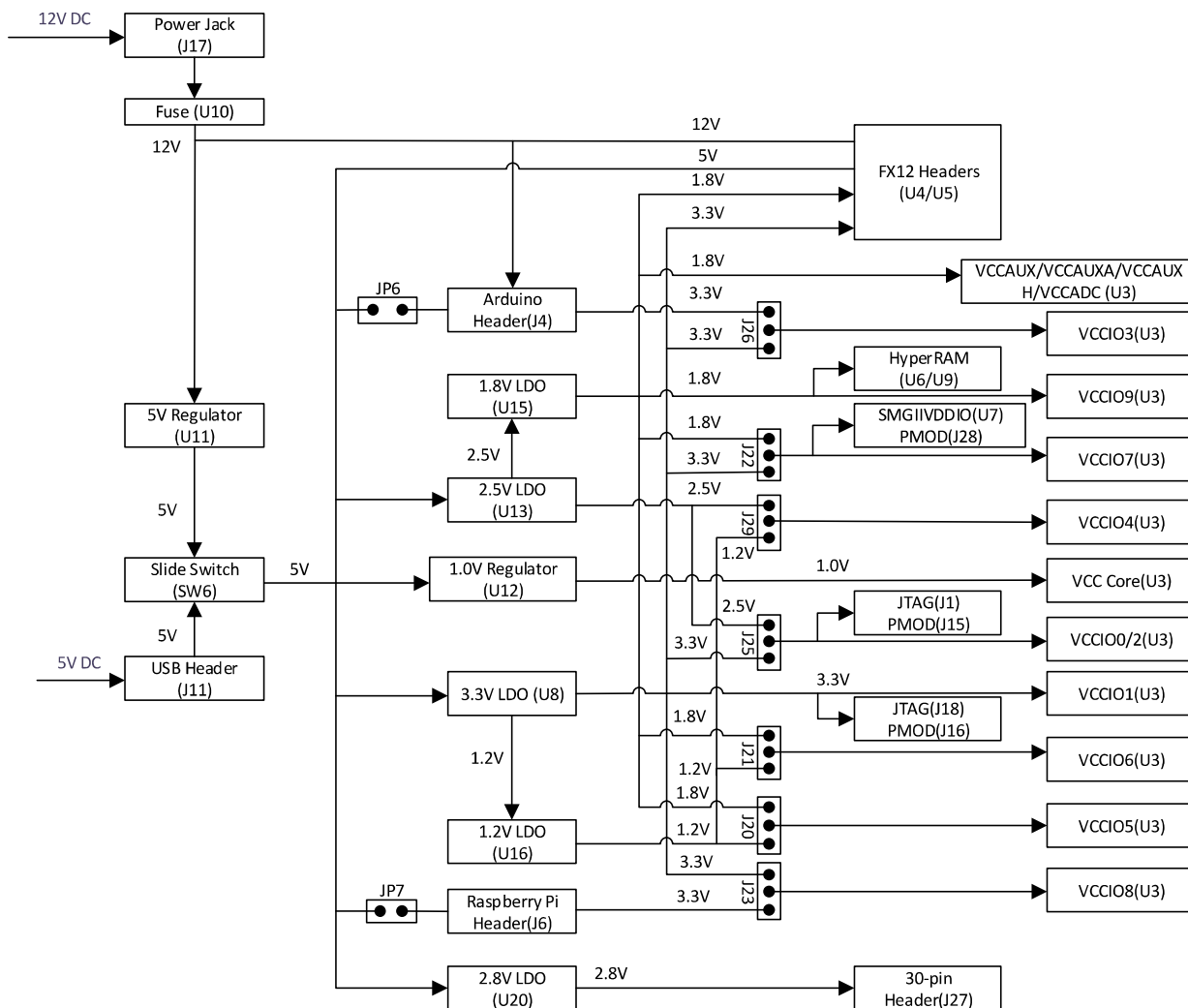
### 1.3. MachXO5-25 Device

The MachXO5-NX Development Board features the MachXO5-25 in a 400-ball caBGA package. This device offers a variety of features and programmability that enhances Secure Control PLD functionality with Multiple Boot capabilities. Its cryptographic engine supports user-mode security features. Along with the cryptographic engine, numerous system functions are included such as two PLLs and 432 kbits of embedded RAM plus hardened implementations of I<sup>2</sup>C and SPI. Flexible, high performance I/O support numerous single-ended and differential standards including LVDS and MIPI. For more information on the capabilities of MachXO5-25 device, see [MachXO5-NX Family Data Sheet \(FPGA-DS-02102\)](#).



## 2. Applying Power to the Board

The MachXO5-NX Development Board comes ready to power up with onboard DC/DC switching regulators and Low Dropout (LDO) generators powered by an external 12 V DC power source. The external power supply can be connected with the DC power input jack J17, which is fused with a surface mounted fuse U10. The 1.25A fuse prevents the crashed current from flowing into the internal circuits and cause serious damage. 12 V DC power also supply Arduino Header J4 and FX12 headers U4/U5 for the board extension, as shown in Figure 2.1.



**Figure 2.1. Board Power Supply**

The onboard 5 V power regulator U11 provide 90% power convert efficiency from 12 V when output current between 50 mA and 3 A. It is distributed to 3.3 V, 2.8 V, 2.5 V LDOs and 1.0 V regulator through one side of slide switch SW6 to support onboard devices. Through another side of SW6, this board can also take the 5 V power from USB header J11 as well, for some low power application. It is user's responsibility to ensure all 5 V power rails on board consume less than 500mA per PC's USB port output capability when take power from J11.

For the board extension, 5 V DC power can also supply FX12 adapter, Raspberry Pi and Arduino boards through the jumpers and onboard headers, to consolidate AC/DC adapters for stack boards system. Conversely, 5V DC power can be either supplied from mated boards with correct jumper settings. However, maintain the 5 V DC power is the basic requirement to bring up this board, by quick check the power good blue LED D18.

The onboard 1.2 V and 1.8 V LDOs take the power from 3.3 V and 2.5 V LDO correspondently.

Table 2.1 summarizes onboard major power rails and their test points.

**Table 2.1. Onboard Major Power Rails**

| Power Net Name | Primary Source                 | Test Point |
|----------------|--------------------------------|------------|
| +12V           | DC Power Jack (J17)            | TP20       |
| PS_5V          | DC/DC Regulator (U11 )         | —          |
| VBUS_5V        | Mini-USB (J11)                 | —          |
| +5.0V          | Selected by Slide switch (SW6) | TP14       |
| +3.3V          | LDO (U8)                       | TP15       |
| +1.2V          | LDO (U16)                      | TP18       |
| +2.5V          | LDO (U13)                      | TP16       |
| +1.8V          | LDO (U15)                      | TP17       |
| +2.8V          | LDO (U20)                      | TP19       |
| +1.0V          | DC/DC Regulator (U12)          | TP21       |
| +3.3V_RASP     | Raspberry Pi Header (J6)       | —          |
| +3.3V_AR       | Arduino Header (J4)            | —          |

As shown in [Figure 2.1](#), this board provides multiple power options for I/O bank voltage flexibility. [Table 2.2](#) summarizes the VCCIO support matrix on this board. For an example, VCCIO0 and VCCIO2 share the same three positions jumper J25 and short its Pin 1 and Pin 2 can bring the 3.3 V LDO output to both I/O bank 0 and bank 2. For power consumption evaluation, this board facilitate some two-position jumpers with 1  $\Omega$  sense resistors to measure the voltage drop on each power rail, then the supply current can be calculated.

**Table 2.2. MachXO5-25 IO Bank Power Rails Stuff**

| MachXO5-25 Power (U3) | Jumpers | 3.3V    | 2.5V    | 1.8V    | 1.2V    | Ext 3.3V | Power Test Point | Sense Resistor of 1 $\Omega$ |
|-----------------------|---------|---------|---------|---------|---------|----------|------------------|------------------------------|
| VCCIO0                | J25     | Pin 1-2 | Pin 2-3 | —       | —       | —        | JP19             | R132                         |
| VCCIO1                | —       | Fixed   | —       | —       | —       | —        | JP16             | R133                         |
| VCCIO2                | J25     | Pin 1-2 | Pin 2-3 | —       | —       | —        | JP20             | R134                         |
| VCCIO3                | J26     | Pin 1-2 | —       | —       | —       | Pin 2-3  | JP21             | R235                         |
| VCCIO4                | J29     | —       | Pin 1-2 | —       | Pin 2-3 | —        | JP22             | R236                         |
| VCCIO5                | J20     | —       | —       | Pin 2-3 | Pin 1-2 | —        | JP23             | R237                         |
| VCCIO6                | J21     | —       | —       | Pin 2-3 | Pin 1-2 | —        | JP24             | R238                         |
| VCCIO7                | J22     | Pin 1-2 | —       | Pin 2-3 | —       | —        | JP25             | R239                         |
| VCCIO8                | J23     | Pin 1-2 | —       | —       | —       | Pin 2-3  | JP26             | R240                         |
| VCCIO9                | —       | —       | —       | Fixed   | —       | —        | JP15             | R138                         |

Other than power rail for each I/O Bank, this board also provides some test points to evaluate the major power consumptions for MachXO5-25 device.

**Table 2.3. MachXO5-25 Major Power Rails Stuff**

| MachXO5-25 Power (U3)    | Power Test Point | Voltage Drop Resistor | Resistance    |
|--------------------------|------------------|-----------------------|---------------|
| VCC_CORE                 | JP18             | R112                  | 0.01 $\Omega$ |
| VCC_AUX/VCC_AUXH/VCCAUXA | JP14             | R131                  | 1 $\Omega$    |
| VCC_ADC                  | JP17             | R137                  | 1 $\Omega$    |

### 3. Hard JTAG/I<sup>2</sup>C Programming

The hardened JTAG/I<sup>2</sup>C programming architecture of the MachXO5-NX Development Board is shown in Figure 3.1. The board has a built-in download controller for programming the MachXO5-25 device. It uses an FT2232H Future Technology Devices International (FTDI) part U1 to convert USB to JTAG from port A, or convert USB to I<sup>2</sup>C from port B. Using Detect Cable function with Radiant programming software installed, you can detect dual ports after power up the board and connect the mini USB to USB-A cable from J11 to your PC ensuring FTDI reset control jumper JP9 is not populated as default. The software select option FTUSB-0 is dedicate for hard JTAG and FTUSB-1 is dedicate for hard I<sup>2</sup>C which is mapping with port A and port B from hardware perspective, as shown in Figure 3.2.

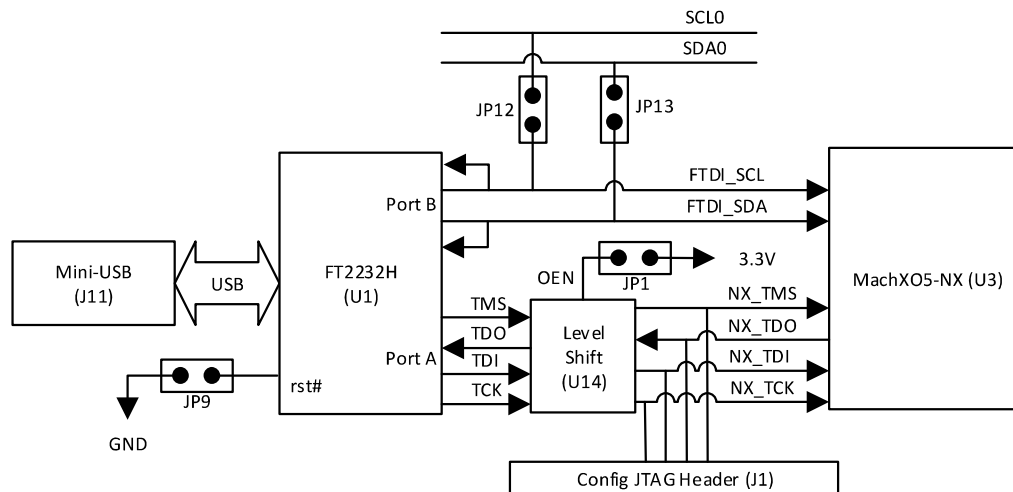


Figure 3.1. JTAG/I<sup>2</sup>C Programming Architecture

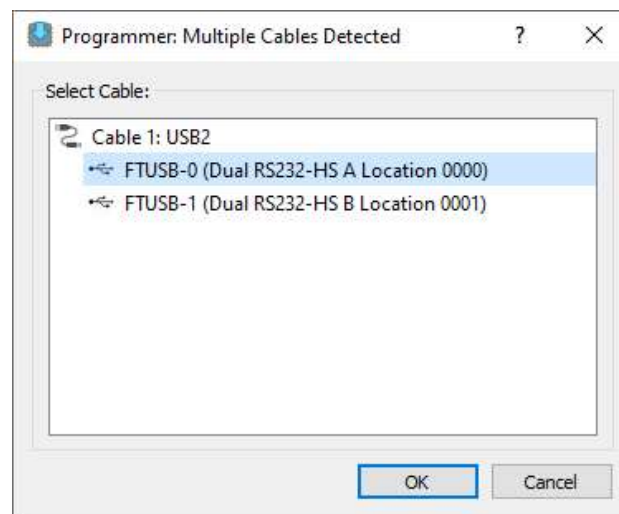


Figure 3.2. Radiant Programmer Detect Dual Ports

#### 3.1. JTAG Download Interface

A level shifter SN74AVC4T774 U14 from TI is inserted between Config FTDI Port A and MachXO5-25 JTAG port to make sure the FTDI fixed I/O voltage can adapt with flexible voltage selection of FPGA's bank 2, as shown in Figure 3.3. An 8-pin header J1 as shown in Figure 3.4 allowing you not only to probe the JTAG signals, but also to access MachXO5-25 JTAG port from external JTAG host such as external Lattice HW-USBN-2B Programming Cable (available separately), or access SSPI port from external SPI host. In those cases, jumper JP1 must be added to pull OEN high and ensure U14 to



output tri-state mode, avoiding multi-drivers on those shared signals. The JTAG connections between J1 and MachXO5-25 are listed in [Table 3.1](#).

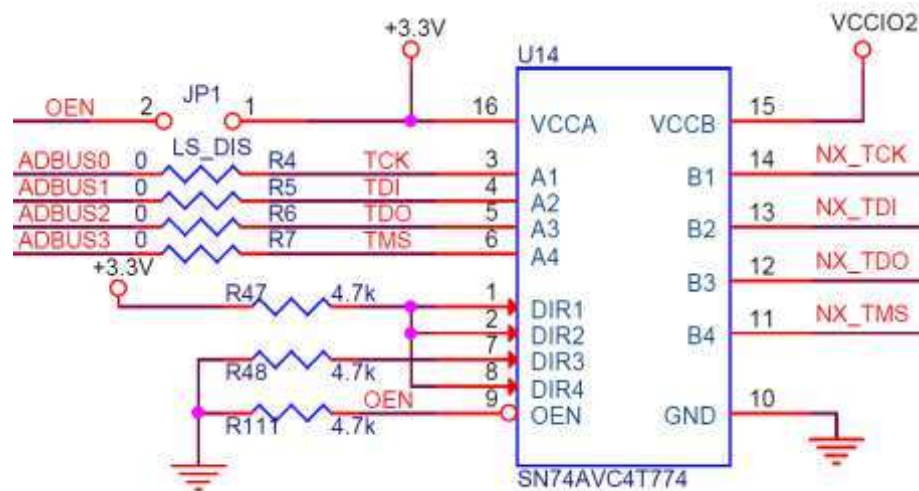


Figure 3.3. Level Shift for JTAG Download Interface

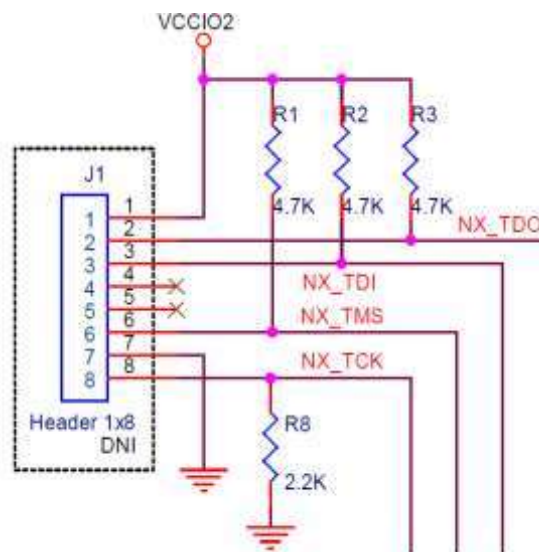


Figure 3.4. JTAG Test Header

Table 3.1. Config JTAG Connections

| J1 Pin Number | JTAG Net Name | MachXO5-25 Ball Location for JTAG | Optional SSPI Function |
|---------------|---------------|-----------------------------------|------------------------|
| 1             | VCCIO2        | —                                 | —                      |
| 2             | NX_TDO        | E20                               | SSI                    |
| 3             | NX_TDI        | E18                               | SSO                    |
| 4             | —             | —                                 | —                      |
| 5             | —             | —                                 | —                      |
| 6             | NX_TMS        | F16                               | SCSN                   |
| 7             | GND           | —                                 | —                      |
| 8             | NX_TCK        | G16                               | SCLK                   |

The MachXO5-NX Development Board also provides test points for other dedicated JTAG configuration pins as shown in [Table 3.2](#).

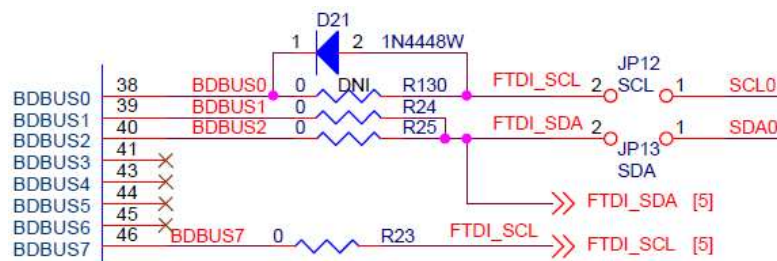
**Table 3.2. Other Config JTAG Control Signals**

| Net Name | MachXO5-25 Ball Location | LED Indicator | Test Point   |
|----------|--------------------------|---------------|--------------|
| JTAGEN   | B20                      | —             | Pin 1 of JP2 |
| PROGRAMN | F12                      | —             | Pin 1 of JP5 |
| INITN    | E13                      | D11           | TP5          |
| DONE     | F13                      | D10           | TP6          |

JP2 for JTAGEN is used to pull down the JTAGEN for enabling JTAG port when JTAG\_PORT is disabled by software. JP5 can bridge push button PB4 with PROGRAMN when PROGRAMN\_PORT function is enabled by software.

## 3.2. I<sup>2</sup>C Download Interface

The USB hub on the PC can also detect the addition of the USB function on Config FTDI Port B and you can select the port FTUSB-1 on the programmer interface for the accessing from Config FTDI Port B to the MachXO5-25 dedicated I<sup>2</sup>C download port ([Figure 3.2](#)) that is named as FTDI\_SDA/FTDI\_SCL with 2.2 k $\Omega$  pull up resistor each. The Diode D21 is inserted to support I<sup>2</sup>C clock stretching mode. [Figure 3.5](#) details the design of Config FTDI Port B for dedicated I<sup>2</sup>C download interface. [Table 3.3](#) summarizes the interconnection with MachXO5-25 and its supported circuits. JP12 and JP13 are used to connect the dedicated I<sup>2</sup>C download port of MachXO5-25 with the bridge I<sup>2</sup>C bus SDA0/SCL0 cross the whole board, in case you need access I<sup>2</sup>C download port from other on board headers other than Config FTDI part. For the detail connection from other headers to bridge I<sup>2</sup>C bus SDA0/SCL0, refer to the [User I2C Interface](#) section.



**Figure 3.5. I<sup>2</sup>C Programming Mode**

**Table 3.3. Download I<sup>2</sup>C Connections**

| Download I <sup>2</sup> C Net Name | MachXO5-25 Ball Location for JTAG | 2.2 k $\Omega$ Pull up Resistor | Bridge I <sup>2</sup> C Net Name | Bridge Jumper |
|------------------------------------|-----------------------------------|---------------------------------|----------------------------------|---------------|
| FTDI_SCL                           | G15                               | R33                             | SCL0                             | JP12          |
| FTDI_SDA                           | F15                               | R34                             | SDA0                             | JP13          |

For more information on MachXO5-25 JTAG/ I<sup>2</sup>C programming, refer to [MachXO5-NX Programming and Configuration User Guide \(FPGA-TN-02271\)](#).

## 4. Soft JTAG/UART User Interface

The soft JTAG/UART user interface for the MachXO5-NX Development Board is shown in Figure 4.1. Supposedly it also uses an FT2232H FTDI part U18 to convert USB to user JTAG from port A, or convert USB to UART from port B. Using Detect Cable function with Radiant programming software installed and ensuring FTDI reset control jumper JP8 is not populated in default, as shown in Figure 3.2, you can detect other dual ports after power up the board. You can then connect the mini USB to USB-A cable from J19 to your PC. The software select option FTUSB-0 is targeted for user JTAG, and FTUSB-1 is targeted for UART that is mapped with port A and port B from hardware perspective.

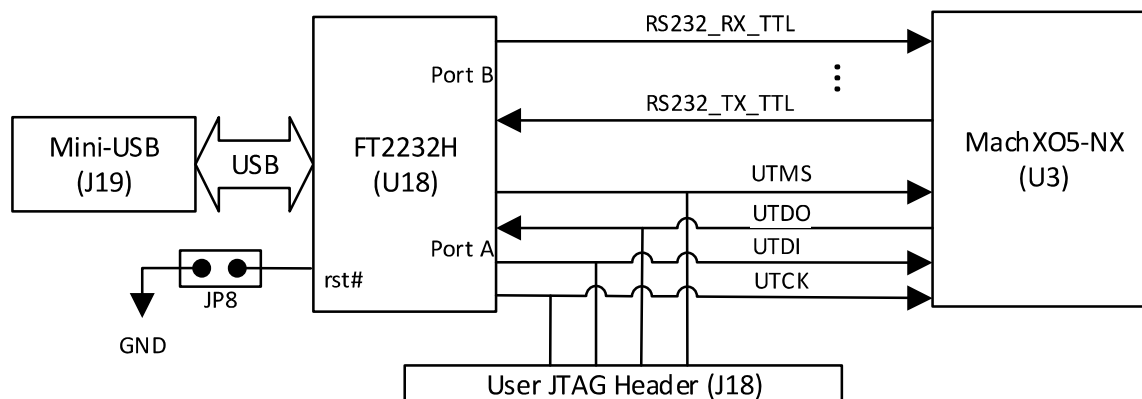


Figure 4.1. JTAG/UART User Interfacing

### 4.1. Soft JTAG User Interface

User FTDI Port A is connected with GPIOs in Bank 1 directly, but you need allocate GPIOs for adaption with JTAG signals by programmable logic, which is defined by FTDI Port A when converting USB to JTAG through FTUSB-0. J18 is an 8-pin standalone JTAG header that is used with an external Lattice download cable (available separately) when the FTDI part is disabled from the JTAG chain after setting JP8. J18 can also be used as test point when USB to JTAG is working.

Table 4.1. Soft JTAG Connections

| J18 Pin Number | FTDI Signal | JTAG Net Name | MachXO5-25 Ball Location |
|----------------|-------------|---------------|--------------------------|
| 1              | —           | VCCIO1        | —                        |
| 2              | UADBUS2     | UTDO          | A12                      |
| 3              | UADBUS1     | UTDI          | A11                      |
| 4              | —           | —             | —                        |
| 5              | —           | —             | —                        |
| 6              | UADBUS3     | UTMS          | A13                      |
| 7              | —           | GND           | —                        |
| 8              | UADBUS0     | UTCK          | A14                      |

### 4.2. Soft UART User Interface

User FTDI Port B is also connected with GPIOs in Bank 1 directly, but you need allocate GPIOs for adaption with UART signals by programmable logic, which is defined by FTDI Port B when converting USB to UART through FTUSB-1.

**Table 4.2. Soft UART Connections**

| FTDI Signal | UART Net Name | MachXO5-25 Ball Location for Port A |
|-------------|---------------|-------------------------------------|
| UBDBUS0     | RS232_RX_TTL  | B11                                 |
| UBDBUS1     | RS232_TX_TTL  | B12                                 |
| UBDBUS2     | RTSn          | B13                                 |
| UBDBUS3     | CTSn          | B14                                 |
| UBDBUS4     | DTRn          | B15                                 |
| UBDBUS5     | DSRn          | B16                                 |
| UBDBUS6     | DCDn          | B17                                 |
| UBDBUS7     | RI            | C11                                 |

## 5. MachXO5-25 Clock Sources

The MachXO5-NX Development Board has multiple external clock options for the MachXO5-25 applications as shown in Figure 5.1.

- 12 MHz from U1 (FTDI)
- 12 MHz from U18 (FTDI)
- 25 MHz from U7 (SGMII PHY)
- 27 MHz from X4 (OSC MEM)
- 125 MHz from X5 (OSC MEM)
- External clock source from J10 (SMA)

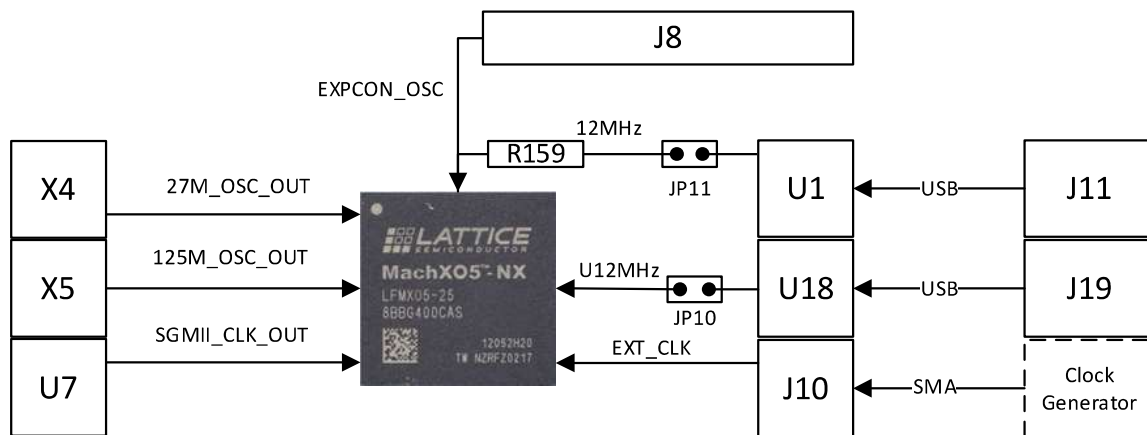


Figure 5.1. Onboard Clock Resources

You need take care that only 27 MHz and 125 MHz clocks are active in default after board power up. Both 12 MHz clocks from the FT2232H FTDI U1 and U18 device are not always on without some hardware configuration. 25 MHz of SGMII and external clock need source from other devices. Refer to Table 5.1 for those clock utilization and enable conditions.

Table 5.1. Input Clock Options

| Clock Frequency | Net Name      | MachXO5-25 Ball Location | Clock Source | Always On? | Enable Conditions                                                    |
|-----------------|---------------|--------------------------|--------------|------------|----------------------------------------------------------------------|
| 12 MHz          | 12MHZ         | E16                      | U1           | No         | Need add R159 and JP11. USB header J11 connected with power on.      |
| 12 MHz          | U12MHZ        | E14                      | U18          | No         | Need add JP10. USB header J19 connected with power on.               |
| 25 MHz          | SGMII_CLK_OUT | T7                       | U7           | No         | Power on. U7 populated and enabled.                                  |
| 27 MHz          | 27M_OSC       | B1                       | X4           | Yes        | Power on. Force 27M_EN high if R161 populated.                       |
| 125 MHz         | 125M_OSC      | V1                       | X5           | Yes        | Power on. Force 125M_EN high if R232 populated.                      |
| Customer        | EXT_CLK       | D19                      | J10          | No         | Need add J10. Connect to external clock generator through SMA cable. |

## 6. SGMII Ethernet Connections

This section describes the MachXO5-NX Development Board SGMII application for Ethernet connections.

**Table 6.1. SGMII Ethernet PHY Connections**

| U7 Pin Number | U7 Signal Name  | Net Name        | MachXO5-25 Ball Location | Application Notes                  |
|---------------|-----------------|-----------------|--------------------------|------------------------------------|
| 1             | TD_P_A          | SGMII_MD0_P     | —                        | To RJ45                            |
| 2             | TD_M_A          | SGMII_MD0_N     | —                        | To RJ45                            |
| 3             | VDDA2P5         | +2.5V           | —                        | 2.5 V Power                        |
| 4             | TD_P_B          | SGMII_MD1_P     | —                        | To RJ45                            |
| 5             | TD_M_B          | SGMII_MD1_N     | —                        | To RJ45                            |
| 6             | VDD1P0          | VCCA_1V_PHY     | —                        | 1.0 V Power                        |
| 7             | TD_P_C          | SGMII_MD2_P     | —                        | To RJ45                            |
| 8             | TD_M_C          | SGMII_MD2_N     | —                        | To RJ45                            |
| 9             | VDDA2P5         | +2.5V           | —                        | 2.5 V Power                        |
| 10            | TD_P_D          | SGMII_MD3_P     | —                        | To RJ45                            |
| 11            | TD_M_D          | SGMII_MD3_P     | —                        | To RJ45                            |
| 12            | RBIAS           | —               | —                        | Pull down to GND                   |
| 13            | VDDA1P8         | SGMII_PHY_D1V8  | —                        | 1.8 V Power                        |
| 14            | XO              | SGMII_XO        | —                        | 25 MHz Crystal Output              |
| 15            | XI              | SGMII_XI        | —                        | 25 MHz Crystal Input               |
| 16            | MDC             | SGMII_MDIO_CLK  | U1                       | Optional pull up to VDDIO          |
| 17            | MDIO            | SGMII_MDIO_DATA | U2                       | Pull up to VDDIO                   |
| 18            | CLK_OUT         | SGMII_CLK_OUT   | T7                       | With 22 $\Omega$ debounce resistor |
| 19            | VDDIO           | SGMII_VDDIO     | —                        | VCCIO7 selectable                  |
| 20            | JTAG_CLK        | —               | —                        | Pull down to GND                   |
| 21            | JTAG_TDO        | —               | —                        | Pull up to VDDIO                   |
| 22            | JTAG_TMS        | —               | —                        | Pull up to VDDIO                   |
| 23            | JTAG_TDI        | —               | —                        | Pull up to VDDIO                   |
| 24            | VDD1P0          | VCCA_1V_PHY     | —                        | 1.0 V Power                        |
| 25            | TX_D3           | —               | —                        | Pull down to GND                   |
| 26            | TX_D2           | —               | —                        | Pull down to GND                   |
| 27            | TX_D1/SGMII_SIP | SGMII_PHY_SIP   | N8                       | 0.1 $\mu$ F AC coupling            |
| 28            | TX_D0/SGMII_SIN | SGMII_PHY_SIN   | P8                       | 0.1 $\mu$ F AC coupling            |
| 29            | GTX_CLK         | —               | —                        | Pull down to GND                   |
| 30            | VDDIO           | SGMII_VDDIO     | —                        | VCCIO7 selectable                  |
| 31            | VDD1P0          | VCCA_1V_PHY     | —                        | 1.0 V Power                        |
| 32            | RX_CLK          | —               | —                        | —                                  |
| 33            | RX_D0/SGMII_COP | SGMII_PHY_COP   | U9                       | 0.1 $\mu$ F AC coupling            |
| 34            | RX_D1/SGMII_CON | SGMII_PHY_CON   | V9                       | 0.1 $\mu$ F AC coupling            |
| 35            | RX_D2/SGMII_SOP | SGMII_PHY_SOP   | N9                       | 0.1 $\mu$ F AC coupling            |
| 36            | RX_D3/SGMII_SON | SGMII_PHY_SON   | P9                       | 0.1 $\mu$ F AC coupling            |
| 37            | TX_CTRL         | —               | —                        | Pull down to GND                   |
| 38            | RX_CTRL         | —               | —                        | —                                  |
| 39            | GPIO_0          | —               | —                        | Pull down to GND                   |
| 40            | GPIO_1          | —               | —                        | Pull down to GND                   |
| 41            | VDDIO           | SGMII_VDDIO     | —                        | VCCIO7 selectable                  |
| 42            | VDD1P0          | VCCA_1V_PHY     | —                        | 1.0 V Power                        |

| U7 Pin Number | U7 Signal Name | Net Name       | MachXO5-25 Ball Location | Application Notes                        |
|---------------|----------------|----------------|--------------------------|------------------------------------------|
| 43            | RESET#         | SGMII_RST_N    | T6                       | Default Pull down                        |
| 44            | INT/PWDN       | SGMII_INT      | T5                       | Default pull up. Shunt JP3 to pull down. |
| 45            | LED_2          | SGMII_LED_2    | —                        | Drive Red LED D15                        |
| 46            | LED_1          | SGMII_LED_1    | —                        | Drive Red LED D14                        |
| 47            | LED_0          | SGMII_LED_0    | —                        | Drive Red LED D13                        |
| 48            | VDDA1P8        | SGMII_PHY_D1V8 | —                        | 1.8 V Power                              |



## 7. HyperRAM

This section describes MachXO5-25 interconnection with 2 HyperRAM device on MachXO5-NX Development Board.

**Table 7.1. HyperRAM Pin Mapping**

| Cypress HyperRAM™ in 24-Ball FBGA |               | Connection for HyperRAM0 (U6) |                          | Connection for HyperRAM1 (U9) |                          |
|-----------------------------------|---------------|-------------------------------|--------------------------|-------------------------------|--------------------------|
| Symbol Name                       | Ball Location | Net Name                      | MachXO5-25 Ball Location | Net Name                      | MachXO5-25 Ball Location |
| RFU1                              | A2            | —                             | —                        | —                             | —                        |
| RFU2                              | A5            | —                             | —                        | —                             | —                        |
| CS#                               | A3            | HR0_CS                        | J3                       | HR1_CS                        | G6                       |
| RESET#                            | A4            | HR_RST                        | D2                       | HR_RST                        | D2                       |
| CK#                               | B1            | HR0_CKN                       | J1                       | HR1_CKN                       | K4                       |
| CK                                | B2            | HR0_CK                        | J2                       | HR1_CK                        | K5                       |
| VSS                               | B3            | GND                           | —                        | GND                           | —                        |
| VSSQ                              | C1            | GND                           | —                        | GND                           | —                        |
| VSSQ                              | E5            | GND                           | —                        | GND                           | —                        |
| VCC                               | B4            | VRAM                          | —                        | VRAM                          | —                        |
| VCCQ                              | E4            | VRAM                          | —                        | VRAM                          | —                        |
| VCCQ                              | D1            | VRAM                          | —                        | VRAM                          | —                        |
| RFU3                              | B5            | —                             | —                        | —                             | —                        |
| RFU4                              | C2            | —                             | —                        | —                             | —                        |
| RFU5                              | C5            | —                             | —                        | —                             | —                        |
| RWDS                              | C3            | HR0_RW                        | D1                       | HR1_RW                        | G5                       |
| DQ0                               | D3            | HR0_DQ0                       | H1                       | HR1_DQ0                       | E1                       |
| DQ1                               | D2            | HR0_DQ1                       | H2                       | HR1_DQ1                       | E2                       |
| DQ2                               | C4            | HR0_DQ2                       | J4                       | HR1_DQ2                       | E3                       |
| DQ3                               | D4            | HR0_DQ3                       | J5                       | HR1_DQ3                       | F1                       |
| DQ4                               | D5            | HR0_DQ4                       | J6                       | HR1_DQ4                       | G1                       |
| DQ5                               | E3            | HR0_DQ5                       | J7                       | HR1_DQ5                       | G2                       |
| DQ6                               | E2            | HR0_DQ6                       | J8                       | HR1_DQ6                       | G3                       |
| DQ7                               | E1            | HR0_DQ7                       | K8                       | HR1_DQ7                       | G4                       |

## 8. Generating the Programming File

The demo project on the MachXO5-NX Development Board Rev A board can be downloaded from the Lattice website (<https://www.latticesemi.com/products/developmentboardsandkits/machxo5-nx-development-board>).

To generate the JEDEC (.jed) file:

1. Open the Radiant software.
2. From the **File** menu, choose **Open > Project**.
3. In the **Open Project** dialog box, select the *test.rdf* file and click **Open**, as shown in Figure 8.1. This opens the demo project.

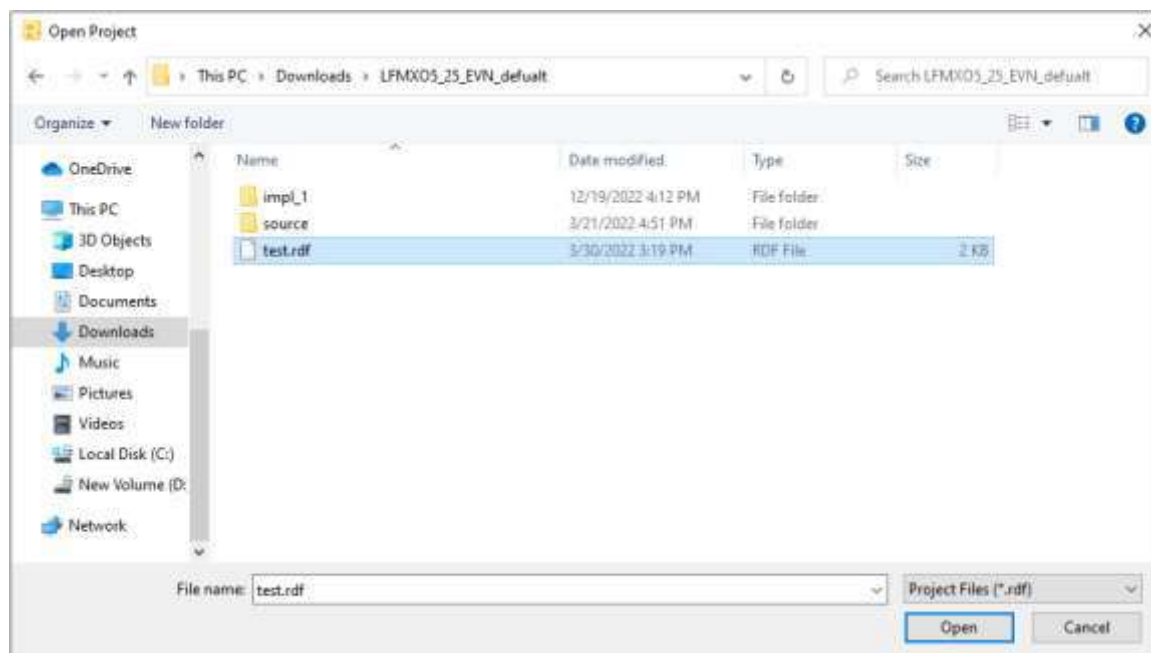
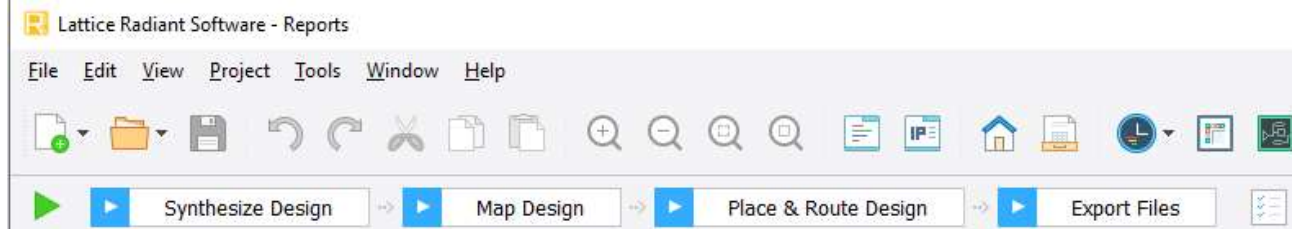


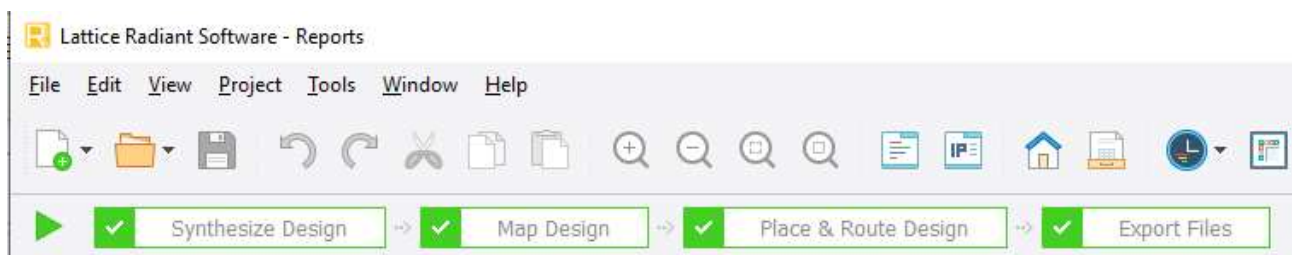
Figure 8.1. Radiant Software – Open Project Dialog Box

4. In the **Process Toolbar**, click **Run All** button , as shown in [Figure 8.2](#).



**Figure 8.2. Radiant Software – Process Toolbar initial state**

Green checkmarks appear on each successfully-completed step, including the generation of the JEDEC file, as shown in [Figure 8.3](#).



**Figure 8.3. Radiant Software –Processes Toolbar completed state**

The generated `.mcs` and `.jed` file are located in the `impl_1` folder.

## 9. Programming the MachXO5-NX Device

Radiant Programmer can be used to program the JEDEC file to the MachXO5-NX embedded flash after the JEDEC data file is generated, as shown in the [Generating the Programming File](#) section. Radiant Programmer is integrated into the Radiant software and is also available as a standalone version.

To program the MachXO5-NX embedded flash:

1. Connect the PC and MachXO5-NX Development Board (J11) using the USB cable.
2. In Radiant Software, click **Tools > Programmer**, as shown in [Figure 9.1](#).

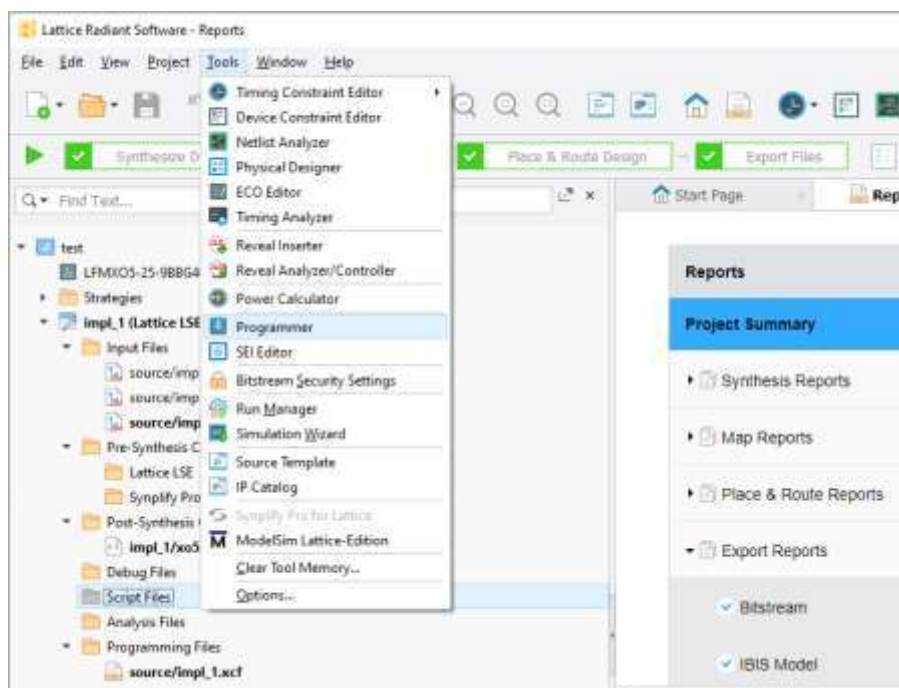


Figure 9.1. Radiant Software – Radiant Programmer

3. After the Radiant Programmer interface opens, as shown in [Figure 9.2](#), power up MachXO5-NX Development Board by correctly positioning power switch **SW6**.

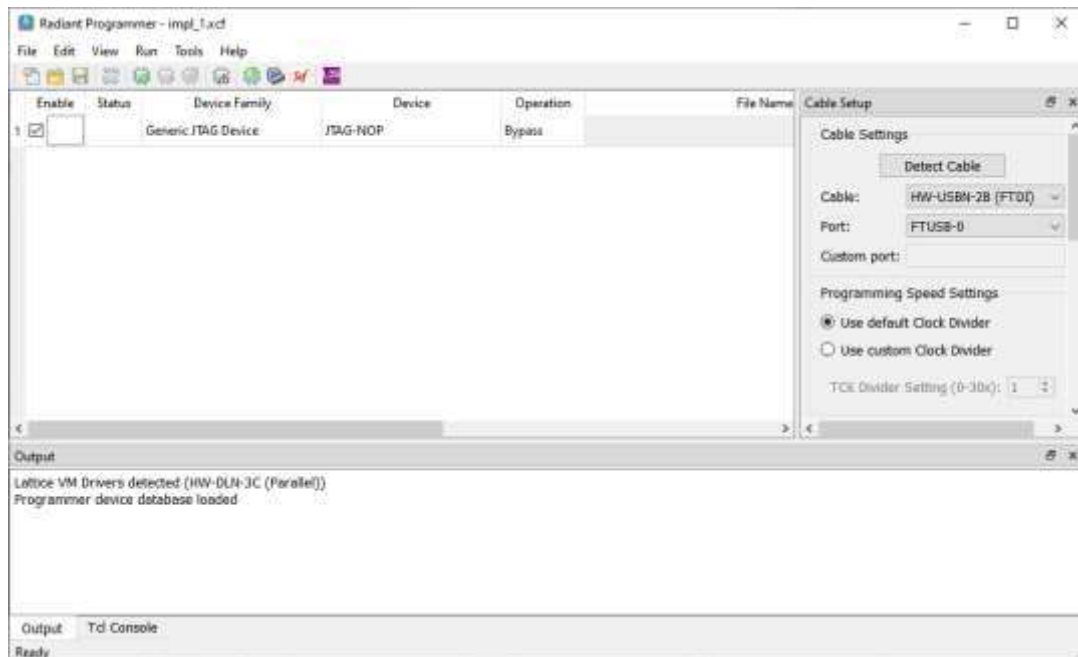


Figure 9.2. Radiant Programmer - Initial Opened

4. Click **Run > Scan Device** to check the board through FTUSB-0 Port of embedded HW-USB-2B(FTDI) cable, as shown in Figure 9.3. The MachXO5-NX device named as LFMXO5-25 should be detected on the JTAG chain as shown in Figure 9.4.

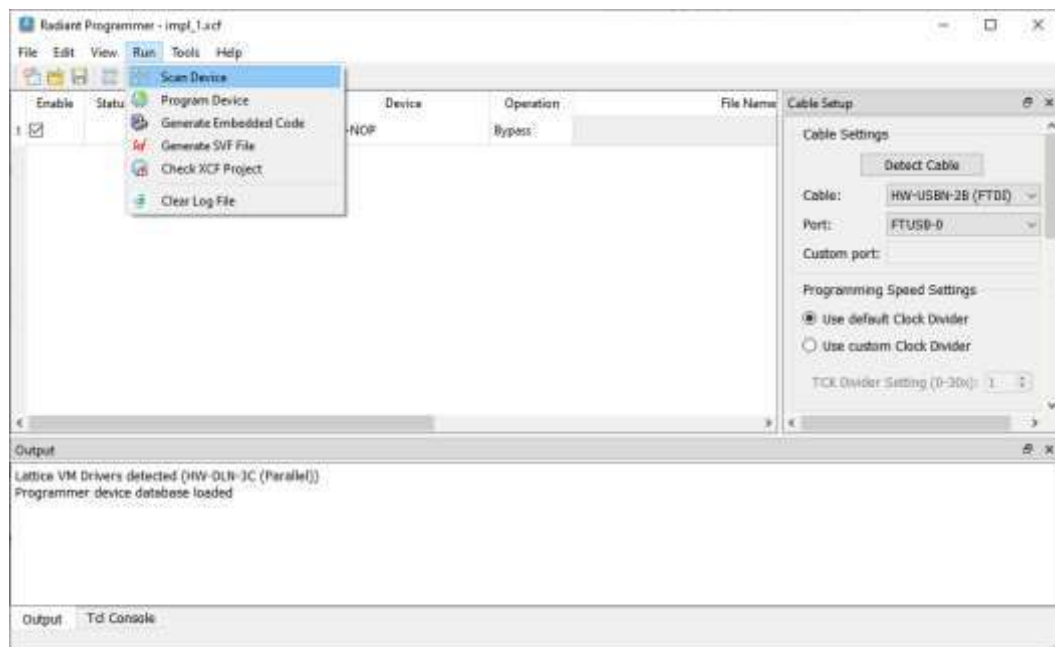


Figure 9.3. Radiant Programmer -Scan Device

5. Change the **Programming Speed Settings** in the **Cable Setup** pane on the right. Use **custom Clock Divider** option to increase the **TCK Divider Setting** to 3 or above, as shown in Figure 9.4.

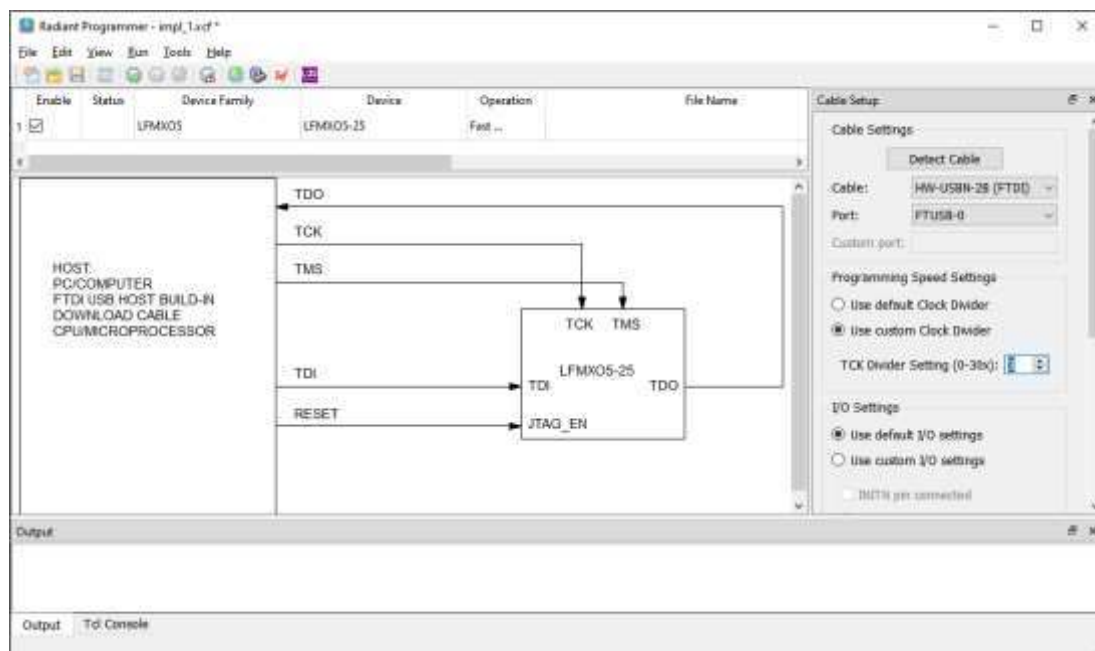


Figure 9.4. Radiant Programmer – Device Detected

6. Open the **Device Properties** dialog box by double click Operation column, as shown in Figure 9.5. Select the following options:

**Access mode – Flash Configuration Memory Port Interface – JTAG**

**Access Mode – Direct FLASH Programming**

**Operation – Erase,Program,Verify**

**Flash Header Programming Options** should be checked and select .mcs file for **Programming file**.

7. **CFGA Programming Options** should be check and select .jed file for **Programming file**. Click OK.

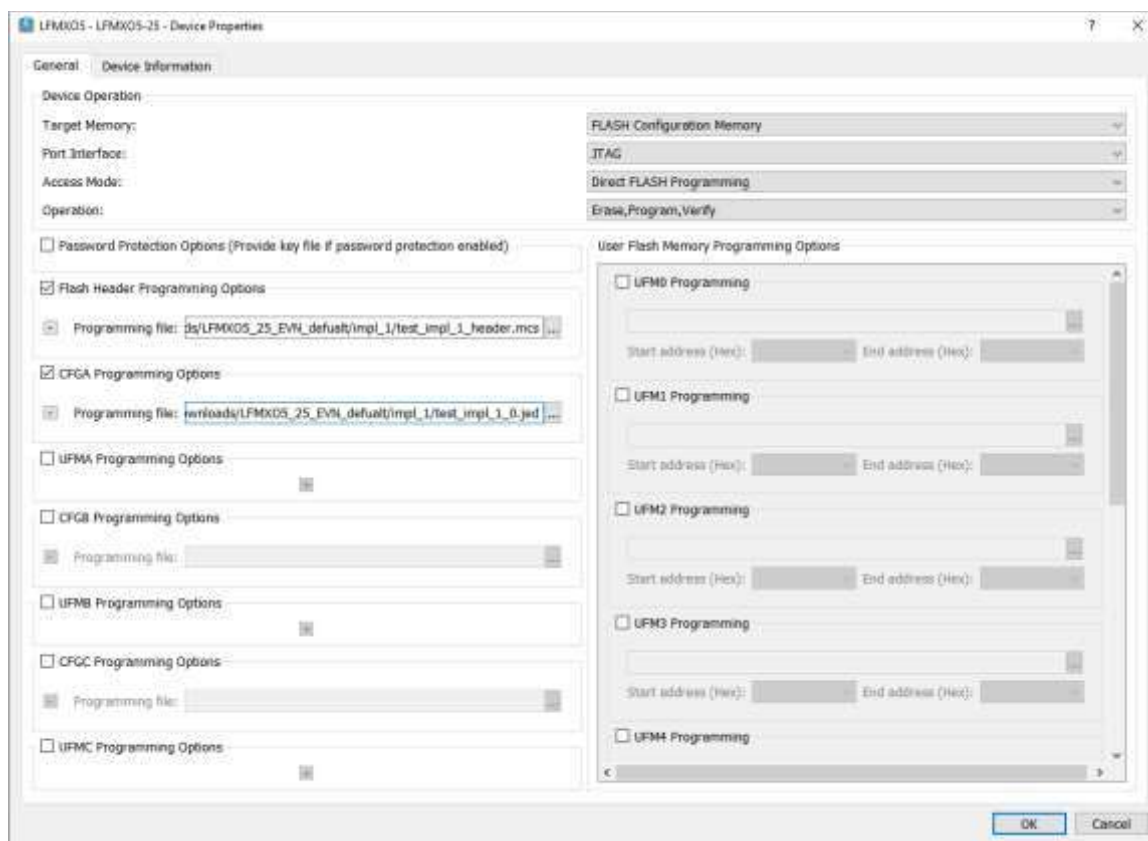


Figure 9.5. Radiant Programmer – Device Properties

8. To program the embedded Flash, click the **Program Device** button  in Radiant Programmer. If successful, the **Status** column shows **PASS**. The Output pane also shows INFO – Operation: successful.

## 10. Headers and Test Connections

This section describes the MachXO5-NX Development Board headers and test connections.

### 10.1. Versa Headers

The board provides two headers, J8 and J9, for expansion purpose.

**Table 10.1. Versa J8 Header Pin Connections**

| J8 Pin Number | Net Name      | MachXO5-25 Ball Location |
|---------------|---------------|--------------------------|
| 1             | GND           | —                        |
| 2             | NC            | —                        |
| 3             | EXPCON_2V5*   | —                        |
| 4             | EXPCON_IO29   | C20                      |
| 5             | EXPCON_IO30   | H14                      |
| 6             | EXPCON_IO31   | G14                      |
| 7             | EXPCON_IO32   | H15                      |
| 8             | EXPCON_IO33   | G18                      |
| 9             | EXPCON_IO34   | H16                      |
| 10            | EXPCON_IO35   | G19                      |
| 11            | EXPCON_IO36   | H20                      |
| 12            | EXPCON_IO37   | H19                      |
| 13            | EXPCON_IO38   | J17                      |
| 14            | EXPCON_IO39   | J18                      |
| 15            | EXPCON_IO40   | J15                      |
| 16            | EXPCON_IO41   | J16                      |
| 17            | EXPCON_IO42   | J13                      |
| 18            | EXPCON_IO43   | J14                      |
| 19            | EXPCON_IO44   | J12                      |
| 20            | EXPCON_IO45   | H13                      |
| 21            | 5VIN*         | —                        |
| 22            | GND           | —                        |
| 23            | EXPCON_2V5*   | —                        |
| 24            | GND           | —                        |
| 25            | +3.3V         | —                        |
| 26            | GND           | —                        |
| 27            | +3.3V         | —                        |
| 28            | GND           | —                        |
| 29            | EXPCON_OSC    | E16                      |
| 30            | GND           | —                        |
| 31            | EXPCON_CLKIN  | E17                      |
| 32            | GND           | —                        |
| 33            | EXPCON_CLKOUT | D20                      |
| 34            | GND           | —                        |
| 35            | EXPCON_3V3**  | —                        |
| 36            | GND           | —                        |



| J8 Pin Number | Net Name     | MachXO5-25 Ball Location |
|---------------|--------------|--------------------------|
| 37            | EXPCON_3V3** | —                        |
| 38            | GND          | —                        |
| 39            | EXPCON_3V3** | —                        |
| 40            | GND          | —                        |

**Notes:**

\* Net is optionally connected to power source through resistor DNI.

\*\* Net is optionally connected to power source through resistor DI.

**Table 10.2. Versa J9 Header Pin Connections**

| J9 Pin Number | Net Name     | MachXO5-25 Ball Location |
|---------------|--------------|--------------------------|
| 1             | HPE_RESOUT#  | F5                       |
| 2             | GND          | —                        |
| 3             | EXPCON_IO0   | D3                       |
| 4             | EXPCON_IO1   | E4                       |
| 5             | EXPCON_IO2   | C3                       |
| 6             | EXPCON_IO3   | C2                       |
| 7             | EXPCON_IO4   | A4                       |
| 8             | EXPCON_IO5   | E5                       |
| 9             | EXPCON_IO6   | F6                       |
| 10            | EXPCON_IO7   | C5                       |
| 11            | EXPCON_IO8   | B2                       |
| 12            | EXPCON_IO9   | A2                       |
| 13            | EXPCON_IO10  | B3                       |
| 14            | EXPCON_IO11  | A3                       |
| 15            | EXPCON_IO12  | B4                       |
| 16            | EXPCON_IO13  | D5                       |
| 17            | EXPCON_IO14  | A5                       |
| 18            | EXPCON_IO15  | B5                       |
| 19            | GND          | —                        |
| 20            | EXPCON_3V3** | —                        |
| 21            | EXPCON_IO16  | A6                       |
| 22            | GND          | —                        |
| 23            | EXPCON_IO17  | B6                       |
| 24            | GND          | —                        |
| 25            | EXPCON_IO18  | A7                       |
| 26            | GND          | —                        |
| 27            | EXPCON_IO19  | A8                       |
| 28            | EXPCON_IO20  | C6                       |
| 29            | EXPCON_IO21  | B8                       |
| 30            | GND          | —                        |
| 31            | EXPCON_IO22  | B9                       |
| 32            | EXPCON_IO23  | A9                       |
| 33            | EXPCON_IO24  | D6                       |
| 34            | GND          | —                        |

| J9 Pin Number | Net Name    | MachXO5-25 Ball Location |
|---------------|-------------|--------------------------|
| 35            | EXPCON_IO25 | C8                       |
| 36            | EXPCON_IO26 | E7                       |
| 37            | EXPCON_IO27 | E8                       |
| 38            | CARDSEL#*   | —                        |
| 39            | EXPCON_IO28 | E6                       |
| 40            | GND         | —                        |

**Notes:**

\* Net is optionally connected to power source through resistor DNI.

\*\* Net is optionally connected to power source through resistor DI.

## 10.2. Arduino Board GPIO Headers

The board provides four headers, J2, J3, J4, and J5, for Arduino Zero board adaption.

**Table 10.3. Arduino J2 Pin Connections**

| J2 Pin Number | Net Name     | Arduino ZERO Board Signal | MachXO5-25 Ball Location | Comments                                                                                              |
|---------------|--------------|---------------------------|--------------------------|-------------------------------------------------------------------------------------------------------|
| 1             | AR_IO8       | ~D8/PA06                  | L12                      | —                                                                                                     |
| 2             | AR_IO9       | ~D9/PA07                  | L13                      | —                                                                                                     |
| 3             | AR_SS_IO10   | ~D10/PA18/SS              | L14                      | Defaults to SS function on Arduino ZERO Board.                                                        |
| 4             | AR_MOSI_IO11 | ~D11/PA16/COPI            | L15                      | Defaults to COPI function on Arduino ZERO Board.                                                      |
| 5             | AR_MISO_IO12 | ~D12/PA19/CIPO            | L16                      | Defaults to CIPO function on Arduino ZERO Board.                                                      |
| 6             | AR_SCK_IO13  | ~D13/PA17/SCK             | K19                      | Defaults to SCK function on Arduino ZERO Board.                                                       |
| 7             | GND          | GND                       | —                        | —                                                                                                     |
| 8             | AR_AREF      | AREF/PA03                 | L19                      | AR_AREF connection to AREF through R43.                                                               |
| 9             | AR_SDA       | D20/PA22/SDA              | N18                      | Defaults to SDA function on Arduino ZERO Board. It is optionally connected to SDA0 through R44 (DNI). |
| 10            | AR_SCL       | D21/PA23/SCL              | N19                      | Defaults to SCL function on Arduino ZERO Board. It is optionally connected to SCL0 through R45 (DNI). |

**Table 10.4. Arduino J3 Pin Connections**

| J3 Pin Number | Net Name | Arduino ZERO Board Signal | MachXO5-25 Ball Location | Comments |
|---------------|----------|---------------------------|--------------------------|----------|
| 1             | AR_IO0   | D0/RX/PA11                | J19                      | —        |
| 2             | AR_IO1   | D1//TX/PA10               | J20                      | —        |
| 3             | AR_IO2   | D2/PA14                   | K12                      | —        |
| 4             | AR_IO3   | ~D3/PA09                  | K13                      | —        |
| 5             | AR_IO4   | ~D4/PA08                  | K14                      | —        |
| 6             | AR_IO5   | ~D5/PA15                  | K15                      | —        |
| 7             | AR_IO6   | ~D6/PA20                  | K16                      | —        |
| 8             | AR_IO7   | D7/PA21                   | K17                      | —        |

**Table 10.5. Arduino J4 Pin Connections**

| J4 Pin Number | Net Name | Arduino ZERO Board Signal | MachXO5-25 Ball Location | Comments                                                                                        |
|---------------|----------|---------------------------|--------------------------|-------------------------------------------------------------------------------------------------|
| 1             | AR_IO14  | ATN                       | L20                      | —                                                                                               |
| 2             | NC       | IOREF                     | —                        | —                                                                                               |
| 3             | AR_RESET | RESET                     | K20                      | Pin U20 should be set high by default. Avoid Arduino ZERO board in Reset status when connected. |
| 4             | +3.3V_AR | +3V3                      | —                        | 3.3 V power supply from Arduino ZERO board.                                                     |
| 5             | AR_5V    | +5V                       | —                        | Jump to 5 V onboard power rail through JP6.                                                     |
| 6             | GND      | GND                       | —                        | —                                                                                               |
| 7             | GND      | GND                       | —                        | —                                                                                               |
| 8             | +12V     | VIN                       | —                        | Share with +12V onboard power rail.                                                             |

**Note:**

If JP6 is installed, 5 V power can be supplied from either the Arduino board or the MachXO5-NX Development Board. With JP6 removed, both boards need their own 5 V power.

**Table 10.6. Arduino J5 Pin Connections**

| J5 Pin Number | Net Name | Arduino ZERO Board Signal | MachXO5-25 Ball Location | Comments                               |
|---------------|----------|---------------------------|--------------------------|----------------------------------------|
| 1             | AR_AD0   | D14/ADC0/PA02             | M11                      | Defaults to ADC0 on Arduino ZERO Board |
| 2             | AR_AD1   | D15/ADC1/PB08             | M12                      | Defaults to ADC1 on Arduino ZERO Board |
| 3             | AR_AD2   | D16/ADC2/PB09             | M13                      | Defaults to ADC2 on Arduino ZERO Board |
| 4             | AR_AD3   | D17/ADC3/PA04             | M14                      | Defaults to ADC3 on Arduino ZERO Board |
| 5             | AR_AD4   | D18/ADC4/PA05             | M17                      | Defaults to ADC4 on Arduino ZERO Board |
| 6             | AR_AD5   | D19/ADC5/PB02             | M18                      | Defaults to ADC5 on Arduino ZERO Board |

## 10.3. FX12 Headers

The board provides two headers, U4 and U5, to connect to FX12 compatible boards or cables. Each header has eight pairs of Low-Voltage Differential Signaling (LVDS) signals for high-speed data receiver.

**Table 10.7. FX12 U4 Header Pin Connections**

| U4 Pin Number | Net Name    | MachXO5-25 Ball Location |
|---------------|-------------|--------------------------|
| 1             | CH0_DCK_P   | W7                       |
| 2             | CH0_DCK_N   | Y7                       |
| 3             | GND         | —                        |
| 4             | CH0_DATA0_P | T8                       |
| 5             | CH0_DATA0_N | U8                       |
| 6             | GND         | —                        |
| 7             | CH0_DATA2_P | R10                      |
| 8             | CH0_DATA2_N | T10                      |
| 9             | GND         | —                        |
| 10            | FX_SN       | V3                       |
| 11            | FX_SCLK     | V4                       |
| 12            | PWR_12V**   | —                        |
| 13            | SDA2        | R6                       |
| 14            | SCL2        | R7                       |
| 15            | GND         | —                        |
| 16            | CH2_DATA0_P | N10                      |
| 17            | CH2_DATA0_N | P10                      |

| U4 Pin Number | Net Name    | MachXO5-25 Ball Location |
|---------------|-------------|--------------------------|
| 18            | GND         | —                        |
| 19            | CH2_DCK_P   | W8                       |
| 20            | CH2_DCK_N   | Y8                       |
| 21            | PWR_12V**   | —                        |
| 22            | RESETN      | V2                       |
| 23            | PWR_5-0V*   | —                        |
| 24            | CH0_DATA1_P | W9                       |
| 25            | CH0_DATA1_N | Y9                       |
| 26            | PWR_3-3V*   | —                        |
| 27            | CH0_DATA3_P | W10                      |
| 28            | CH0_DATA3_N | Y10                      |
| 29            | PWR_1-8V*   | —                        |
| 30            | FX_MOSI     | U5                       |
| 31            | FX_MISO     | U6                       |
| 32            | PWR_1-8V*   | —                        |
| 33            | GND         | —                        |
| 34            | GND         | —                        |
| 35            | PWR_3-3V*   | —                        |
| 36            | CH2_DATA1_P | U10                      |
| 37            | CH2_DATA1_N | V10                      |
| 38            | PWR_5-0V*   | —                        |
| 39            | SDA1        | R4                       |
| 40            | SCL1        | R5                       |

**Notes:**

\* Signal is optionally connected to power source through resistor DNI.

\*\* 12 V power needs external supply from pin 8 of J4.

**Table 10.8. FX12 U5 Header Pin Connections**

| U5 Pin Number | Net Name    | MachXO5-25 Ball Location |
|---------------|-------------|--------------------------|
| 1             | CH1_DCK_P   | Y11                      |
| 2             | CH1_DCK_N   | W11                      |
| 3             | GND         | —                        |
| 4             | CH1_DATA0_P | V11                      |
| 5             | CH1_DATA0_N | U11                      |
| 6             | GND         | —                        |
| 7             | CH1_DATA2_P | V12                      |
| 8             | CH1_DATA2_N | U12                      |
| 9             | GND         | —                        |
| 10            | FX_SN       | V3                       |
| 11            | FX_SCLK     | V4                       |
| 12            | PWR_12V**   | —                        |
| 13            | SDA2        | R6                       |
| 14            | SCL2        | R7                       |
| 15            | GND         | —                        |
| 16            | CH3_DATA0_P | T11                      |
| 17            | CH3_DATA0_N | R11                      |
| 18            | GND         | —                        |
| 19            | CH3_DCK_P   | Y12                      |
| 20            | CH3_DCK_N   | W12                      |

| U5 Pin Number | Net Name    | MachXO5-25 Ball Location |
|---------------|-------------|--------------------------|
| 21            | PWR_12V**   | —                        |
| 22            | RESETN      | V2                       |
| 23            | PWR_5-0V*   | —                        |
| 24            | CH1_DATA1_P | Y14                      |
| 25            | CH1_DATA1_N | W14                      |
| 26            | PWR_3-3V*   | —                        |
| 27            | CH1_DATA3_P | Y13                      |
| 28            | CH1_DATA3_N | W13                      |
| 29            | PWR_1-8V    | —                        |
| 30            | FX_MOSI     | U5                       |
| 31            | FX_MISO     | U6                       |
| 32            | PWR_1-8V*   | —                        |
| 33            | GND         | —                        |
| 34            | GND         | —                        |
| 35            | PWR_3-3V*   | —                        |
| 36            | CH3_DATA1_P | N11                      |
| 37            | CH3_DATA1_N | P11                      |
| 38            | PWR_5-0V*   | —                        |
| 39            | SDA1        | R4                       |
| 40            | SCL1        | R5                       |

**Notes:**

\* Signal is optionally connected to power source through resistor DNI.

\*\* 12 V power needs external supply from pin 8 of J4.

## 10.4. Aardvark Header (DNI)

The Aardvark I<sup>2</sup>C/SPI Host Adapter is a fast and powerful I<sup>2</sup>C bus and SPI bus host adapter through USB. It allows you to interface a Windows, Linux, or Mac OS X PC through USB to a downstream embedded system environment and transfer serial messages using the I<sup>2</sup>C and SPI protocols.

The MachXO5-NX Development Board provides an Aardvark compatible header for customer applications. The I<sup>2</sup>C bus is optional connecting to a global I<sup>2</sup>C bus on the board.

**Table 10.9. Aardvark J7 Header Pin Connections**

| J7 Pin Number | Net Name | MachXO5-25 Ball Location |
|---------------|----------|--------------------------|
| 1             | AK_SCL   | M19                      |
| 2             | GND      | —                        |
| 3             | AK_SDA   | M20                      |
| 4             | +5V_I2C  | —                        |
| 5             | AK_MISO  | N14                      |
| 6             | +5V_SPI  | —                        |
| 7             | AK_SCLK  | N15                      |
| 8             | AK_MOSI  | N17                      |
| 9             | AK_SS    | N16                      |
| 10            | GND      | —                        |

## 10.5. Raspberry Pi Board GPIO Header

The MachXO5-NX Development Board provides a 40-pin receptacle that is compatible with the GPIO header of Raspberry Pi 2/3 serial models.

**Table 10.10. Raspberry Pi J6 Header Pin Connections**

| J6 Pin Number | Net Name   | MachXO5-25 Ball Location |
|---------------|------------|--------------------------|
| 1             | 3.3V_RASP* | —                        |
| 2             | RASP_5V**  | —                        |
| 3             | RASP_IO02  | L8                       |
| 4             | RASP_5V**  | —                        |
| 5             | RASP_IO03  | L7                       |
| 6             | GND        | —                        |
| 7             | RASP_IO04  | L6                       |
| 8             | RASP_IO14  | M7                       |
| 9             | GND        | —                        |
| 10            | RASP_IO15  | K3                       |
| 11            | RASP_IO17  | L5                       |
| 12            | RASP_IO18  | M6                       |
| 13            | RASP_IO27  | L4                       |
| 14            | GND        | —                        |
| 15            | RASP_IO22  | L2                       |
| 16            | RASP_IO23  | L3                       |
| 17            | 3.3V_RASP* | —                        |
| 18            | RASP_IO24  | L1                       |
| 19            | RASP_IO10  | M2                       |
| 20            | GND        | —                        |
| 21            | RASP_IO09  | M1                       |
| 22            | RASP_IO25  | N2                       |
| 23            | RASP_IO11  | N1                       |
| 24            | RASP_IO08  | P2                       |
| 25            | GND        | —                        |
| 26            | RASP_IO07  | P1                       |
| 27            | RASP_ID_SD | K2                       |
| 28            | RASP_ID_SC | K1                       |
| 29            | RASP_IO05  | N3                       |
| 30            | GND        | —                        |
| 31            | RASP_IO06  | N4                       |
| 32            | RASP_IO12  | P3                       |
| 33            | RASP_IO13  | P4                       |
| 34            | GND        | —                        |
| 35            | RASP_IO19  | P5                       |
| 36            | RASP_IO16  | M5                       |
| 37            | RASP_IO26  | P6                       |
| 38            | RASP_IO20  | N7                       |
| 39            | GND        | —                        |

| J6 Pin Number | Net Name  | MachXO5-25 Ball Location |
|---------------|-----------|--------------------------|
| 40            | RASP_IO21 | M8                       |

**Notes:**

\* 3.3 V power is supplied from Raspberry Pi board.

\*\* 5 V power can come from either the Raspberry Pi board or the MachXO5-NX Development Board when jumper JP7 is installed. When jumper JP7 is not installed, both boards need their own 5 V power.

## 10.6. PMOD Headers

The MachXO5-NX Development Board provides two 12-pin receptacle headers that is compatible with the Digilent PMOD™ interface spec.

**Table 10.11. J15 Header Pin Connections**

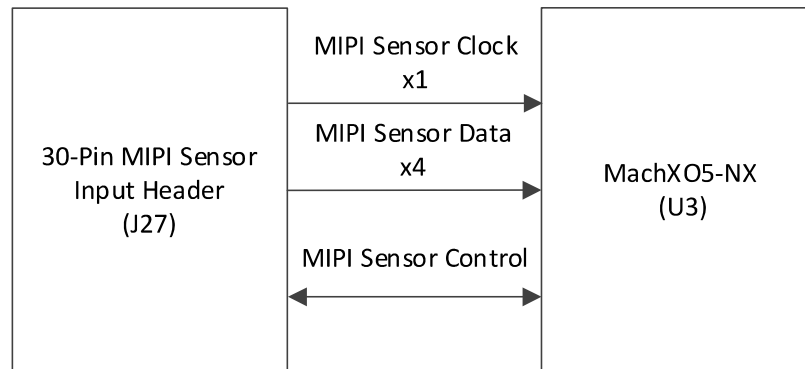
| J15 Pin Number | Net Name | MachXO5-25 Ball Location |
|----------------|----------|--------------------------|
| 1              | PMOD0_1  | G7                       |
| 2              | PMOD0_2  | G9                       |
| 3              | PMOD0_3  | G8                       |
| 4              | PMOD0_4  | H8                       |
| 5              | GND      | —                        |
| 6              | VCCIO0   | —                        |
| 7              | PMOD0_5  | F7                       |
| 8              | PMOD0_6  | F9                       |
| 9              | PMOD0_7  | F8                       |
| 10             | PMOD0_8  | H9                       |
| 11             | GND      | —                        |
| 12             | VCCIO0   | —                        |

**Table 10.12. J16 Header Pin Connections**

| J16 Pin Number | Net Name | MachXO5-25 Ball Location |
|----------------|----------|--------------------------|
| 1              | PMOD1_1  | E11                      |
| 2              | PMOD1_2  | D13                      |
| 3              | PMOD1_3  | D15                      |
| 4              | PMOD1_4  | C16                      |
| 5              | GND      | —                        |
| 6              | VCCIO1   | —                        |
| 7              | PMOD1_5  | D11                      |
| 8              | PMOD1_6  | C13                      |
| 9              | PMOD1_7  | C15                      |
| 10             | PMOD1_8  | D16                      |
| 11             | GND      | —                        |
| 12             | VCCIO1   | —                        |

## 10.7. MIPI Camera Header

The MachXO5-NX Development Board support MIPI Camera sensor input with soft D-PHY. [Figure 10.1](#) shows the block diagram of the MIPI Camera Sensor interface on the board. The data path interface between the camera sensor module and MachXO5-25 is CSI-2. The cameras are configured from the MachXO5-25 device through the MIPI Sensor Control interface including I<sup>2</sup>C, frame sync, and reset signals drive the camera.



**Figure 10.1. MIPI Camera Sensor Interface**

MachXO5-NX Development Board supports a 30-pin Kyocera header footprint of 245804030000829+ for MIPI Camera sensor input. Table 10.13 show the signal assignment for the MIPI Camera sensor input Header of J27. Use J24 as described in Figure 10.2 to select Camera CVDD power for Pin 25 of J8.

**Table 10.13. MIPI Camera Sensor Interconnections**

| MIPI Camera Sensor Input Header (J8) Pin Number | Net Name       | MachXO5-25 Ball Location |
|-------------------------------------------------|----------------|--------------------------|
| 1                                               | NC             | —                        |
| 2                                               | DPHY0_CKN      | R14                      |
| 3                                               | DPHY0_CKP      | T14                      |
| 4                                               | GND            | —                        |
| 5                                               | DPHY0_DN3      | N12                      |
| 6                                               | DPHY0_DP3      | N13                      |
| 7                                               | GND            | —                        |
| 8                                               | DPHY0_DN1      | R13                      |
| 9                                               | DPHY0_DP1      | P13                      |
| 10                                              | GND            | —                        |
| 11                                              | DPHY0_DN0      | T13                      |
| 12                                              | DPHY0_DP0      | U13                      |
| 13                                              | GND            | —                        |
| 14                                              | DPHY0_DN2      | U14                      |
| 15                                              | DPHY0_DP2      | V13                      |
| 16                                              | GND            | —                        |
| 17                                              | GND            | —                        |
| 18                                              | VDD2V8         | —                        |
| 19                                              | NC             | —                        |
| 20                                              | DPHY0_CLK      | K7                       |
| 21                                              | DPHY0_FSYNC    | K6                       |
| 22                                              | DPHY0_SDA      | H5                       |
| 23                                              | DPHY0_SCL      | H6                       |
| 24                                              | DPHY0_RST      | H7                       |
| 25                                              | CVDD           | —                        |
| 26                                              | VRAM (DVDD1V8) | —                        |
| 27                                              | GND            | —                        |
| 28                                              | GND            | —                        |
| 29                                              | AVDD2V8        | —                        |
| 30                                              | GND            | —                        |



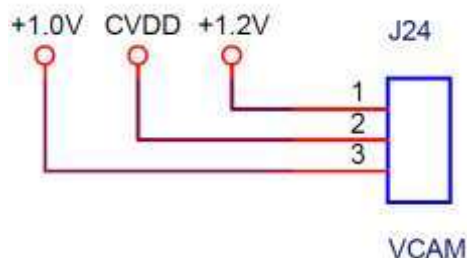


Figure 10.2. MIPI Camera Sensor Power Supply Header

## 10.8. User I<sup>2</sup>C Interface

This board provides more options for user I<sup>2</sup>C access from different MachXO5-25 Wide Range I/O to multiple onboard headers. They are solid connected for target applications, but those connections to bridge SDA0/SCL0 are not populated in default. You need to build your interconnection for I<sup>2</sup>C applications across the board. For example, if you want to use an Ardvark I<sup>2</sup>C host to access FX12 adapt board, you can use internal fabric logic of MachXO5-25 to bridge AK\_SCL/AK\_SDA with SCL1/SDA1 and SCL2/SDA2, or add bridge resistors according to Table 10.14 to connect all of them to SCL0/SDA0 for bridge interconnections on board without involvement of FPGA. You also need to setup the design with tri-state mode for outputting high with pull up resistors. If there is no pull up setup on the counterpart boards or internal GPIOs of FPGA, you can add JP12 and JP13 to leverage the R33 and R34 for pulling up bridge SCL0/SDA0 to selectable VCCIO2. Take care that the DPHY0\_SCL/DPHY0\_SDA are special case. They need dedicate pull up resistors R233/R234 due to they are supported from 1.8 V I/O Bank 9. Also, R233/R234 can be used to pull up SCL0/SDA0 by adding R229/R228 when Bank 7 is selected to support 1.8 V for FX12 header I<sup>2</sup>C control. At this time, JP12 and JP13 should be removed and R224/R225 or R226/R227 should be added to leverage the 1.8 V pull up for I/O Bank 7.

Table 10.14. I<sup>2</sup>C Connections

| Extend header            | MachXO5-25 Bank | MachXO5-25 Ball Location for JTAG | Net Name    | Bridge Resistor to SCL0/SDA0 |
|--------------------------|-----------------|-----------------------------------|-------------|------------------------------|
| Versa Header (J9)        | 0               | D5                                | EXPCON_IO13 | R35 (DNI)                    |
|                          |                 | B5                                | EXPCON_IO15 | R37 (DNI)                    |
| Aardvark Header (J7)     | 3               | M19                               | AK_SCL      | R231 (DNI)                   |
|                          |                 | M20                               | AK_SDA      | R230 (DNI)                   |
| Arduino Header (J2)      | 3               | N19                               | AR_SCL      | R45 (DNI)                    |
|                          |                 | N18                               | AR_SDA      | R44 (DNI)                    |
| FX12 Headers (U4/U5)     | 7               | R5                                | SCL1        | R224 (DNI)                   |
|                          |                 | R4                                | SDA1        | R225 (DNI)                   |
| FX12 Headers (U4/U5)     | 7               | R7                                | SCL2        | R226 (DNI)                   |
|                          |                 | R6                                | SDA2        | R227 (DNI)                   |
| Raspberry Pi Header (J6) | 8               | K1                                | RASP_ID_SC  | R85 (DNI)                    |
|                          |                 | K2                                | RASP_ID_SD  | R87 (DNI)                    |
| Raspberry Pi Header (J6) | 8               | L7                                | RASP_IO03   | R96 (DNI)                    |
|                          |                 | L8                                | RASP_IO02   | R84 (DNI)                    |
| Camera Header (J27)      | 9               | H6                                | DPHY0_SCL   | R229 (DNI)                   |
|                          |                 | H5                                | DPHY0_SDA   | R228 (DNI)                   |

## 10.9. ADC and Potentiometer

There are two dedicate ADC input pairs for MachXO5-25. This board provides multiple application options. For default population, one pair of ADC0 is used to measure the core VCC voltage drop through a 10 mΩ resistor R112. Therefore, the core VCC current is calculable, as shown in Figure 10.3. Positive input of another pair ADC1 is connected to a 10 kΩ Trimmer Potentiometers (POT1) which provides voltage variation from 0 V to selectable VCCIO4, as shown in Figure 10.4. The negative input of ADC1 is grounded through 1 kΩ resistor.

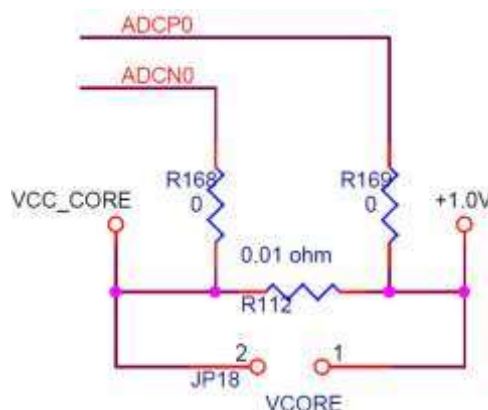


Figure 10.3. Circuit Design for ADC0

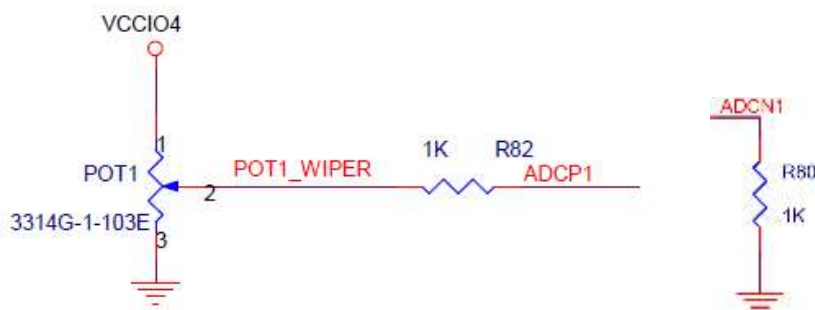


Figure 10.4. Circuit Design for ADC1

Rotate the Trimmer clockwise to decrease the voltage, as shown in Figure 10.5. To increase the voltage to ADCP1, rotate the POT counter-clockwise.

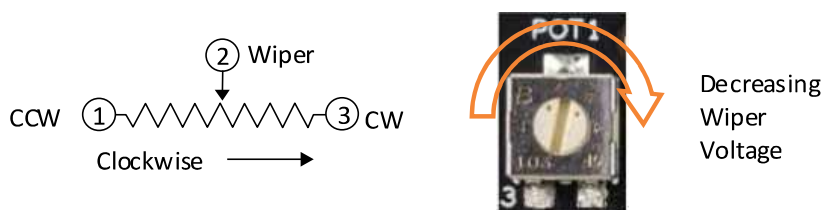


Figure 10.5. Trimmer Wiper Description

Optionally, both ADC pairs are also routed to PMOD like header J28. For their signal assignment, refer to [Table 10.15](#).

**Table 10.15. J28 (DNI) Header Pin Connections**

| J28 Pin Number | Net Name | MachXO5-25 Ball Location | Application Notes          |
|----------------|----------|--------------------------|----------------------------|
| 1              | MDIR0    | W1                       | Within IO Bank 7           |
| 2              | MEN0     | V5                       | Within IO Bank 7           |
| 3              | ADCP0    | Y16                      | Remove R168 for separation |
| 4              | ADCN0    | Y17                      | Remove R169 for separation |
| 5              | GND      | —                        | —                          |
| 6              | VCCIO7   | —                        | 1.8V/3.3V selectable       |
| 7              | MDIR1    | W2                       | Within IO Bank 7           |
| 8              | MEN1     | V6                       | Within IO Bank 7           |
| 9              | ADCP1    | Y18                      | Remove R82 for separation  |
| 10             | ADCN1    | Y19                      | Remove R80 for separation  |
| 11             | GND      | —                        | —                          |
| 12             | VCCIO7   | —                        | 1.8V/3.3V selectable       |

## 10.10. Other Test Points

The MachXO5-NX Development Board provides some test points for user flexibility.

**Table 10.16. Test Point Connections**

| Test Point | Net Name    | MachXO5-25 Ball Location |
|------------|-------------|--------------------------|
| TP1        | PMU_WAKEUPN | G17                      |
| TP2        | TP2         | K18                      |

## 11. LEDs and Switches

LEDs and switches of the MachXO5-NX Development Board that can be used in demo and customer designs are described in this section.

### 11.1. Four-Position DIP Switch

Four MachXO5-25 pins are connected to the four switches of SW1, as shown in the circuit design in Figure 11.1. The CTS side actuated DIP switches are connected to logic level 0 when in the ON position, as shown in Figure 11.2.

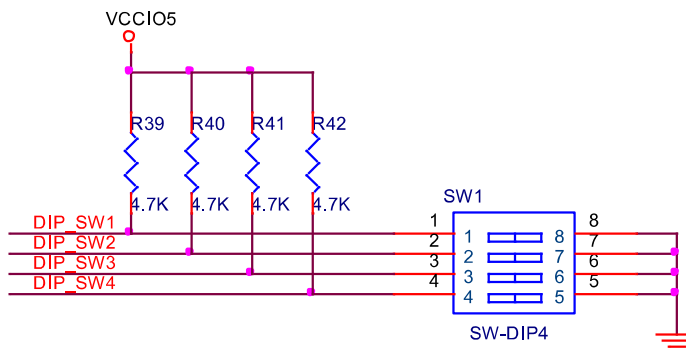


Figure 11.1. Four-Position DIP Switch Circuits



Figure 11.2. Four-position DIP Switch

One side of each switch is connected to GPIOs within the VCCIO5 bank and pulled up through 4.7 kΩ resistors. The other side is grounded. The designated pins are connected, as shown in Table 11.1.

Table 11.1. Four-Position DIP Switch Signals

| Net Name | MachXO5-25 Ball Location | SW1 DIP Switch Position | 4.7 kΩ Pull up Resistor | Logic Level at ON Position |
|----------|--------------------------|-------------------------|-------------------------|----------------------------|
| DIP_SW1  | T1                       | 1                       | R39                     | 0                          |
| DIP_SW2  | T2                       | 2                       | R40                     | 0                          |
| DIP_SW3  | T3                       | 3                       | R41                     | 0                          |
| DIP_SW4  | T4                       | 4                       | R42                     | 0                          |

### 11.2. General Purpose Push Buttons

The MachXO5-NX Development Board provides four push button switches, SW2, SW3, SW4 and SW5, for demos and user applications. Pressing these buttons drives a logic level 0 to the corresponding I/O pins.

**Table 11.2. Push Button Switch Signals**

| Push Button Ref Name | Net Name | MachXO5-25 Ball Location | Test Points  |
|----------------------|----------|--------------------------|--------------|
| SW2                  | PB1      | E19                      | TP3          |
| SW3                  | PB2      | F20                      | TP4          |
| SW4                  | PB3      | B7                       | Pin 2 of JP4 |
| SW5                  | PB4      | G20                      | Pin 2 of JP5 |

SW2 and SW3 are designed for general-purpose applications. SW4 and SW5 are designed with additional jumper JP4 and JP5. SW4 can be used as ASC global reset push button when JP4 is set to connect with EXPCON\_IO20, which is connect to MANDATORY\_RESET signal when mated with Lattice ASC Bridge Board. Refer to [ASC Bridge Board Evaluation Board User Guide \(FPGA-EB-02025\)](#) for detailed information with ASC application. SW5 can be used as PROGRAMN push button when JP5 is set to trigger the configuration process without power cycle. For detailed information on PROGRAMN, refer to [MachXO5 Programming and Configuration User Guide \(FPGA-TN-02271\)](#).

### 11.3. General Purpose LEDs

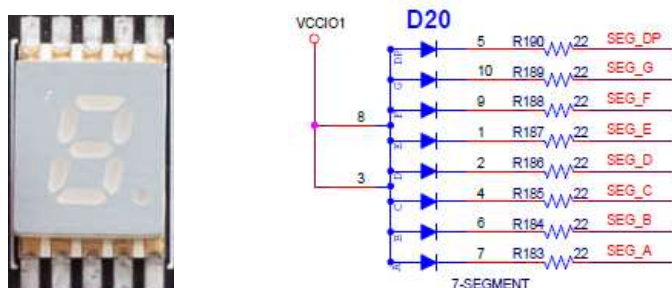
The MachXO5-NX Development Board provides eight red LEDs that are connected to I/O within Bank 5. The LEDs are lighted when the output is driven LOW. [Table 11.3](#) lists the red LEDs and their associated pins.

**Table 11.3. LED Signals**

| Red LEDs Ref Name | Net Name | MachXO5-25 Ball Location |
|-------------------|----------|--------------------------|
| D1                | XLED0    | R3                       |
| D2                | XLED1    | R2                       |
| D3                | XLED2    | R1                       |
| D4                | XLED3    | P7                       |
| D5                | XLED4    | H12                      |
| D6                | XLED5    | H11                      |
| D7                | XLED6    | G13                      |
| D8                | XLED7    | G12                      |

### 11.4. Seven-Segment Display

The MachXO5-NX Development Board features a blue Seven-segment Display of D20, as shown in [Figure 11.3](#), controlled by I/O within Bank 5. Each segment LED is lighted blue when the output is driven LOW. [Table 11.4](#) lists the connections between display LED segments and their associated driver pins.



**Figure 11.3. Seven-Segment Display and its Symbol**

**Table 11.4. Seven-segment Display Connections**

| Net Name | D20 Pin Number | MachXO5-25 Ball Location |
|----------|----------------|--------------------------|
| SEG_A    | 7              | F14                      |
| SEG_B    | 6              | G11                      |
| SEG_C    | 4              | E15                      |
| SEG_D    | 2              | F11                      |
| SEG_E    | 1              | A15                      |
| SEG_F    | 9              | A16                      |
| SEG_G    | 10             | A17                      |
| SEG_DP   | 5              | A18                      |

## 12. Software Requirements

The following software are required to develop designs for the MachXO5™-NX Development Board:

- Radiant 3.11 (or later version)
- Radiant Programmer 3.11 (or later version)

## 13. Storage and Handling

Static electricity can shorten the life span of electronic components. Observe these tips to prevent damage that can occur from electrostatic discharge:

- Use antistatic precautions such as operating on an antistatic mat and wearing an antistatic wristband.
- Store the MachXO5™-NX Development Board in the provided packaging.
- Touch a metal USB housing to equalize voltage potential between you and the board.

## 14. Ordering Information

Table 14.1 Ordering Information

| Description                  | Ordering Part Number | China RoHS Environment-Friendly Use Period (EFUP)                                   |
|------------------------------|----------------------|-------------------------------------------------------------------------------------|
| MachXO5-NX Development Board | LFMXO5-25-EVN        |  |

## Technical Support Assistance

Submit a technical support case through [www.latticesemi.com/techsupport](http://www.latticesemi.com/techsupport).

For frequently asked questions, refer to the Lattice Answer Database at [www.latticesemi.com/Support/AnswerDatabase](http://www.latticesemi.com/Support/AnswerDatabase).



# MachX05-NX Development Board

## 11 - POWER REGULATORS



|                                                                                                                                                                      |                                                |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------|
| Lattice Semiconductor Applications<br>Email: <a href="mailto:techsupport@latticesemi.com">techsupport@latticesemi.com</a><br>Phone (503) 268-8001 -or- (800) LATTICE |                                                |
| <b>Title Page</b>                                                                                                                                                    |                                                |
| Size<br>A                                                                                                                                                            | Project<br><b>MachXO5-NX Development Board</b> |
| Date: Thursday, January 13, 2022                                                                                                                                     |                                                |
| Sheet 1 of 11                                                                                                                                                        |                                                |
| 2                                                                                                                                                                    |                                                |
| Schematic Rev. 1.0<br>Board Rev. A                                                                                                                                   |                                                |

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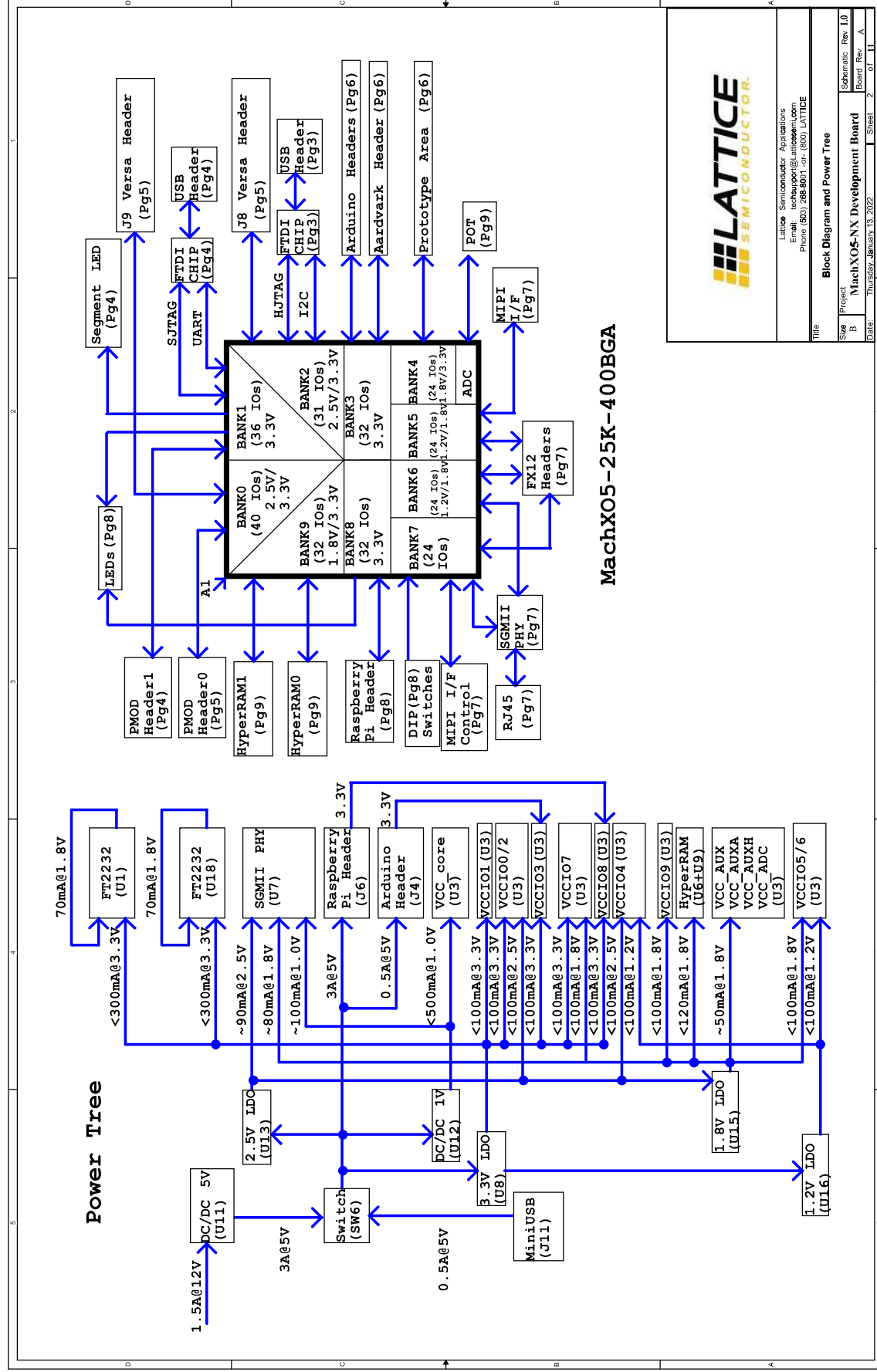


Figure A. 2. Block Diagram and Power Tree

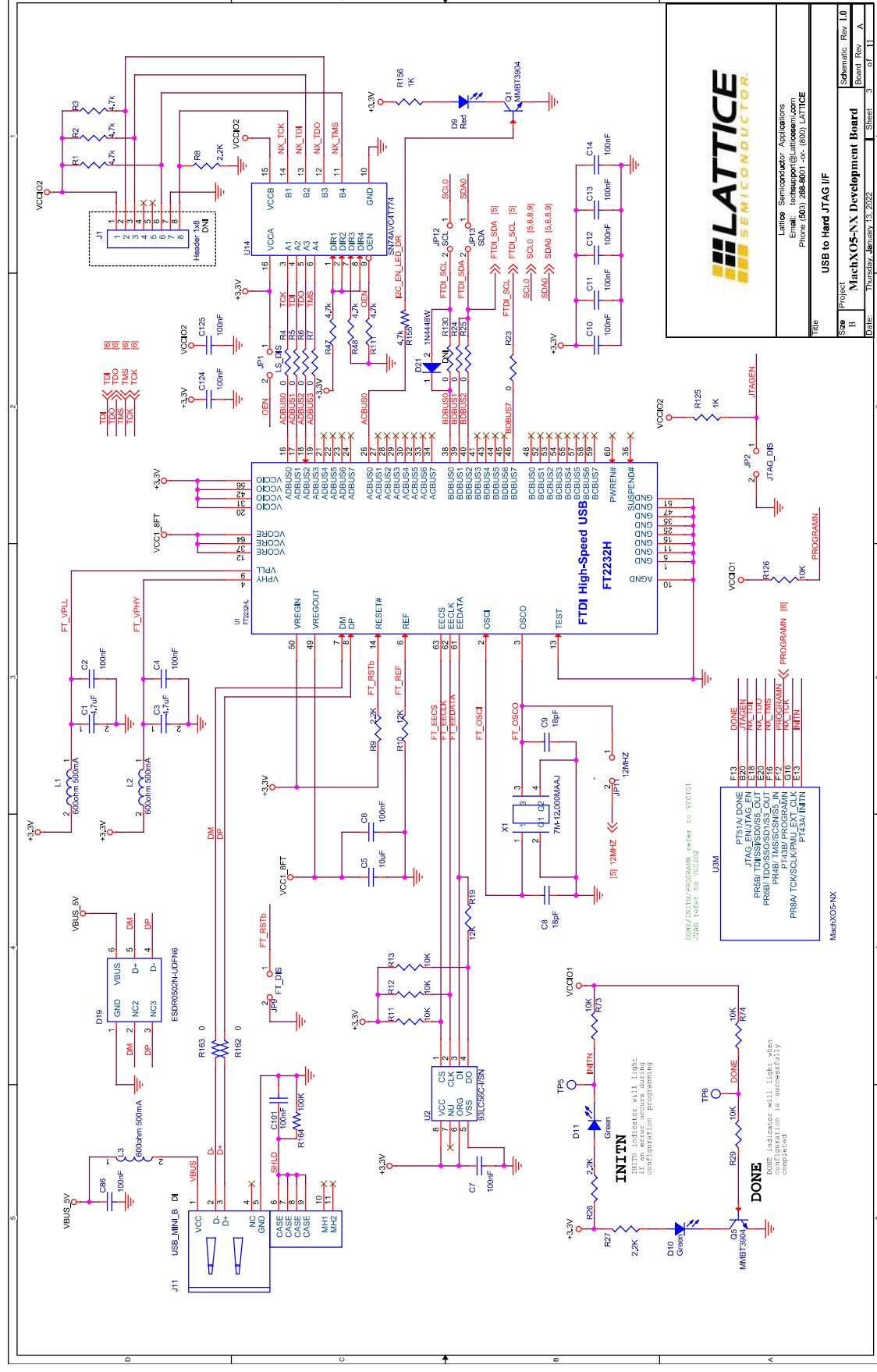


Figure A. 3. USB to Hard JTAG I/F

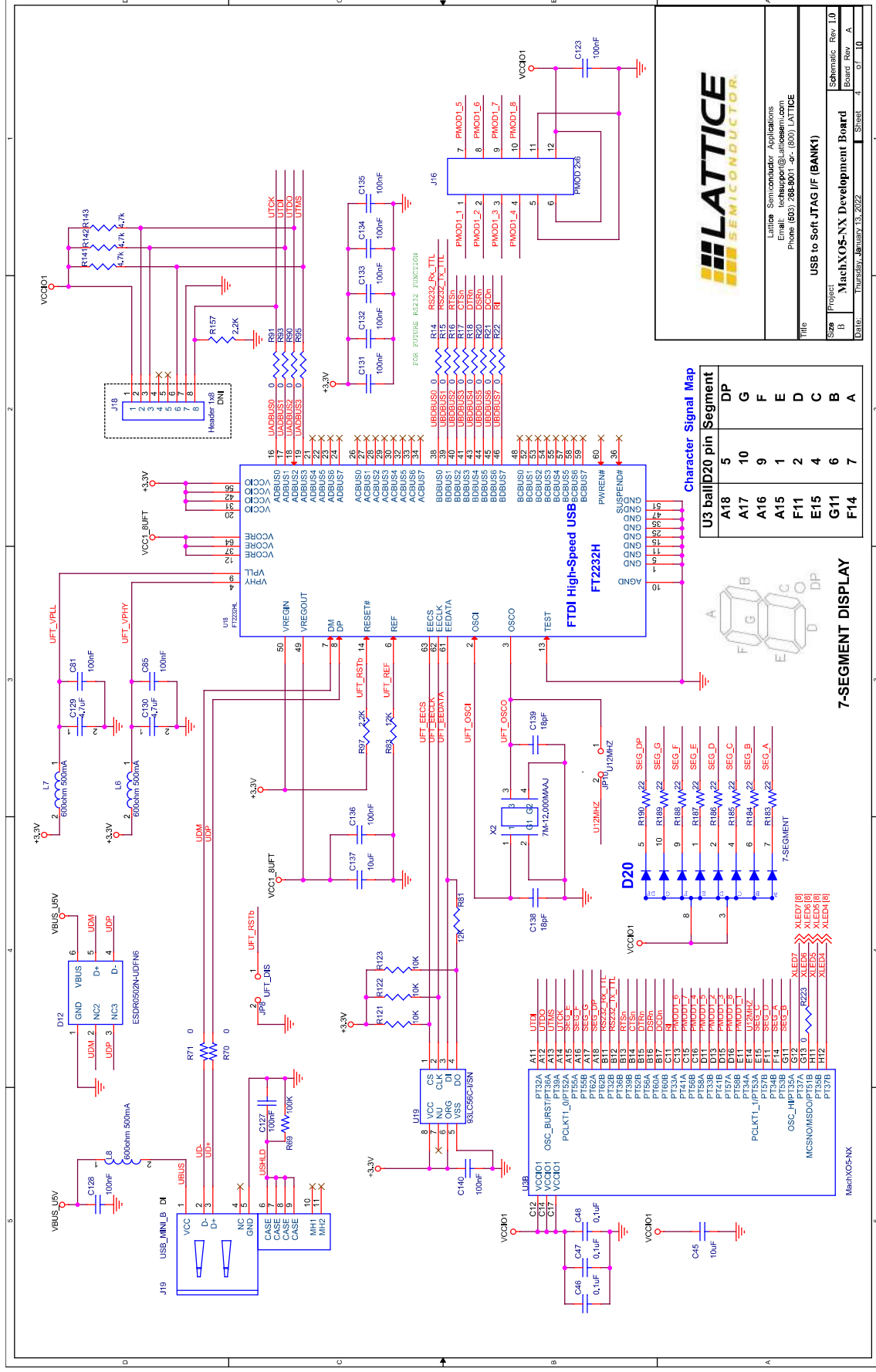
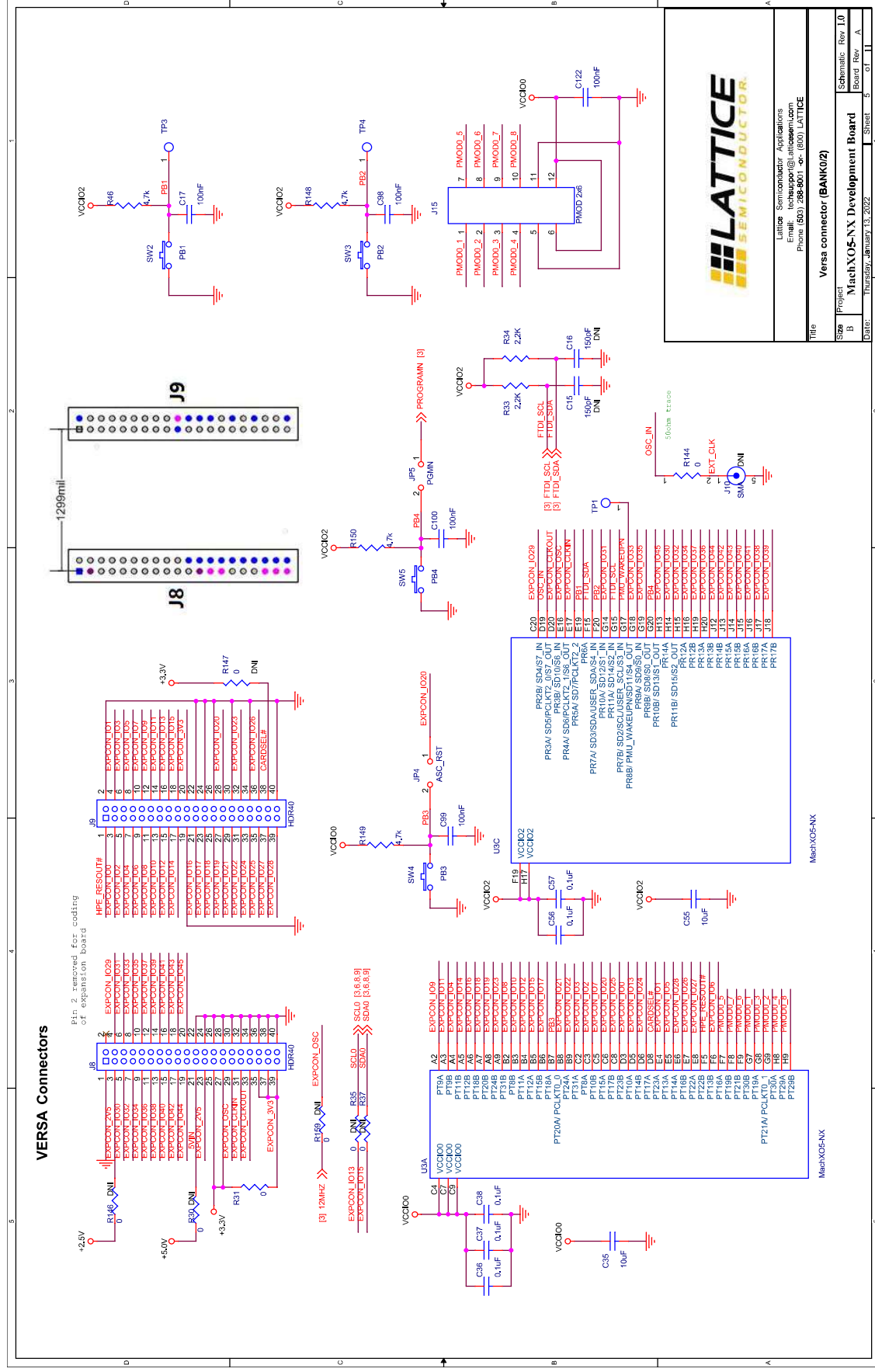


Figure A. 4. USB to Soft JTAG I/F (BANK1)



### Figure A.5. Versa Connector (BANK0/2)

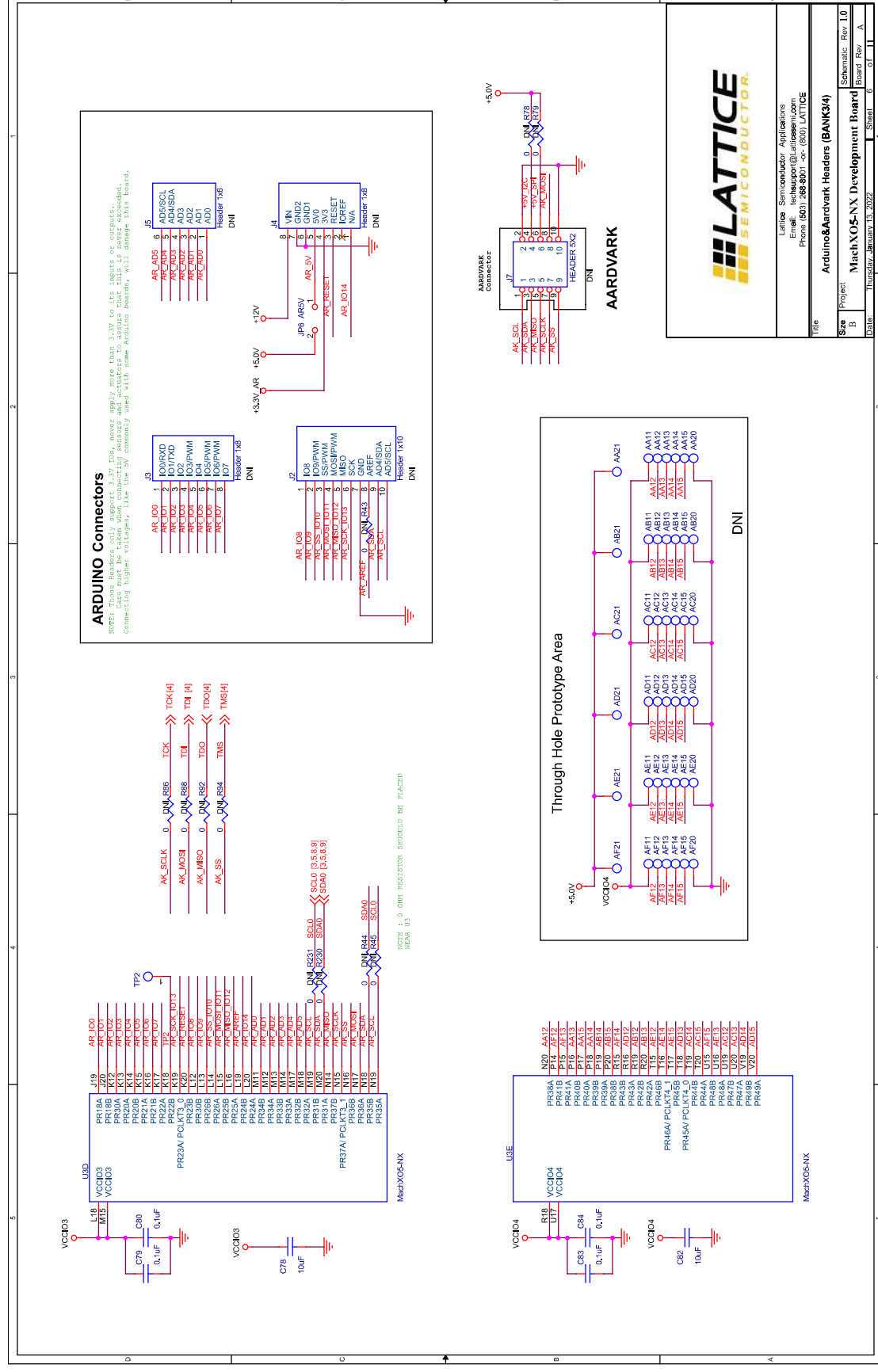
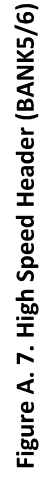


Figure A. 6. Arduino&Aardvark Header (BANK3/4)





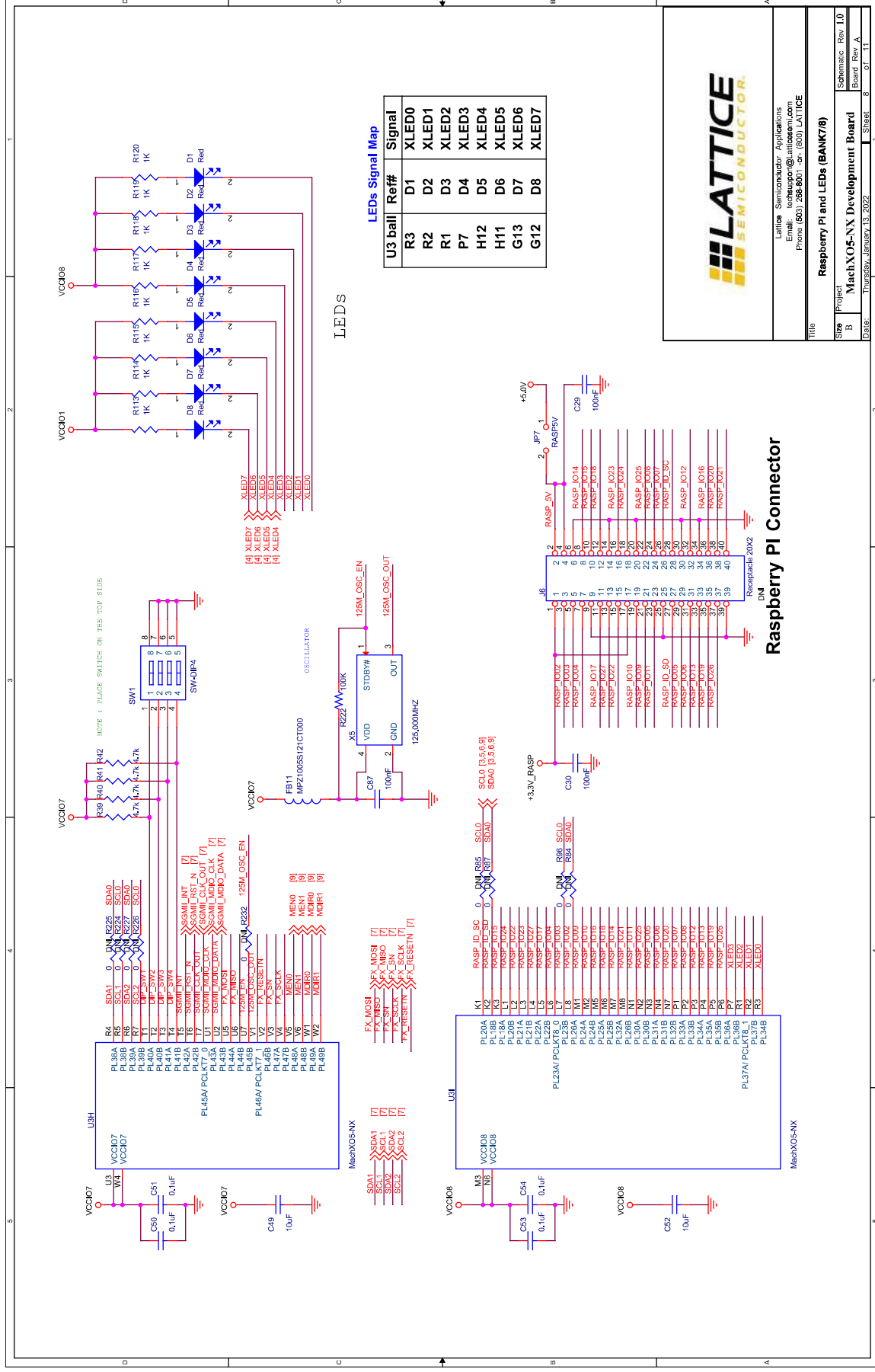


Figure A. 8. Raspberry Pi and LEDs (BANK7/8)



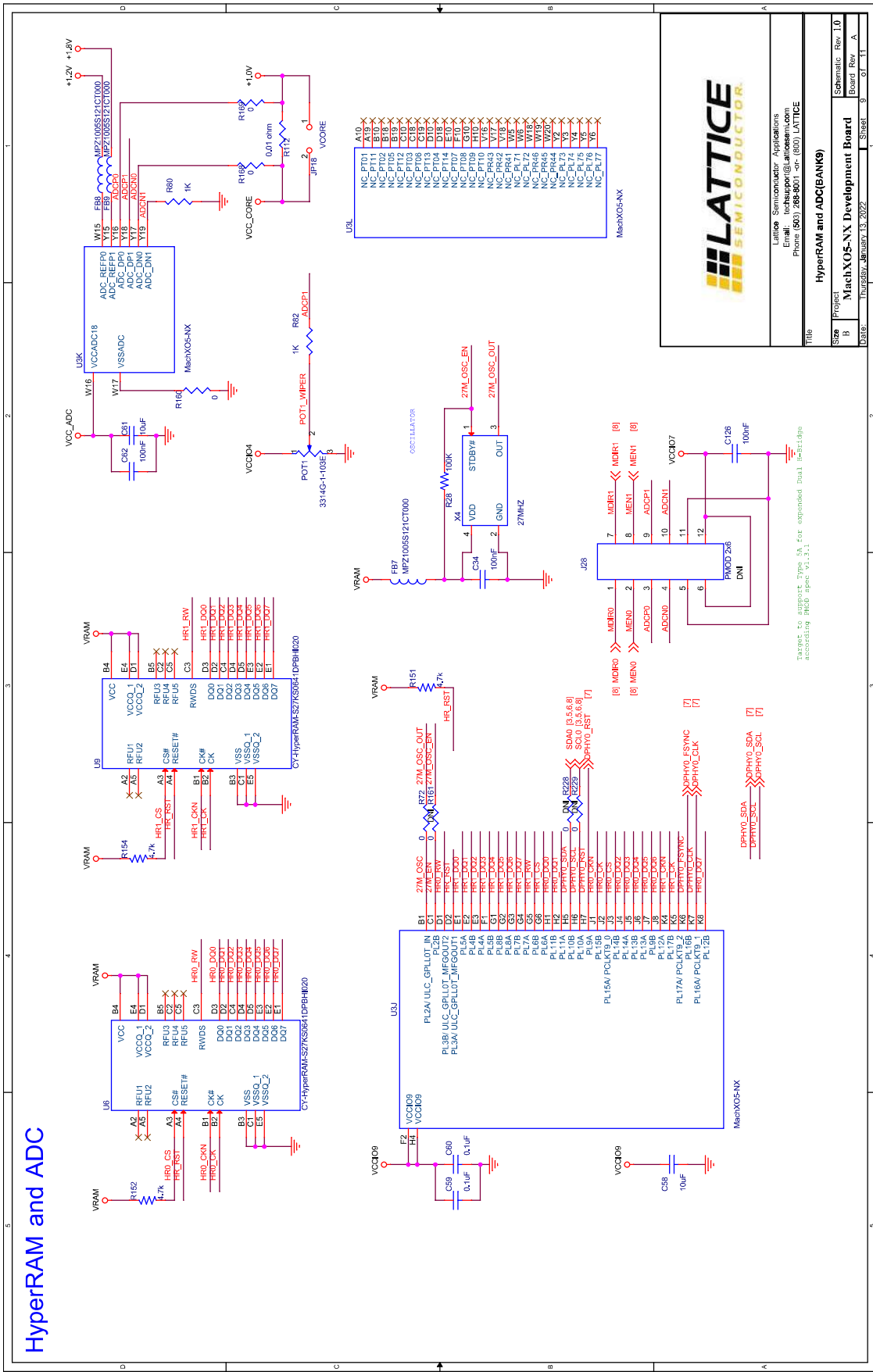


Figure A. 9. HyperRam and ADC (BANK9)

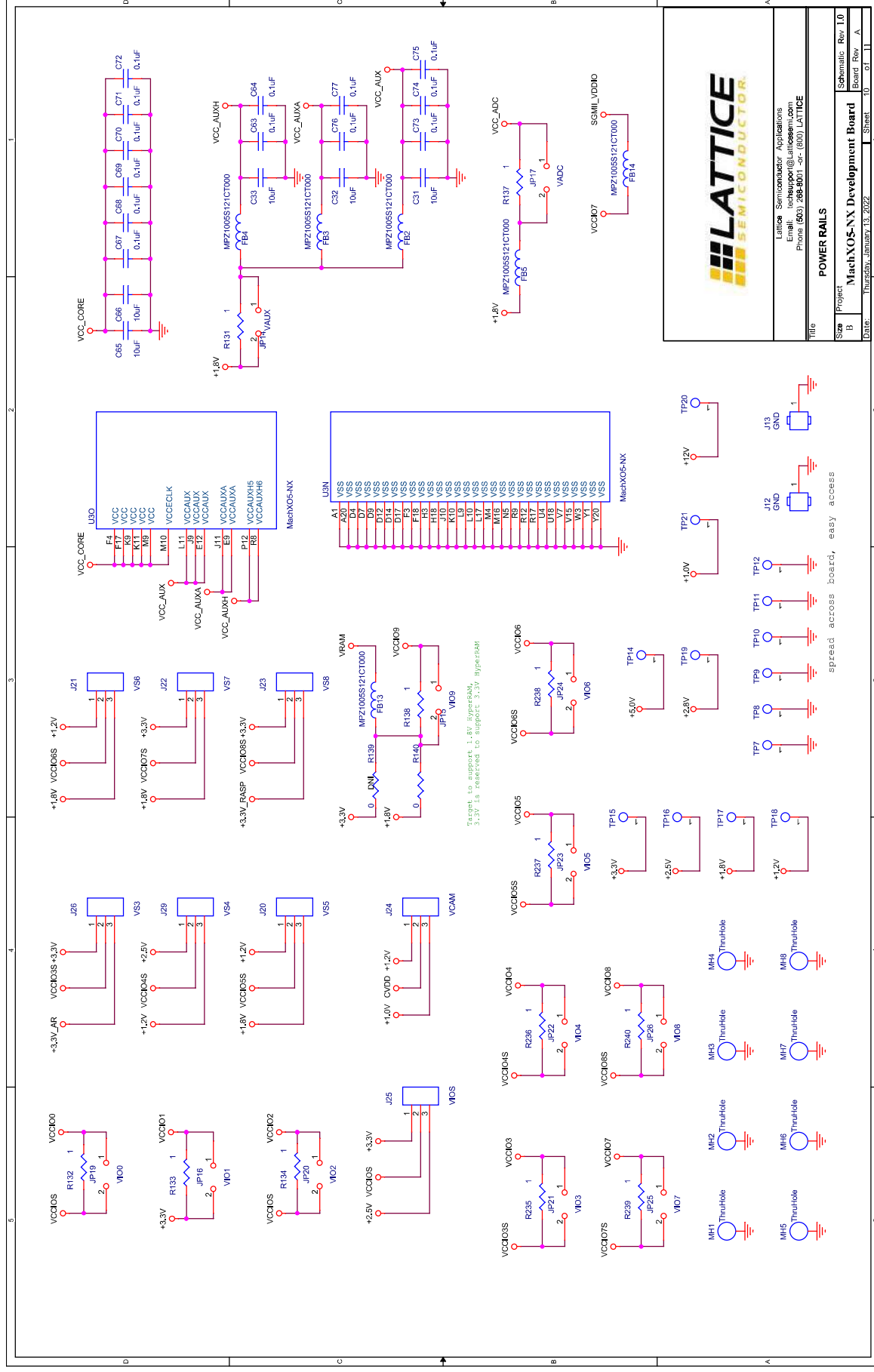
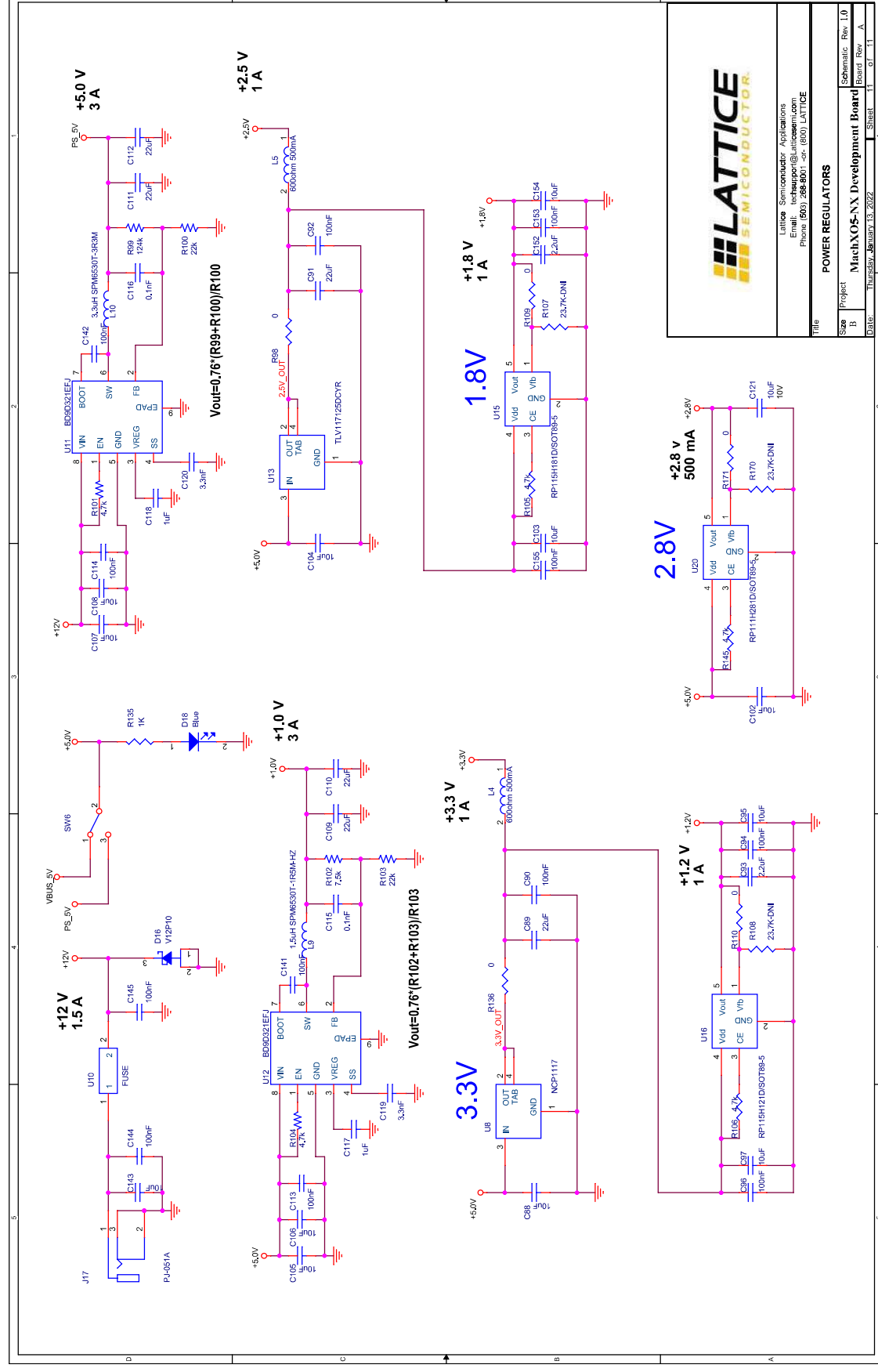


Figure A. 10. Power Rails



**Figure A. 11. Power Regulators**

## Appendix B. MachXO5-NX Development Board Bill of Materials

| Item | Reference                                                                                                                                                                                                                                                                                                                             | Qty | Part         | PCB Footprint | Part Number            | Manufacturer | Description                       | Assembly |
|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|--------------|---------------|------------------------|--------------|-----------------------------------|----------|
| 1    | AF11,AE11,AD11,<br>AC11,AB11,AA11,<br>AF12,AE12,AD12,<br>AC12,AB12,AA12,<br>AF13,AE13,AD13,<br>AC13,AB13,AA13,<br>AF14,AE14,AD14,<br>AC14,AB14,AA14,<br>AF15,AE15,AD15,<br>AC15,AB15,AA15,<br>AF20,AE20,AD20,<br>AC20,AB20,AA20,<br>AF21,AE21,AD21,<br>AC21,AB21,AA21                                                                 | 42  | T POINT<br>R | TP            | —                      | —            | —                                 | DNI      |
| 2    | C1,C3,C129,C130                                                                                                                                                                                                                                                                                                                       | 4   | 4.7uF        | C0603         | 885012106005           | Wurth        | CAP CER<br>4.7UF 6.3V<br>X5R 0603 | —        |
| 3    | C2,C4,C6,C7,C10,C11,<br>C12,C13,C14,C17,C20,<br>C21,C22,C23,C24,C25,<br>C26,C27,C29,C30,C34,<br>C62,C81,C85,C86,C87,<br>C90,C92,C94,C96,C98,<br>C99,C100,C101,C113,<br>C114,C122,C123,C124,<br>C125,C126,C127,C128,<br>C131,C132,C133,C134,<br>C135,C136,C140,C141,<br>C142,C144,C145,C146,<br>C147,C148,C149,C150,<br>C151,C153,C155 | 62  | 100nF        | C0402         | GRM155R71H1<br>04KE14D | Murata       | CAP CER<br>0.1UF 50V<br>X7R 0402  | —        |
| 4    | C5,C31,C32,C33,C35,<br>C39,C42,C45,C49,C52,<br>C55,C58,C61,C65,C66,<br>C78,C82,C95,C97,C103<br>,C121,C137,C154,C156<br>,C157,C166,C169,C172<br>,C174,C178,C180                                                                                                                                                                        | 31  | 10uF         | C0603         | 0603ZD106KAT<br>2A     | KYOCERA AVX  | CAP CER 10UF<br>10V X5R 0603      | —        |
| 5    | C8,C9,C18,C19,C28,<br>C138,C139                                                                                                                                                                                                                                                                                                       | 7   | 18pF         | C0402         | C0402C180K3G<br>ACTU   | KEMET        | CAP CER 18PF<br>25V NP0 0402      | —        |
| 6    | C15,C16                                                                                                                                                                                                                                                                                                                               | 2   | 150pF        | C0402         | —                      | —            | —                                 | DNI      |
| 7    | C36,C37,C38,C40,C41,<br>C43,C44,C46,C47,C48,<br>C50,C51,C53,C54,C56,<br>C57,C59,C60,C63,C64,<br>C67,C68,C69,C70,C71,<br>C72,C73,C74,C75,C76,<br>C77,C79,C80,C83,C84,<br>C162,C163,C164,C165,<br>C170,C171,C176,C177,<br>C182,C183,C184                                                                                                | 46  | 0.1uF        | C0201         | CC0201KRX5R8<br>BB104  | YAGEO        | CAP CER<br>0.1UF 25V<br>X5R 0201  | —        |

| Item | Reference                                                        | Qty | Part               | PCB Footprint            | Part Number         | Manufacturer | Description                          | Assembly |
|------|------------------------------------------------------------------|-----|--------------------|--------------------------|---------------------|--------------|--------------------------------------|----------|
| 8    | C88,C102,C104,C105,C106,C107,C108,C143                           | 8   | 10uF               | C1206                    | CL31B106KBH NNE     | Samsung      | CAP CER 10UF 50V X7R 1206            | —        |
| 9    | C89,C91,C109,C110,C111,C112                                      | 6   | 22uF               | C0603                    | CL10A226MO7 JZNC    | Samsung      | CAP CER 22UF 16V X5R 0603            | —        |
| 10   | C93,C152                                                         | 2   | 2.2uF              | RLP-133                  | CL21B225KPFN NNE    | Samsung      | CAP CER 2.2UF 10V X7R 0805           | —        |
| 11   | C115,C116                                                        | 2   | 0.1nF              | C0603                    | CC0603JRNPO9 BN101  | YAGEO        | CAP CER 100PF 50V COG/NPO 0603       | —        |
| 12   | C117,C118,C158,C159,C160,C161,C167,C168,C173,C175,C179,C181,C185 | 13  | 1uF                | C0603                    | CL10A105KO8 NNNC    | Samsung      | CAP CER 1UF 16V X5R 0603             | —        |
| 13   | C119,C120                                                        | 2   | 3.3nF              | C0201                    | GRM033R71A3 32JA01D | Murata       | CAP CER 3300PF 10V X7R 0201          | —        |
| 14   | D1,D2,D3,D4,D5,D6,D7,D8,D9,D13,D14,D15                           | 12  | Red                | led_0603                 | LTST-C190KRKT       | LITE-On INC  | LED RED CLEAR 0603 SMD               | —        |
| 15   | D10,D11                                                          | 2   | Green              | led_0603                 | LTST-C190KGKT       | LITE-On INC  | LED GREEN CLEAR CHIP SMD             | —        |
| 16   | D12,D19                                                          | 2   | ESDR050 2N-UDFN6   | UDFN6_0 40               | ESDR0502NMU TBG     | ON semi      | TVS DIODE 5.5VWM 6UDFN               | —        |
| 17   | D16                                                              | 1   | V12P10             | V12P10                   | V12P10-M3/87A       | Vishay       | DIODE SCHOTTKY 12A 100V SMPC TO-277A | —        |
| 18   | D18                                                              | 1   | Blue               | led_0603                 | LTST-C190TBKT       | LITE-On INC  | LED 468NM BLUE CLEAR 0603 SMD        | —        |
| 19   | D20                                                              | 1   | 7-SEGMENT          | LED10-057-394-XZFMDK0 5A | XZFMDK05A           | SunLED       | DISPLAY 7-SEG 0.2" SGL RED 10SMD     | —        |
| 20   | D21                                                              | 1   | 1N4448 W           | 1N4448W                  | 1N4448WT            | Onsemi       | DIODE GEN PURP 75V 200MA SOD523F     | —        |
| 21   | FB1,FB2,FB3,FB4,FB5,FB6,FB7,FB8,FB9,FB10,FB11,FB12,FB13,FB14     | 14  | MPZ100 5S121CT 000 | MPZ100S 5121CT00 0       | MPZ100S5121 CT000   | TDK          | FERRITE BEAD 120 OHM 0402 1LN        | —        |
| 22   | J1,J18                                                           | 2   | Header 1x8         | hdr_amp_87220_8_1x8_100  | 22284081            | Molex        | CONN HEADER 8POS .100 VERT TIN       | DNI      |

| Item | Reference                       | Qty | Part             | PCB Footprint                  | Part Number        | Manufacturer         | Description                      | Assembly |
|------|---------------------------------|-----|------------------|--------------------------------|--------------------|----------------------|----------------------------------|----------|
| 23   | J2                              | 1   | Header 1x10      | CONF1X10-254P_2612X240X85OH_TH | 10129378-910002BLF | Amphenol             | CONN HEADER VERT 10POS 2.54MM    | DNI      |
| 24   | J3,J4                           | 2   | Header 1x8       | CONF1X8-254P_2104X240X85OH_TH  | 10129378-908002BLF | Amphenol             | CONN HEADER VERT 8POS 2.54MM     | DNI      |
| 25   | J5                              | 1   | Header 1x6       | CONF1X6-254P_1596X240X85OH_TH  | 10129378-906002BLF | Amphenol             | CONN HEADER VERT 6POS 2.54MM     | DNI      |
| 26   | J6                              | 1   | Receptacle 20X2  | HDR254-2X20_soc ket            | PPTC202LFBN-RC     | Sullins              | CONN HEADER FEM 40POS .1" DL TIN | DNI      |
| 27   | J7                              | 1   | HEADER 5X2       | HDR254-2X5_SHR OUDED           | 30310-6002HB       | 3M                   | CONN HEADER 10POS DL STR GOLD    | DNI      |
| 28   | J8,J9                           | 2   | HDR40            | HDR-20x2                       | PRPC020DFBN-RC     | Sullins              | CONN HEADER VERT 40POS 2.54MM    | —        |
| 29   | J10                             | 1   | SMA              | bnc5-100-280t                  | 5-1814832-1        | TE Connectivity      | CONN SMA JACK STR 50 OHM PCB     | DNI      |
| 30   | J11,J19                         | 1   | USB_MINI_B       | usb2-0-rec-240-0001-9          | UX60-MB-5ST        | Hirose               | CONN RECEPT MINI USB2.0 5POS     | —        |
| 31   | J12,J13                         | 2   | GND              | TUR_TH                         | 1573-2             | Keystone Electronics | TERMINAL TURRET DBL .082"L       | —        |
| 32   | J14                             | 1   | 7498111001-RJ45  | RJ45-7498111001                | 7498111001         | Würth                | CONN JACK 1PORT 1000 BASE-T SMD  | —        |
| 33   | J15,J16                         | 2   | PMOD 2x6         | PPPC062LJBN-RC                 | PPPC062LJBN-RC     | Sullins              | CONN HDR 12POS 0.1 GOLD PCB R/A  | —        |
| 34   | J17                             | 1   | PJ-051A          | PJ_051A                        | PJ-051A            | CUI Device           | CONN PWR JACK 2X5.5MM SOLDER     | —        |
| 35   | J20,J21,J22,J23,J24,J25,J26,J29 | 8   | HDR1X3           | HDR1X3                         | PRPC003SAAN-RC     | Sullins              | CONN HEADER VERT 3POS 2.54MM     | —        |
| 36   | J27                             | 1   | 245804030000829+ | 245804030000829                | 245804030000829+   | Kyocera AVX          | CONN RCPT 30POS SMD              | —        |

| Item | Reference                                                                                                                                              | Qty | Part              | PCB Footprint      | Part Number          | Manufacturer | Description                               | Assembly |
|------|--------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-------------------|--------------------|----------------------|--------------|-------------------------------------------|----------|
| 37   | J28                                                                                                                                                    | 1   | PMOD<br>2x6       | PPPC062L<br>JBN-RC | PPPC062LJBN-<br>RC   | Sullins      | CONN HDR<br>12POS 0.1<br>GOLD PCB<br>R/A  | DNI      |
| 38   | JP1,JP2,JP3,JP4,JP5,<br>JP6,JP7,JP8,JP9,JP10,<br>JP11,JP12,JP13,JP14,<br>JP15,JP16,JP17,JP18,<br>JP19,JP20,JP21,JP22,<br>JP23,JP24,JP25,JP26           | 26  | JUMPER            | Header_1<br>x2     | 861400021YO2<br>LF   | Amphenol     | CONN<br>HEADER VERT<br>2POS<br>2.54MM     | —        |
| 39   | L1,L2,L3,L4,L5,L6,L7,L8                                                                                                                                | 8   | 600ohm<br>500mA   | fb0603             | BLM18AG601S<br>N1D   | Murata       | FERRITE CHIP<br>600 OHM<br>500MA 0603     | —        |
| 40   | L9                                                                                                                                                     | 1   | SPM653<br>OT-1R5M | SPM6530<br>T-2R2M  | SPM6530T-<br>1R5M100 | TDK          | FIXED IND<br>1.5UH 11A<br>10.67MOHM<br>SM | —        |
| 41   | L10                                                                                                                                                    | 1   | SPM653<br>OT-3R3M | SPM6530<br>T-2R2M  | SPM6530T-<br>3R3M-HZ | TDK          | FIXED IND<br>3.3UH 6.8A<br>29.7MOHM<br>SM | —        |
| 42   | POT1                                                                                                                                                   | 1   | 3314G-1-<br>103E  | sot23-<br>3314G-1  | 3314G-1-103E         | Bourns Inc.  | TRIMMER 10K<br>OHM 0.25W<br>SMD           | —        |
| 43   | Q1,Q2,Q3,Q4,Q5                                                                                                                                         | 5   | 2N3904            | MMBT390<br>4       | MMBT3904-7-<br>F     | Diodes       | TRANS NPN<br>40V 0.2A SOT-<br>23          | —        |
| 44   | R1,R2,R3,R39,R40,<br>R41,R42,R46,R47,R48,<br>R101,R104,R105,R106,<br>R111,R141,R142,R143,<br>R145,R148,R149,R150,<br>R151,R152,R154,R155,<br>R233,R234 | 28  | 4.7k              | R0402              | RT0402FRE074<br>K7L  | yageo        | RES SMD 4.7K<br>OHM 1%<br>1/16W 0402      | —        |
| 45   | R4,R5,R6,R7,R14,R15,<br>R16,R17,R18,R20,R21,<br>R22,R23,R24,R25,R31,<br>R90,R91,R93,R95,R98,<br>R136,R140,R160,R168,<br>R169                           | 26  | 0                 | R0603              | RC0603FR-<br>070RL   | yageo        | RES 0.0 OHM<br>1/10W JUMP<br>0603 SMD     | —        |
| 46   | R8,R9,R26,R27,R33,<br>R34,R76,R77,R97,<br>R157,R219,R220,R221                                                                                          | 13  | 2.2k              | R0402              | RC0402FR-<br>072K2L  | yageo        | RES 2.2K<br>OHM 1%<br>1/16W 0402          | —        |
| 47   | R10,R19,R81,R83                                                                                                                                        | 4   | 12K               | R0603              | RC0603FR-<br>0712KL  | yageo        | RES 12K OHM<br>1/10W 1%<br>0603 SMD       | —        |
| 48   | R11,R12,R13,R29,R73,<br>R74,R121,R122,R123,<br>R124,R126,R129                                                                                          | 12  | 10K               | R0402              | RT0402FRE071<br>OKL  | yageo        | RES SMD 10K<br>OHM 1%<br>1/16W 0402       | —        |
| 49   | R28,R69,R164,R222                                                                                                                                      | 4   | 100K              | R0402              | AC0402FR-<br>7W100KL | yageo        | RES 100<br>KOHM 1%<br>1/8W 0402           | —        |

| Item | Reference                                                                                                                                                                      | Qty | Part          | PCB Footprint | Part Number          | Manufacturer | Description                               | Assembly |
|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|---------------|---------------|----------------------|--------------|-------------------------------------------|----------|
| 50   | R30,R35,R37,R43,R44,<br>R45,R67,R68,R78,R79,<br>R84,R85,R86,R87,R88,<br>R92,R94,R96,R130,<br>R139,R146,R147,R159,<br>R161,R224,R225,R226,<br>R227,R228,R229,R230,<br>R231,R232 | 33  | 0             | R0603         | —                    | —            | —                                         | DNI      |
| 51   | R32                                                                                                                                                                            | 1   | 11K           | R0603         | RT0603DRD07<br>11KL  | yageo        | RES SMD 11K<br>OHM 0.5%<br>1/10W 0603     | —        |
| 52   | R36,R89,R203,R205                                                                                                                                                              | 4   | 100           | R0603         | RC0603FR-<br>07100RL | yageo        | RES SMD 100<br>OHM 1%<br>1/10W 0603       | —        |
| 53   | R38                                                                                                                                                                            | 1   | 2.2k          | R0402         | —                    | —            | —                                         | DNI      |
| 54   | R49,R50,R51,R52,R53,<br>R54,R55,R56,R57,R58,<br>R59,R60,R61,R62,R63,<br>R64                                                                                                    | 16  | 100           | R0201         | —                    | —            | —                                         | DNI      |
| 55   | R65,R66                                                                                                                                                                        | 2   | 2.49K         | R0603         | RT0603DRE072<br>K49L | yageo        | RES SMD<br>2.49KOHM<br>0.5% 1/10W<br>0603 | —        |
| 56   | R70,R71,R72,R109,R11<br>0,R144,R162,R163,R17<br>1,R223                                                                                                                         | 10  | 0             | R0402         | AC0402JR-<br>070RL   | yageo        | RES SMD 0<br>OHM JUMPER<br>1/16W 0402     | —        |
| 57   | R75,R183,R184,R185,<br>R186,R187,R188,R189,<br>R190                                                                                                                            | 9   | 22            | R0603         | RC0603FR-<br>0722RL  | yageo        | RES SMD 22<br>OHM 1%<br>1/10W 0603        | —        |
| 58   | R80,R82,R113,R114,<br>R115,R116,R117,R118,<br>R119,R120,R125,R135,<br>R156,R165,R166,R167                                                                                      | 16  | 1k            | R0402         | AF0402FR-<br>071KL   | yageo        | RES SMD 1K<br>OHM 1%<br>1/16W 0402        | —        |
| 59   | R99                                                                                                                                                                            | 1   | 124K          | R0603         | RT0603DRD07<br>124KL | yageo        | RES SMD<br>124K OHM<br>0.5% 1/10W<br>0603 | —        |
| 60   | R100,R103                                                                                                                                                                      | 2   | 22K           | R0402         | AC0402FR-<br>0722KL  | yageo        | RES SMD 22K<br>OHM 1%<br>1/16W 0402       | —        |
| 61   | R102                                                                                                                                                                           | 1   | 7.5k          | R0603         | RT0603DRD07<br>7K5L  | yageo        | RES SMD 7.5K<br>OHM 0.5%<br>1/10W 0603    | —        |
| 62   | R107,R108,R170                                                                                                                                                                 | 3   | 23.7K-<br>DNI | R0603         | —                    | —            | —                                         | DNI      |
| 63   | R112                                                                                                                                                                           | 1   | 10mOhm<br>s   | R0603         | WSL0603R010<br>0FEA  | Vishay       | RES 0.01<br>OHM 1%<br>1/10W 0603          | —        |
| 64   | R131,R132,R133,R134,<br>R137,R138,R235,R236,<br>R237,R238,R239,R240                                                                                                            | 12  | 1             | R0603         | RT0603DRE071<br>RL   | yageo        | RES 1 OHM<br>0.5% 1/10W<br>0603           | —        |
| 65   | R158                                                                                                                                                                           | 1   | 1M Ohm        | R0402         | AC0402FR-<br>071ML   | yageo        | RES SMD 1M<br>OHM 1%<br>1/16W 0402        | —        |



| Item | Reference                                                                                  | Qty | Part                          | PCB Footprint             | Part Number        | Manufacturer | Description                      | Assembly |
|------|--------------------------------------------------------------------------------------------|-----|-------------------------------|---------------------------|--------------------|--------------|----------------------------------|----------|
| 66   | SW1                                                                                        | 1   | SW-DIP4                       | sw_sp_st_cts_195-4mst     | 195-4MST           | CTS          | SWITCH PIANO DIP SPST 50MA 24V   | —        |
| 67   | SW2,SW3,SW4,SW5                                                                            | 4   | SYS_RST                       | sw_sp_st_eswitch_tl1015   | TL1015AF160QG      | E-Switch     | SWITCH TACTILE SPST-NO 0.05A 12V | —        |
| 68   | SW6                                                                                        | 1   | 1101M2 S2CQE2                 | SWITCH_3 P-6A             | 1101M2S3CQE2       | C&K          | Slide Switches                   | —        |
| 69   | TP1,TP2,TP3,TP4,TP5,TP6,TP7,TP8,TP9,TP10,TP11,TP12,TP14,TP15,TP16,TP17,TP18,TP19,TP20,TP21 | 20  | T POINT R                     | TP                        | —                  | —            | —                                | DNI      |
| 70   | U1,U18                                                                                     | 2   | FT2232HL                      | tqfp64_0p5_12p2x12p2_h1p6 | FT2232HL-TRAY      | FTDI         | IC USB HS DUAL UART/FIFO 64-LQFP | —        |
| 71   | U2,U19                                                                                     | 2   | 93LC56C-I/SN                  | so8_50_244                | 93LC56C-I/SN       | Microchip    | IC EEPROM 2KBIT 3MHZ 8SOIC       | —        |
| 72   | U3                                                                                         | 1   | JEDI_D6_Final                 | BGA400-080-17X17-SOCKET   | LFMXO5-25-9BBG400C | Lattice      | Target Device                    | —        |
| 73   | U4,U5                                                                                      | 2   | Hirose - FX12 - 40 Pos        | Hirose-FX12               | FX12B-40P-0.4SV    | Hirose       | CONN PLUG 40POS 0.4MM SMD SHIELD | —        |
| 74   | U6,U9                                                                                      | 2   | CY-HyperRAM-S27KS0641DPBHIO20 | 24FBGA_S27KS              | S27KS0641DPBHIO20  | Cypress      | IC PSRAM 64MBIT PARALLEL 24FBGA  | —        |
| 75   | U7                                                                                         | 1   | DP83867ERGZT                  | 48VQFN_DP83867            | DP83867ERGZT       | TI           | IC ETHERNET PHY 48VQFN           | *        |
| 76   | U8                                                                                         | 1   | NCP1117                       | sot223_4p                 | NCP1117ST33T3G     | ON semi      | IC REG LDO 3.3V 1A SOT223        | —        |
| 77   | U10                                                                                        | 1   | FUSE                          | 0154004DRT                | 01571.25DR         | Littelfuse   | Fuse 260C 1.25A VFA NANO Clip    | —        |
| 78   | U11,U12                                                                                    | 2   | BD9D321EFJ                    | HTSOP_8_BD9D321           | BD9D321EFJ-E2      | Rohm         | IC REG BUCK ADJ 3A 8HTSOP-J      | —        |
| 79   | U13                                                                                        | 1   | TLV117125DCYR                 | sot223_4p                 | TLV117125DCYR      | TI           | IC REG LINEAR 2.5V 1A SOT223-4   | —        |
| 80   | U14                                                                                        | 1   | SN74AVC4T774                  | tssop16-0p65mm            | SN74AVC4T774PWR    | TI           | IC TRNSLTR BIDIRECTIONAL 16TSSOP | —        |

| Item | Reference | Qty | Part                | PCB Footprint   | Part Number          | Manufacturer | Description                      | Assembly |
|------|-----------|-----|---------------------|-----------------|----------------------|--------------|----------------------------------|----------|
| 81   | U15       | 1   | RP115H181D/SOT89-5  | SOT89-5         | RP115H181D-T1-FE     | RICOH        | IC REG LINEAR 1.8V 1A SOT89-5    | —        |
| 82   | U16       | 1   | RP115H121D/SOT89-5  | SOT89-5         | RP115H121D-T1-FE     | RICOH        | IC REG LINEAR 1.2V 1A SOT89-5    | —        |
| 83   | U20       | 1   | RP111H281D/SOT89-5  | SOT89-5         | RP111H281D-T1-FE     | RICOH        | IC REG LINEAR 2.8V 1A SOT89-5    | —        |
| 84   | X1,X2     | 2   | 7M-12.000MAAJ       | xtal_4p_7m      | 7M-12.000MAAJ-T      | TXC          | CRYSTAL 12MHZ 18PF SMD           | —        |
| 85   | X3        | 1   | ABM3-25             | XTAL_AB M3      | ABM7-25.000MHZ-D2Y-T | Abracon LLC  | CRYSTAL 25.0000MHZ 18PF SMD      | —        |
| 86   | X4        | 1   | DSC1001DE2-027.0000 | x4-2520         | DSC1001DE2-027.0000  | Abracon LLC  | MEMS OSC XO 27.0000MHZ CMOS SMD  | —        |
| 87   | X5        | 1   | 125.000MHZ          | crystal_4p_7050 | DSC1001AE5-125.0000  | Microchip    | MEMS OSC XO 125.0000MHZ CMOS SMD | —        |
| 88   | —         | 1   | —                   | —               | —                    | Pctron       | —                                | —        |

**\*Note:** The MachXO5™-NX Development Board, OPN of which is LFMXO5-25-EVN, is delivered without the Ethernet PHY due to long lead time.

## Appendix C. User Defined Preference File Listing

```
// These names follow the MachXO5™-NX Development Board schematic but,  
// they may be defined by the user. Thus, they can be copied into the  
// preference file and edited to match a different naming convention if  
// needed or used to fill in the Spreadsheet view.
```

```
// MachXO5-25 LED Connections  
// Note: The following order matches the LED locations on the board  
// from top D1 to bottom D8
```

```
ldc_set_location -site {R3} [get_ports {LED[0]}]  
ldc_set_location -site {R2} [get_ports {LED[1]}]  
ldc_set_location -site {R1} [get_ports {LED[2]}]  
ldc_set_location -site {P7} [get_ports {LED[3]}]  
ldc_set_location -site {H12} [get_ports {LED[4]}]  
ldc_set_location -site {H11} [get_ports {LED[5]}]  
ldc_set_location -site {G13} [get_ports {LED[6]}]  
ldc_set_location -site {G12} [get_ports {LED[7]}]
```

```
//DIP Switch Connections
```

```
ldc_set_location -site {T1} [get_ports {DIPSW[0]}]  
ldc_set_location -site {T2} [get_ports {DIPSW[1]}]  
ldc_set_location -site {T3} [get_ports {DIPSW[2]}]  
ldc_set_location -site {T4} [get_ports {DIPSW[3]}]
```

```
//Push Button Connections
```

```
ldc_set_location -site {E19} [get_ports PB1]  
ldc_set_location -site {F20} [get_ports PB2]  
ldc_set_location -site {B7} [get_ports PB3]  
ldc_set_location -site {G20} [get_ports PB4]
```

```
//Clock inputs
```

```
ldc_set_location -site {E14} [get_ports CLK_12MHz]  
ldc_set_location -site {T7} [get_ports CLK_25MHz]  
ldc_set_location -site {B1} [get_ports CLK_27MHz]  
ldc_set_location -site {V1} [get_ports CLK_125MHz]  
ldc_set_location -site {D19} [get_ports CLK_EXT]
```

```
//SEG LED Connections
```

```
ldc_set_location -site {A18} [get_ports SEG_LED_DP]  
ldc_set_location -site {A17} [get_ports SEG_LED_G]  
ldc_set_location -site {A16} [get_ports SEG_LED_F]  
ldc_set_location -site {A15} [get_ports SEG_LED_E]  
ldc_set_location -site {F11} [get_ports SEG_LED_D]  
ldc_set_location -site {E15} [get_ports SEG_LED_C]  
ldc_set_location -site {G11} [get_ports SEG_LED_B]  
ldc_set_location -site {F14} [get_ports SEG_LED_A]
```

```
//HyperRAM
```

```
ldc_set_location -site {D2} [get_ports ram0_1_rst]  
ldc_set_location -site {J2} [get_ports ram0_ck_p]  
ldc_set_location -site {J1} [get_ports ram0_ck_n]  
ldc_set_location -site {J3} [get_ports ram0_cs]  
ldc_set_location -site {H1} [get_ports ram0_dq0]  
ldc_set_location -site {H2} [get_ports ram0_dq1]  
ldc_set_location -site {J4} [get_ports ram0_dq2]  
ldc_set_location -site {J5} [get_ports ram0_dq3]
```

```
ldc_set_location -site {J6} [get_ports ram0_dq4]
ldc_set_location -site {J7} [get_ports ram0_dq5]
ldc_set_location -site {J8} [get_ports ram0_dq6]
ldc_set_location -site {K8} [get_ports ram0_dq7]
ldc_set_location -site {D1} [get_ports ram0_rw]
ldc_set_location -site {K5} [get_ports ram1_ck_p]
ldc_set_location -site {K4} [get_ports ram1_ck_n]
ldc_set_location -site {G6} [get_ports ram1_cs]
ldc_set_location -site {E1} [get_ports ram1_dq0]
ldc_set_location -site {E2} [get_ports ram1_dq1]
ldc_set_location -site {E3} [get_ports ram1_dq2]
ldc_set_location -site {F1} [get_ports ram1_dq3]
ldc_set_location -site {G1} [get_ports ram1_dq4]
ldc_set_location -site {G2} [get_ports ram1_dq5]
ldc_set_location -site {G3} [get_ports ram1_dq6]
ldc_set_location -site {G4} [get_ports ram1_dq7]
ldc_set_location -site {G5} [get_ports ram1_rw]

//PMOD0 Connections
ldc_set_location -site {G7} [get_ports PMOD0_1]
ldc_set_location -site {G9} [get_ports PMOD0_2]
ldc_set_location -site {G8} [get_ports PMOD0_3]
ldc_set_location -site {H8} [get_ports PMOD0_4]
ldc_set_location -site {F7} [get_ports PMOD0_5]
ldc_set_location -site {F9} [get_ports PMOD0_6]
ldc_set_location -site {F8} [get_ports PMOD0_7]
ldc_set_location -site {H9} [get_ports PMOD0_8]

//PMOD1 Connections
ldc_set_location -site {E11} [get_ports PMOD1_1]
ldc_set_location -site {D13} [get_ports PMOD1_2]
ldc_set_location -site {D15} [get_ports PMOD1_3]
ldc_set_location -site {C16} [get_ports PMOD1_4]
ldc_set_location -site {D11} [get_ports PMOD1_5]
ldc_set_location -site {C13} [get_ports PMOD1_6]
ldc_set_location -site {C15} [get_ports PMOD1_7]
ldc_set_location -site {D16} [get_ports PMOD1_8]

//USER JTAG Connections
ldc_set_location -site {A11} [get_ports UTDI]
ldc_set_location -site {A12} [get_ports UTDO]
ldc_set_location -site {A13} [get_ports UTMS]
ldc_set_location -site {A14} [get_ports UTCK]

//USER RS232 Connections
ldc_set_location -site {B11} [get_ports RS232_Rx_TTL]
ldc_set_location -site {B12} [get_ports RS232_Tx_TTL]
ldc_set_location -site {B13} [get_ports RTSn]
ldc_set_location -site {B14} [get_ports CTSn]
ldc_set_location -site {B15} [get_ports DTRn]
ldc_set_location -site {B16} [get_ports DSRn]
ldc_set_location -site {B17} [get_ports DCDn]
ldc_set_location -site {C11} [get_ports RI]

//RASPBERRY PI Connections
ldc_set_location -site {L8} [get_ports RASP_IO02]
ldc_set_location -site {L7} [get_ports RASP_IO03]
ldc_set_location -site {L6} [get_ports RASP_IO04]
```

```
ldc_set_location -site {N3} [get_ports RASP_IO05]
ldc_set_location -site {N4} [get_ports RASP_IO06]
ldc_set_location -site {P1} [get_ports RASP_IO07]
ldc_set_location -site {P2} [get_ports RASP_IO08]
ldc_set_location -site {M1} [get_ports RASP_IO09]
ldc_set_location -site {M2} [get_ports RASP_IO10]
ldc_set_location -site {N1} [get_ports RASP_IO11]
ldc_set_location -site {P3} [get_ports RASP_IO12]
ldc_set_location -site {P4} [get_ports RASP_IO13]
ldc_set_location -site {M7} [get_ports RASP_IO14]
ldc_set_location -site {K3} [get_ports RASP_IO15]
ldc_set_location -site {M5} [get_ports RASP_IO16]
ldc_set_location -site {L5} [get_ports RASP_IO17]
ldc_set_location -site {M6} [get_ports RASP_IO18]
ldc_set_location -site {P5} [get_ports RASP_IO19]
ldc_set_location -site {N7} [get_ports RASP_IO20]
ldc_set_location -site {M8} [get_ports RASP_IO21]
ldc_set_location -site {L2} [get_ports RASP_IO22]
ldc_set_location -site {L3} [get_ports RASP_IO23]
ldc_set_location -site {L1} [get_ports RASP_IO24]
ldc_set_location -site {N2} [get_ports RASP_IO25]
ldc_set_location -site {P6} [get_ports RASP_IO26]
ldc_set_location -site {L4} [get_ports RASP_IO27]
ldc_set_location -site {K1} [get_ports RASP_ID_SC]
ldc_set_location -site {K2} [get_ports RASP_ID_SD]
```

#### //VERSA HEADER Connections

```
ldc_set_location -site {D3} [get_ports EXPCON_IO0]
ldc_set_location -site {E4} [get_ports EXPCON_IO1]
ldc_set_location -site {C3} [get_ports EXPCON_IO2]
ldc_set_location -site {C2} [get_ports EXPCON_IO3]
ldc_set_location -site {A4} [get_ports EXPCON_IO4]
ldc_set_location -site {E5} [get_ports EXPCON_IO5]
ldc_set_location -site {F6} [get_ports EXPCON_IO6]
ldc_set_location -site {C5} [get_ports EXPCON_IO7]
ldc_set_location -site {B2} [get_ports EXPCON_IO8]
ldc_set_location -site {A2} [get_ports EXPCON_IO9]
ldc_set_location -site {B3} [get_ports EXPCON_IO10]
ldc_set_location -site {A3} [get_ports EXPCON_IO11]
ldc_set_location -site {B4} [get_ports EXPCON_IO12]
ldc_set_location -site {D5} [get_ports EXPCON_IO13]
ldc_set_location -site {A5} [get_ports EXPCON_IO14]
ldc_set_location -site {B5} [get_ports EXPCON_IO15]
ldc_set_location -site {A6} [get_ports EXPCON_IO16]
ldc_set_location -site {B6} [get_ports EXPCON_IO17]
ldc_set_location -site {A7} [get_ports EXPCON_IO18]
ldc_set_location -site {A8} [get_ports EXPCON_IO19]
ldc_set_location -site {C6} [get_ports EXPCON_IO20]
ldc_set_location -site {B8} [get_ports EXPCON_IO21]
ldc_set_location -site {B9} [get_ports EXPCON_IO22]
ldc_set_location -site {A9} [get_ports EXPCON_IO23]
ldc_set_location -site {D6} [get_ports EXPCON_IO24]
ldc_set_location -site {C8} [get_ports EXPCON_IO25]
ldc_set_location -site {E7} [get_ports EXPCON_IO26]
ldc_set_location -site {E8} [get_ports EXPCON_IO27]
ldc_set_location -site {E6} [get_ports EXPCON_IO28]
ldc_set_location -site {C20} [get_ports EXPCON_IO29]
ldc_set_location -site {H14} [get_ports EXPCON_IO30]
```

```
ldc_set_location -site {G14} [get_ports EXPCON_IO31]
ldc_set_location -site {H15} [get_ports EXPCON_IO32]
ldc_set_location -site {G18} [get_ports EXPCON_IO33]
ldc_set_location -site {H16} [get_ports EXPCON_IO34]
ldc_set_location -site {G19} [get_ports EXPCON_IO35]
ldc_set_location -site {H20} [get_ports EXPCON_IO36]
ldc_set_location -site {H19} [get_ports EXPCON_IO37]
ldc_set_location -site {J17} [get_ports EXPCON_IO38]
ldc_set_location -site {J18} [get_ports EXPCON_IO39]
ldc_set_location -site {J15} [get_ports EXPCON_IO40]
ldc_set_location -site {J16} [get_ports EXPCON_IO41]
ldc_set_location -site {J13} [get_ports EXPCON_IO42]
ldc_set_location -site {J14} [get_ports EXPCON_IO43]
ldc_set_location -site {J12} [get_ports EXPCON_IO44]
ldc_set_location -site {H13} [get_ports EXPCON_IO45]
ldc_set_location -site {E16} [get_ports EXPCON_OSC]
ldc_set_location -site {E17} [get_ports EXPCON_CLKIN]
ldc_set_location -site {D20} [get_ports EXPCON_CLKOUT]
ldc_set_location -site {F5} [get_ports HPE_RESOUT#]
ldc_set_location -site {D8} [get_ports HPE_CARDSEL#]
```

## //Aardvark Header Connections

```
ldc_set_location -site {M19} [get_ports AK_SCL]
ldc_set_location -site {M20} [get_ports AK_SDA]
ldc_set_location -site {N14} [get_ports AK_MISO]
ldc_set_location -site {N15} [get_ports AK_SCLK]
ldc_set_location -site {N16} [get_ports AK_SS]
ldc_set_location -site {N17} [get_ports AK_MOSI]
```

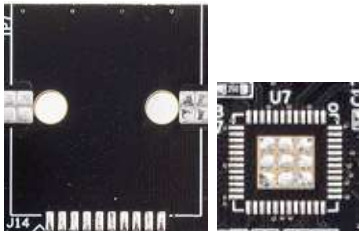
## //Arduino Header Connections

```
ldc_set_location -site {J19} [get_ports AR_IO0]
ldc_set_location -site {J20} [get_ports AR_IO1]
ldc_set_location -site {K12} [get_ports AR_IO2]
ldc_set_location -site {K13} [get_ports AR_IO3]
ldc_set_location -site {K14} [get_ports AR_IO4]
ldc_set_location -site {K15} [get_ports AR_IO5]
ldc_set_location -site {K16} [get_ports AR_IO6]
ldc_set_location -site {K17} [get_ports AR_IO7]
ldc_set_location -site {L12} [get_ports AR_IO8]
ldc_set_location -site {L13} [get_ports AR_IO9]
ldc_set_location -site {L14} [get_ports AR_SS_IO10]
ldc_set_location -site {L15} [get_ports AR_MOSI_IO11]
ldc_set_location -site {L16} [get_ports AR_MISO_IO12]
ldc_set_location -site {K19} [get_ports AR_SCK_IO13]
ldc_set_location -site {L20} [get_ports AR_IO14]
ldc_set_location -site {N18} [get_ports AR_SDA]
ldc_set_location -site {N19} [get_ports AR_SCL]
ldc_set_location -site {K20} [get_ports AR_RESET]
ldc_set_location -site {M11} [get_ports AR_AD0]
ldc_set_location -site {M12} [get_ports AR_AD1]
ldc_set_location -site {M13} [get_ports AR_AD2]
ldc_set_location -site {M14} [get_ports AR_AD3]
ldc_set_location -site {M17} [get_ports AR_AD4]
ldc_set_location -site {M18} [get_ports AR_AD5]
```

## Appendix D. MachXO5-NX Development Board Revision Information

### MachXO5-NX Development Board – Working with Revision A

#### BOM Difference of Revision A Board

| Feature Variations   | Without Ethernet                                                                  | With Ethernet                                                                      | Application Notes                       |
|----------------------|-----------------------------------------------------------------------------------|------------------------------------------------------------------------------------|-----------------------------------------|
| Major Identification |  |  | J14 – Top View<br>U7 – Bottom View      |
| BOM Difference       | J14 and U7 NOT installed                                                          | Production version, BOM full populated according to Appendix B                     | Caused by BOM supply issues             |
| OPN                  | LFMXO5-25-EVN                                                                     | LFMXO5-25-E-EVN                                                                    | Both PCB printed:<br>P/N: LFMXO5-25-EVN |

## References

For more information, refer to the following documents:

- [MachXO5 Programming and Configuration User Guide \(FPGA-TN-02271\)](#)
- [Programming Cable User Guide \(FPGA-UG-02042\)](#)



## Revision History

### Revision 1.1, December 2022

| Section                           | Change Summary       |
|-----------------------------------|----------------------|
| Generating the Programming File   | Newly added section. |
| Programming the MachXO5-NX Device |                      |

### Revision 1.0, June 2022

| Section | Change Summary      |
|---------|---------------------|
| All     | Production release. |

### Revision 0.90, May 2022

| Section | Change Summary       |
|---------|----------------------|
| All     | Preliminary release. |



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