SBOS390A–JANUARY 2008–REVISED MARCH 2008

8-Channel, Ultralow-Power, Variable Gain Amplifier with Low-Noise Pre-Amp

FEATURES

- **Ultralow Power: 65mW/Channel**
- **Low Noise: 0.8nV/√Hz**
- **Low-Noise Pre-Amp (LNP):**
  - **20dB Fixed Gain**
  - **250mV$_{PP}$ Linear Input Range**
- **Variable Gain Amplifier:**
  - **Gain Control Range: 46dB**
  - **Selectable PGA Gain: 20dB, 25dB, 27dB, 30dB**
  - **Fast Overload Recovery**
  - **Output Clamping Control**
- **Integrated Low-Pass Filter:**
  - **Second-Order, Linear Phase**
  - **Bandwidth: 10MHz, 15MHz**
- **High Accuracy:**
  - **Low Gain Error: ±0.5dB**
  - **Excellent Channel Matching: ±0.25dB**
- **Distortion, HD2: –50dBc at 5MHz**
- **Integrated CW Switch Matrix:**
  - **Easy Current Summing**
- **Serial Control Interface**
- **Small Package: QFN-64, 9×9mm**

APPLICATIONS

- **Medical Imaging, Ultrasound Systems**
  - **Portable Systems**
  - **Low- and Mid-Range Systems**

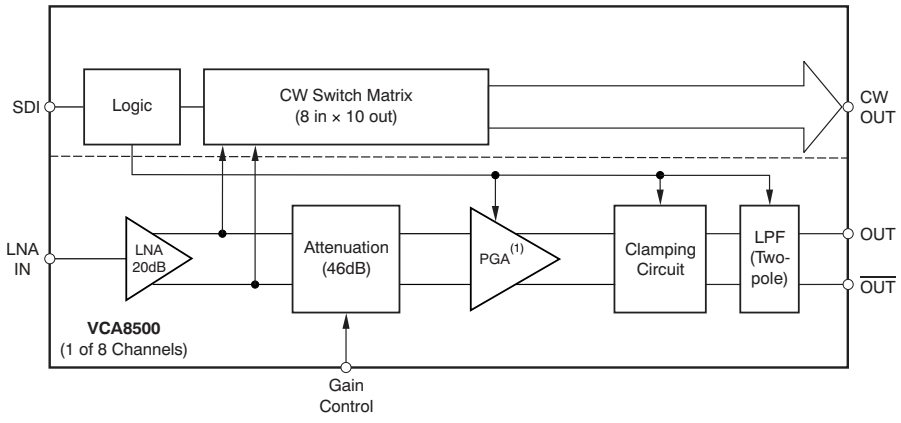
DESCRIPTION

The VCA8500 is an 8-channel variable gain amplifier consisting of a low-noise pre-amplifier (LNP) and a variable-gain amplifier (VGA). This combination, along with the device features, makes it ideal for a variety of ultrasound systems.

The LNP gain is fixed at 20dB, and has excellent noise and signal handling characteristics. The gain of the voltage-controlled attenuator can vary over a 46dB range with a 0V to 1.2V control voltage common to all channels of the VCA8500.

The post-gain amplifier (PGA) can be programmed for four gain settings: 20dB, 25dB, 27dB, or 30dB gain. As a means to improve system overload recovery time, the VCA8500 provides an internal clamping function. The PGA settings as well the clamp levels are controlled through the serial interface.

The VCA8500 is built on TI's BiCOM process and is available in a small QFN-64 PowerPAD™ package.



NOTE (1): 20dB, 25dB, 27dB, or 30dB gain setting.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY	ECO STATUS(2)
VCA8500	QFN-64	RGC	–40°C to +85°C	VCA8500	VCA8500IRGCT	Tape and Reel, 250	Pb-Free, Green
					VCA8500IRGCR	Tape and Reel, 2000	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) **Eco-Status information:** Additional details including specific material content can be accessed at www.ti.com/leadfree
GREEN: Ti defines Green to mean Lead (Pb)-Free and in addition, uses less package materials that do not contain halogens, including bromine (Br), or antimony (Sb) above 0.1% of total product weight.
N/A: Not yet available Lead (Pb)-Free; for estimated conversion dates, go to www.ti.com/leadfree.
Pb-FREE: Ti defines Lead (Pb)-Free to mean RoHS compatible, including a lead concentration that does not exceed 0.1% of total product weight, and, if designed to be soldered, suitable for use in specified lead-free soldering processes.

NOTE

These packages conform to Lead-Free and Green Manufacturing Specifications.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Over operating free-air temperature range, unless otherwise noted.

PARAMETER		VCA8500	UNIT
Supply voltage range, AVDD1		–0.3 to +3.9	V
Supply voltage range, AVDD2		–0.3 to +6	V
Supply voltage range, DVDD		–0.3 to +3.9	V
Voltage at analog inputs		–0.3 to (AVDD1 +0.3)	V
Voltage at digital inputs		–0.3 to (DVDD to +0.3)	V
Soldering temperature (lead, 5s)(3)		+260	°C
Maximum junction temperature (T_J), any condition(2)		+150	°C
Maximum junction temperature (T_J), continuous operation, long-term reliability(2)		+125	°C
Storage temperature range, T_{stg}		–55 to +150	°C
Operating temperature range, T_A		–40 to +85	°C
ESD rating	Human body model (HBM)	2000	V
	Charged device model (CDM)	1000	V
	Machine model (MM)	200	V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to the ground terminal, which is the exposed thermal pad of the package.

(3) Both the part being reworked and the board must be baked out before rework to reduce the risk of delamination. Refer to Application Note SLUA271 (available for download at www.ti.com) for recommended rework techniques.

ELECTRICAL CHARACTERISTICS

All specifications at T_A = +25°C, AVDD2 = 5.0V, AVDD1 = DVDD = 3.3V; single-ended, ac-coupled (1µF) input configuration to the preamp (LNA), f_{IN} = 5MHz, V_{CNTL} = 1.0V, PG = 30dB, clamp disabled (CL = 1), LPF = 15MHz, and R_{LOAD} = 1kΩ on each output to ground, unless otherwise noted.

PARAMETER	TEST CONDITIONS	VCA8500			UNIT	TEST LEVEL(1)
		MIN	TYP	MAX		
PREAMPLIFIER (LNA)						
LNA gain	Single-ended input to differential output		20		dB	C
Input voltage	Linear operation (THD ≤ –40dBc)		250		mV_{PP}	C
Input voltage noise	At f = 2MHz		0.70		$nV/\sqrt{Hz}$	B
Input current noise	At f = 2MHz		3.0		$pA/\sqrt{Hz}$	B
Input bias voltage (V_{BL})	Internally generated		+2.4		V	B
Bandwidth	Small-signal, –3dB		55		MHz	C
Input resistance(2)	At f = 4MHz		8		kΩ	C
Input capacitance(2)	Including internal ESD and clamping diodes		30		pF	C
TGC SIGNAL PATH (LNA, VCA, PGA)						
Input voltage noise	PGA = 30dB, R_S = 0Ω, f = 2MHz		0.81		$nV/\sqrt{Hz}$	B
	PGA = 20dB, R_S = 0Ω, f = 2MHz		0.95		$nV/\sqrt{Hz}$	B
Noise figure	R_S = 200Ω, f = 1MHz to 10MHz		1.1		dB	C
Group delay variation	1MHz to 10MHz		±3		ns	B
Overload recovery time	To within 1% of $2V_{PP}$ output (V_{CNTL} = 0.54V), PGA = 20dB		80		ns	B
Output voltage (V_{OUT})	Differential, non-clipped		2		V_{PP}	B
Output common-mode voltage (V_{CM})			+1.65		V	B
Output impedance	DC to 10MHz, single-ended, either output		1		Ω	C
Output current	R_L = 5Ω into V_{CM}		±20		mA	B
Second-harmonic distortion	f_{IN} = 5MHz, PGA = 20dB, V_{OUT} = $1V_{PP}$	–50	–60		dBc	A
	f_{IN} = 5MHz, PGA = 30dB, V_{OUT} = $2V_{PP}$	–42	–55		dBc	A
Third-harmonic distortion	f_{IN} = 5MHz, PGA = 20dB, V_{OUT} = $1V_{PP}$	–48	–68		dBc	A
	f_{IN} = 5MHz, PGA = 30dB, V_{OUT} = $2V_{PP}$	–40	–50		dBc	A
Two-tone intermodulation	f_1 = 4.99MHz, f_2 = 5.01MHz, V_{CNTL} = 1V; V_{OUT} = $1V_{PP}$		–52		dBc	B
Crosstalk, channel-to-channel	Worst case; PGA = 20dB, V_{CNTRL} = 0.6V, V_{OUT} = $1V_{PP}$		–67		dBc	B
	PGA = 30dB, V_{OUT} = $1V_{PP}$		–66		dBc	B
FILTER						
Low-pass filter (second-order)	–3dB point		10, 15		MHz	B
Tolerance			±15		%	B
High-pass filter (first-order, due to internal ac coupling)	–3dB point, V_{CNTL} = 1.2V		150		kHz	C

(1) Test levels: **(A)** 100% tested at +25°C. Over temperature limits set by characterization and simulation. **(B)** Limits set by characterization and simulation, not production tested. **(C)** Typical value only for information.
(2) See Figure 29 of the Typical Characteristics.

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, AVDD2 = 5.0V, AVDD1 = DVDD = 3.3V; single-ended, ac-coupled (1µF) input configuration to the preamp (LNA), f_{IN} = 5MHz, V_{CNTL} = 1.0V, PG = 30dB, clamp disabled (CL = 1), LPF = 15MHz, and R_{LOAD} = 1kΩ on each output to ground, unless otherwise noted.

PARAMETER	TEST CONDITIONS	VCA8500			UNIT	TEST LEVEL(1)
		MIN	TYP	MAX		
ACCURACY						
Gain (PGA)	Selectable through SPI™		20, 25, 27, 30		dB	A
Total gain, maximum	LNA + PGA gain, V_{CNTL} = 1.2V	48	49.5	51	dB	A
Gain range	V_{CNTL} = 0V to 1.2V		46		dB	A
Gain range	V_{CNTL} = 0.1V to 1.0V		40		dB	A
Gain slope	V_{CNTL} = 0.1V to 1.0V		44.4		dB/V	A
Gain error, absolute	0V < V_{CNTL} < 0.1V		±0.5		dB	A
	0.1V < V_{CNTL} < 1.0V	–1.5	±0.5	+1.5	dB	A
	1.0V < V_{CNTL} < 1.2V		±0.5		dB	A
Gain matching	Channel-to-channel		±0.25	±0.5	dB	A
Output offset voltage	Differential	–25	±1	+25	mV	A
	Single-ended(3)	–50	±25	+50	mV	A
Clamp level (V_{OUT})	CL = 0		1.7		V_{PP}	A
	CL = 1 (clamp disabled)		2.8		V_{PP}	B
GAIN CONTROL INTERFACE						
Input voltage range (V_{CNTL})	Gain range = 46dB		0 to 1.2		V	A
Input resistance			25		kΩ	C
Response time	V_{CNTL}= 0V to 1.2V step; to 90% signal level, V_{OUT} = 1V_{PP}		0.5		µs	B
Gain control bandwidth			1.5		MHz	C
CW SIGNAL PATH						
Output transconductance (V/I)	At V_{IN} = 100mV_{PP}	14	16.4	18	mA/V	A
	At V_{IN} = 200mV_{PP}		14.5		mA/V	B
Dynamic CW output current, max			2.9		mA_{PP}	B
Static CW output current (sink)			0.9		mA	B
Output common-mode voltage (V_{CM0})	Supplied externally		+2.5		V	B
Output compliance range	Symmetric around V_{CMO}		±0.5		V	B
Output capacitance			10		pF	C
Output impedance			50		kΩ	C
Input voltage noise, CW mode	At f = 2MHz		1.15		nV/√Hz	B
Signal-dependent noise (RTO)	At 2kHz offset from 2MHz CW carrier		+2		dB	B
	At 2kHz offset from 5MHz CW carrier		+2		dB	B
Output noise correlation factor	Summing of eight channels (all modes) [compared to ideal 0dB]		0.6		dB	B

(3) Deviation from ideal common-mode voltage (V_{CM} = 1.65V).

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, AVDD2 = 5.0V, AVDD1 = DVDD = 3.3V; single-ended, ac-coupled (1µF) input configuration to the preamp (LNA), f_{IN} = 5MHz, V_{CNTL} = 1.0V, PG = 30dB, clamp disabled (CL = 1), LPF = 15MHz, and R_{LOAD} = 1kΩ on each output to ground, unless otherwise noted.

PARAMETER	TEST CONDITIONS	VCA8500			UNIT	TEST LEVEL(1)
		MIN	TYP	MAX		
DIGITAL INPUTS (SDI)	(PD, DIN, DOUT, CLK, RST)					
V_{IH}, high-level input voltage		2.0		V_D	V	B
V_{IL}, low-level input voltage		0		0.8	V	B
Input current			±10		µA	A
Clock frequency (f_{CLK})		10k		20M	Hz	B
Input resistance			1		MΩ	C
Input capacitance			5		pF	C
POWER SUPPLY						
Supply Voltages						
AVDD1, DVDD	Operating	3.15	3.3	3.6	V	B
AVDD2	Operating	4.75	5	5.25	V	B
Supply Currents(4)						
IAVDD1	TGC mode (D5 = 1)		145	156	mA	A
	CW mode (D5 = 0)		78	84	mA	A
IDVDD	TGC, CW mode		1.5	3	mA	A
IAVDD2	TGC mode		8	10	mA	A
	CW mode		54	59	mA	A
Power dissipation, total	All channels, TGC mode, no signal		522	570	mW	A
	All channels, CW mode, no signal		533	575	mW	A
POWER-DOWN MODES						
Standby Mode	PD (pin 49) = high					
IAVDD1			18		mA	A
IDVDD			1.5		mA	A
IAVDD2			8		mA	A
Power dissipation			104	130	mW	A
Power-down response time			0.2		µs	C
Power-up response time(5)	PD to valid output (90% level)		50		µs	C
Shut-Down Mode	D2 (PWR) = high					
IAVDD1			1.5		mA	A
IDVDD			1.5		mA	A
IAVDD2			2		mA	A
Power dissipation			19	35	mW	A
THERMAL CHARACTERISTICS						
Temperature range	Ambient, operating	–40		+85	°C	
Thermal resistance, θ_{JA}	Soldered pad; four-layer PCB with thermal vias		22.5		°C/W	
Thermal resistance, θ_{JC}			17.0		°C/W	

(4) Clamp enabled (D4 = 0).
(5) See Figure 59 of the Typical Characteristics.

DEVICE INFORMATION

RGC PACKAGE
QFN-64
(TOP VIEW)

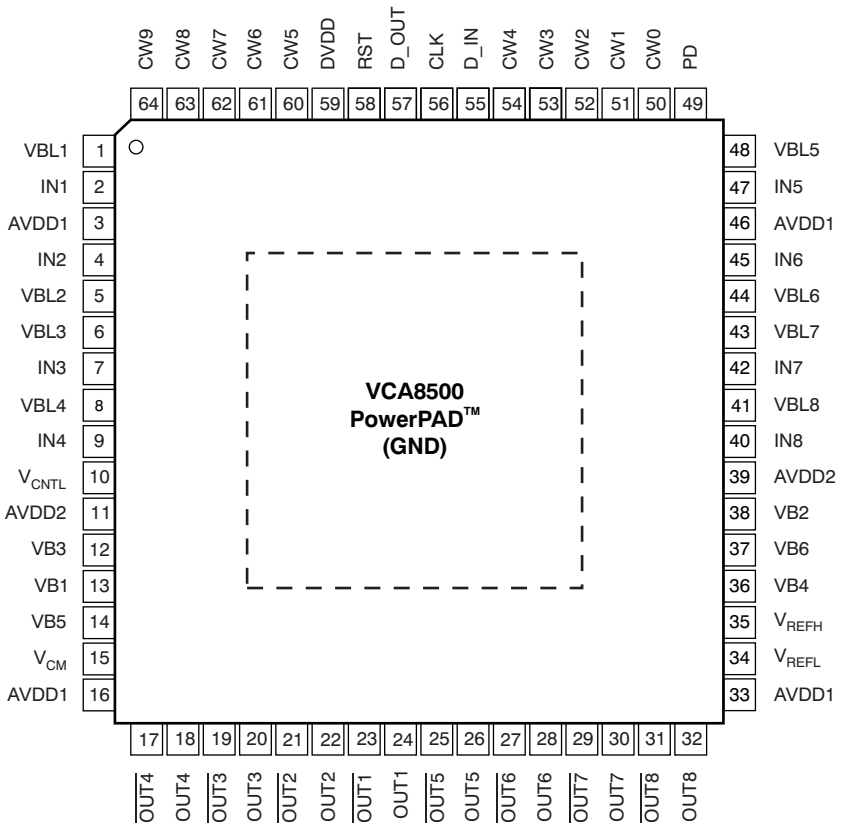


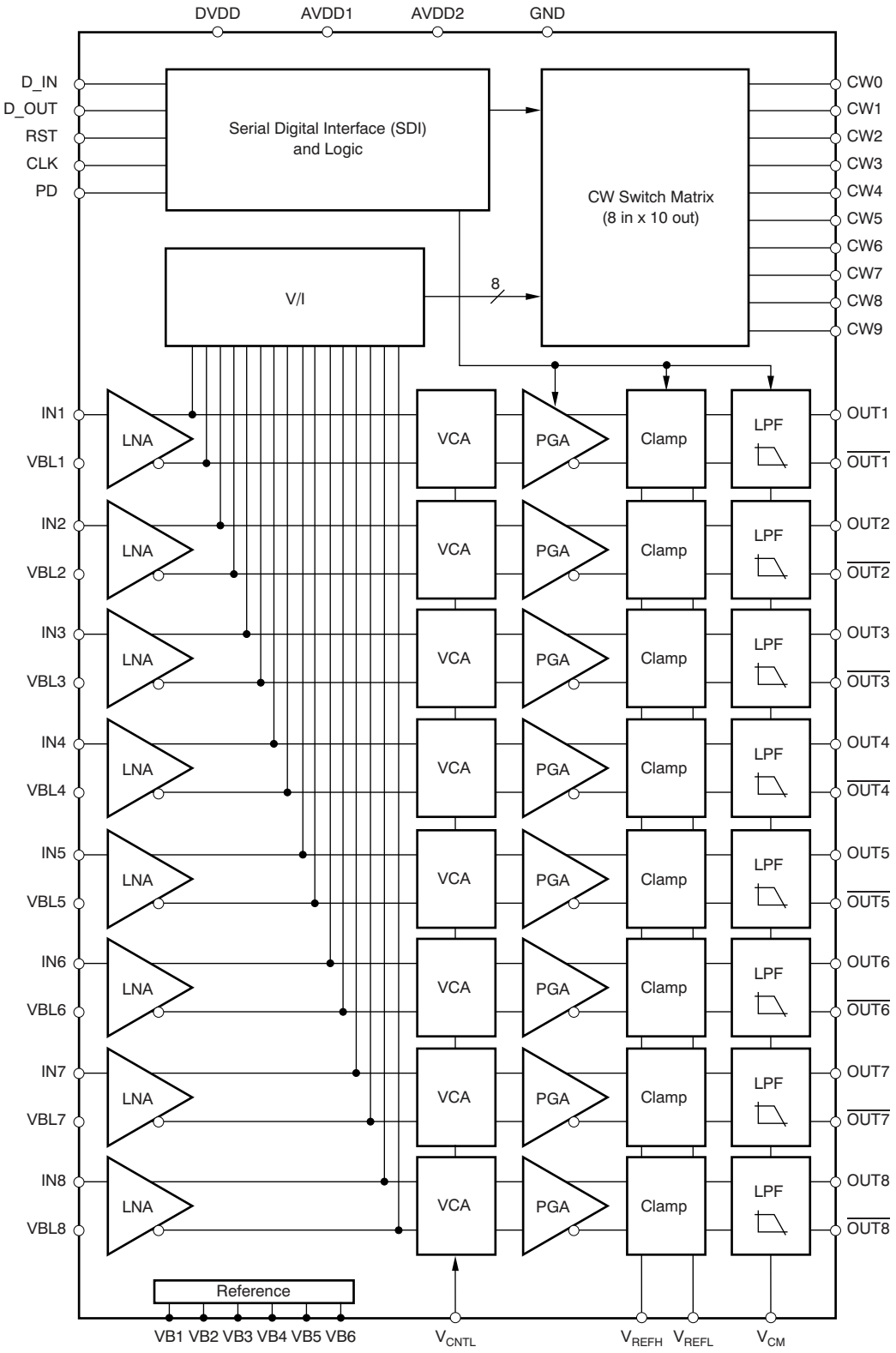
Table 1. TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
PIN NO.	NAME		
1	VBL1		LNA bias voltage (+2.4V); bypass with 0.1μF capacitor (min)
2	IN1	I	LNA input channel 1
3	AVDD1		+3.3V analog supply
4	IN2	I	LNA input channel 2
5	VBL2		LNA bias voltage (+2.4V); bypass with 0.1μF capacitor (min)
6	VBL3		LNA bias voltage (+2.4V); bypass with 0.1μF capacitor (min)
7	IN3	I	LNA input channel 3
8	VBL4		LNA bias voltage (+2.4V); bypass with 0.1μF capacitor (min)
9	IN4		LNA input channel 4
10	V_{CNTL}	I	Attenuator control voltage input (all channels)
11	AVDD2		+5V analog supply (VCA, CW)
12	VB3		Internal bias voltage (+4.2V); bypass with 0.1μF capacitor (min)
13	VB1		Internal bias voltage (+2.4V); bypass with 2.2μF capacitor (1.0μF min)
14	VB5		Internal bias voltage (+2.4V); bypass with 0.1μF capacitor (min)
15	V_{CM}		Internal common-mode voltage (+1.65V); bypass with 0.1μF capacitor (min)
16	AVDD1		+3.3V analog supply
17	$\overline{OUT4}$	O	PGA output channel 4 (inverted)
18	OUT4	O	PGA output channel 4

Table 1. TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
PIN NO.	NAME		
19	$\overline{\text{OUT3}}$	O	PGA output channel 3 (inverted)
20	OUT3	O	PGA output channel 3
21	$\overline{\text{OUT2}}$	O	PGA output channel 2 (inverted)
22	OUT2	O	PGA output channel 2
23	$\overline{\text{OUT1}}$	O	PGA output channel 1 (inverted)
24	OUT1	O	PGA output channel 1
25	$\overline{\text{OUT5}}$	O	PGA output channel 5 (inverted)
26	OUT5	O	PGA output channel 5
27	$\overline{\text{OUT6}}$	O	PGA output channel 6 (inverted)
28	OUT6	O	PGA output channel 6
29	$\overline{\text{OUT7}}$	O	PGA output channel 7 (inverted)
30	OUT7	O	PGA output channel 7
31	$\overline{\text{OUT8}}$	O	PGA output channel 8 (inverted)
32	OUT8	O	PGA output channel 8
33	AVDD1		+3.3V analog supply
34	V_{REFL}		Clamp reference level low, 2.0V; bypass with 0.1μF capacitor (min)
35	V_{REFH}		Clamp reference level high, 2.7V; bypass with 0.1μF capacitor (min)
36	VB4		Internal bias voltage (+2.4V); bypass with 0.1μF capacitor (min)
37	VB6		Internal bias voltage (+2.9V); bypass with 0.1μF capacitor (min)
38	VB2		Internal bias voltage (+2.7V); bypass with 0.1μF capacitor (min)
39	AVDD2		+5V analog supply (VCA, CW)
40	IN8	I	LNA input channel 8
41	VBL8		LNA bias voltage (+2.4V); bypass with 0.1μF capacitor (min)
42	IN7	I	LNA input channel 7
43	VBL7		LNA bias voltage (+2.4V); bypass with 0.1μF capacitor (min)
44	VBL6	I	LNA bias voltage (+2.4V); bypass with 0.1μF capacitor (min)
45	IN6		LNA input channel 6
46	AVDD1		+3.3V analog supply
47	IN5	I	LNA input channel 5
48	VBL5		LNA bias voltage (+2.4V); bypass with 0.1μF capacitor (min)
49	PD	I	Power-down pin for standby mode; 0 = normal operation, 1 = power down
50	CW0	O	CW channel 0 current output
51	CW1	O	CW channel 1 current output
52	CW2	O	CW channel 2 current output
53	CW3	O	CW channel 3 current output
54	CW4	O	CW channel 4 current output
55	D_IN	I	Serial data input
56	CLK	I	Clock input for serial interface
57	D_OUT	O	Serial data output
58	RST	I	Reset input; rising edge resets register to default values.
59	DVDD		+3.3V digital supply; connect to a low-noise analog supply plane (AVDD1)
60	CW5		CW channel 5 current output
61	CW6		CW channel 6 current output
62	CW7		CW channel 7 current output
63	CW8		CW channel 8 current output
64	CW9		CW channel 9 current output
—	GND		PowerPAD must be connected to the analog ground of the printed circuit board; use this ground for bypass capacitor return ground.

FUNCTIONAL BLOCK DIAGRAM



INPUT REGISTER BIT MAPS

Register Map

BYTE #1	BYTE #2		BYTE #3		BYTE #4		BYTE #5	
D0:D7	D8:D11	D12:D15	D16:D19	D20:D23	D24:D27	D28:D31	D32:D35	D36:D39
Control	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8

Table 2. Default Register Configuration

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	0	1	1

Table 3. Byte 1—Control Byte Register Map

BIT #	NAME	DESCRIPTION
D0 (LSB)	1	Start bit; must be a '1' (high); 40-bit countdown starts with first falling clock edge.
D1	R/$\overline{W}$	1 = Write, 0 = Read; read prevents latching of new data/bits. Control register remains latched with previously loaded data.
D2	PWR	1 = Power-down mode enabled (shutdown).
D3	BW	Low-pass filter bandwidth setting (see Table 8)
D4	CL	Clamp level setting (see Table 8)
D5	Mode	1 = TGC mode, 0 = CW doppler mode (TGC powered down)
D6	PG0	LSB of PGA gain control (see Table 9)
D7 (MSB)	PG1	MSB of PGA gain control

Table 4. Byte 2—First Data Byte

BIT #	NAME	DESCRIPTION
D8 (LSB)	DB1:1	Channel 1, LSB of matrix control
D9	DB1:2	Channel 1, matrix control
D10	DB1:3	Channel 1, matrix control
D11	DB1:4	Channel 1, MSB of matrix control
D12	DB2:1	Channel 2, LSB of matrix control
D13	DB2:2	Channel 2, matrix control
D14	DB2:3	Channel 2, matrix control
D15 (MSB)	DB2:4	Channel 2; MSB of matrix control

Table 5. Byte 3—Second Data Byte

BIT #	NAME	DESCRIPTION
D16 (LSB)	DB3:1	Channel 3, LSB of matrix control
D17	DB3:2	Channel 3, matrix control
D18	DB3:3	Channel 3, matrix control
D19	DB3:4	Channel 3, MSB of matrix control
D20	DB4:1	Channel 4, LSB of matrix control
D21	DB4:2	Channel 4, matrix control
D22	DB4:3	Channel 4, matrix control
D23 (MSB)	DB4:4	Channel 4, MSB of matrix control

Table 6. Byte 4—Third Data Byte

BIT #	NAME	DESCRIPTION
D24 (LSB)	DB5:1	Channel 5, LSB of matrix control
D25	DB5:2	Channel 5, matrix control
D26	DB5:3	Channel 5, matrix control
D27	DB5:4	Channel 5, MSB of matrix control
D28	DB6:1	Channel 6; LSB of matrix control
D29	DB6:2	Channel 6, matrix control
D30	DB6:3	Channel 6, matrix control
D31 (MSB)	DB6:4	Channel 6, MSB of matrix control

Table 7. Byte 5—Fourth Data Byte

BIT #	NAME	DESCRIPTION
D32 (LSB)	DB7:1	Channel 7, LSB of matrix control
D33	DB7:2	Channel 7, matrix control
D34	DB7:3	Channel 7, matrix control
D35	DB7:4	Channel 7, MSB of matrix control
D36	DB8:1	Channel 8; LSB of matrix control
D37	DB8:2	Channel 8, matrix control
D38	DB8:3	Channel 8, matrix control
D39 (MSB)	DB8:4	Channel 8, MSB of matrix control

Table 8. Clamp Level and LPF Bandwidth Setting

NAME	SETTING	FUNCTION
BW	D3 = 0	Bandwidth set to 15MHz (default)
	D3 = 1	Bandwidth set to 10MHz
CL	D4 = 0	Clamps the output signal at $1.7V_{PP}$ on each PGA output channel (default)
	D4 = 1	Clamp transparent (disabled)

Table 9. PGA Gain Setting

PG1	PG0	FUNCTION
0	0	Set PGA gain to 20dB (default)
0	1	Set PGA gain to 25dB
1	0	Set PGA gain to 27dB
1	1	Set PGA gain to 30dB

Table 10. CW Switch Matrix Control for Each Channel

DBn:4 (MSB)	DBn:3	DBn:2	DBn:1 (LSB)	LNA Input Channel Directed To:
0	0	0	0	Output CW0
0	0	0	1	Output CW1
0	0	1	0	Output CW2
0	0	1	1	Output CW3
0	1	0	0	Output CW4
0	1	0	1	Output CW5
0	1	1	0	Output CW6
0	1	1	1	Output CW7
1	0	0	0	Output CW8
1	0	0	1	Output CW9
1	0	1	0	Connected to AVDD2; channel disabled
1	0	1	1	Connected to AVDD2; channel disabled
1	1	0	0	Connected to AVDD2; channel disabled
1	1	0	1	Connected to AVDD2; channel disabled
1	1	1	0	Connected to AVDD2; channel disabled
1	1	1	1	Connected to AVDD2; channel disabled

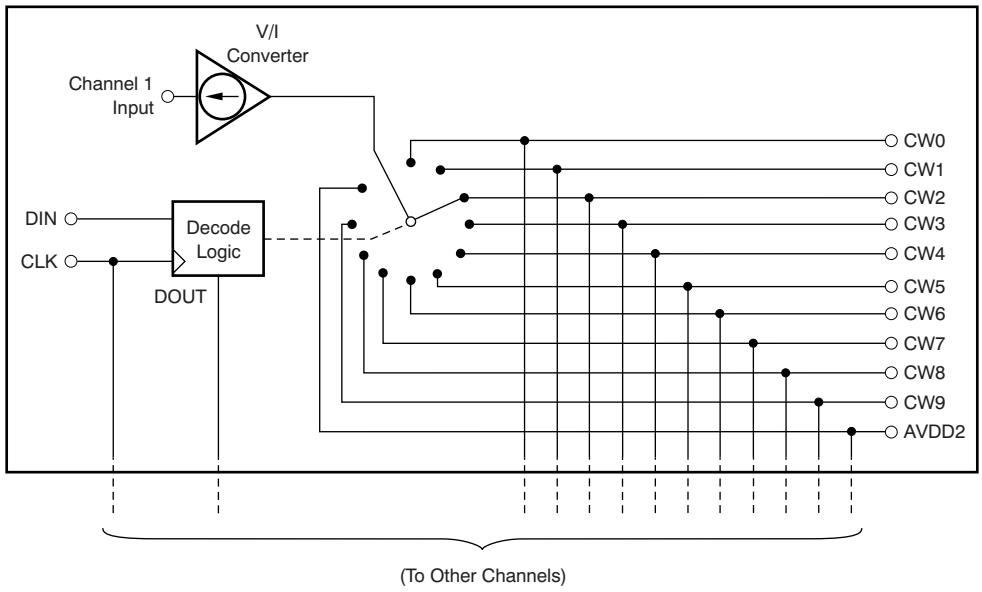
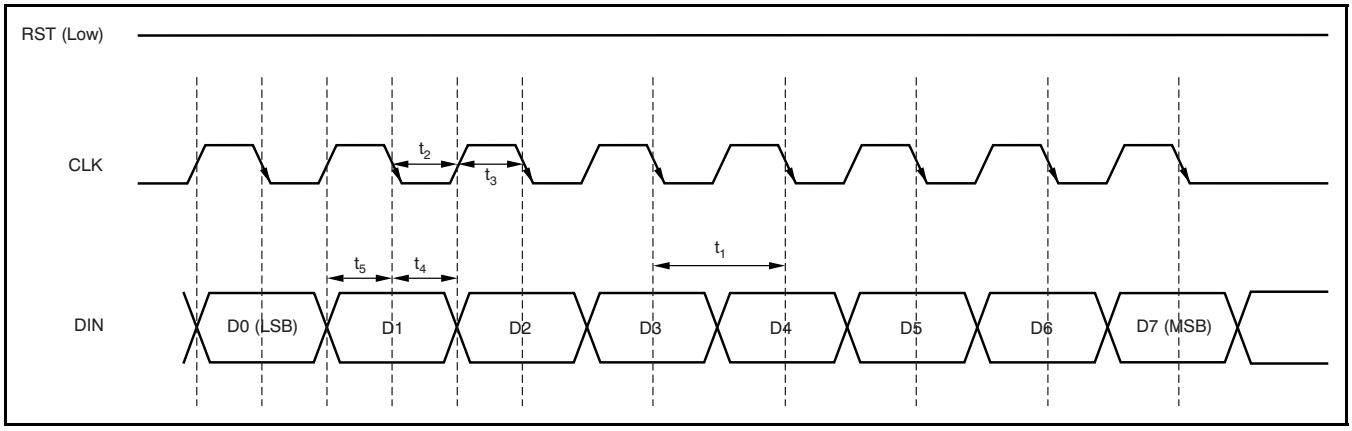


Figure 1. Basic CW Cross-Point Switch Matrix Configuration

SERIAL DIGITAL INTERFACE (SDI)

- All writes and reads are five bytes at a time. Each byte consists of 8 bits, for a total instruction set of 40 bits.
- Data are latched on the falling edge of CLK.
- Separate write (DIN) and read data (DOUT) lines.
- Reads follow the same bitstream pattern seen in the write cycle.
- Reads extract data from the FIFO buffer, not the latched register.
- DOUT data are continuously available and do not need to be enabled with a read cycle. Selecting a read cycle in the control register only prevents latching of data. The control register remains latched.
- The Reset pin (RST) must be low in order to allow the register to update with new data. RST can be held low permanently. To initiate a reset cycle, pull the RST pin high for at least 100ns.

TIMING INFORMATION



NOTE: This figure shows timing example for one data byte. A full register update cycle requires all five bytes (that is, 40 bits).

SERIAL PORT TIMING TABLE

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_1	Serial CLK period	100			ns
t_2	Serial CLK HIGH time	40			ns
t_3	Serial CLK LOW time	40			ns
t_4	Data hold time	5			ns
t_5	Data setup time	5			ns
RST	Reset pulse (L - H - L)	100			ns

TYPICAL CHARACTERISTICS

All specifications at T_A = +25°C, AVDD2 = 5.0V, AVDD1 = DVDD = 3.3V; single-ended, ac-coupled (1µF) input configuration to the preamp (LNA), f_{IN} = 5MHz, V_{CNTL} = 1.0V, clamp disabled (CL = 1), LPF = 15MHz, and R_{LOAD} = 1kΩ on each output to ground, unless otherwise noted.

GAIN vs V_{CNTRL} (at PGA = X)

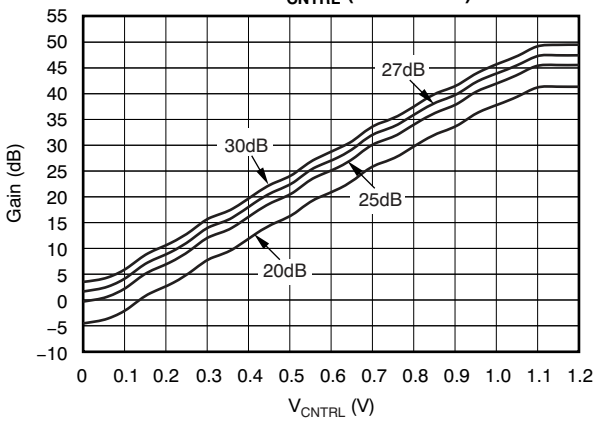


Figure 2.

GAIN ERROR vs V_{CNTRL}

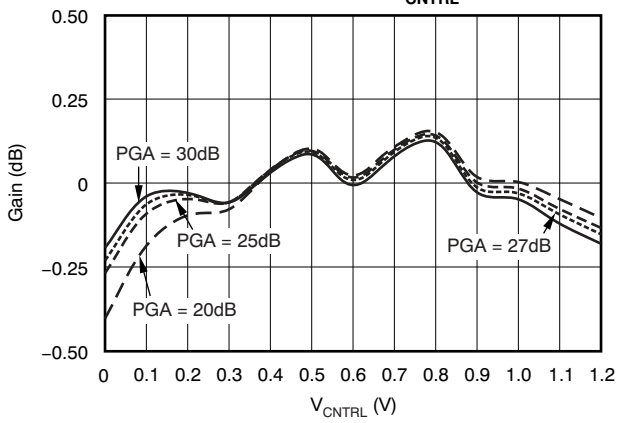


Figure 3.

GAIN vs V_{CNTRL} OVER TEMPERATURE

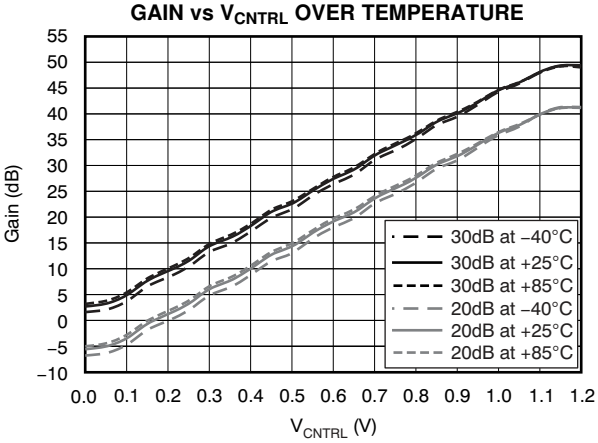


Figure 4.

GAIN ERROR DRIFT vs V_{CNTRL}

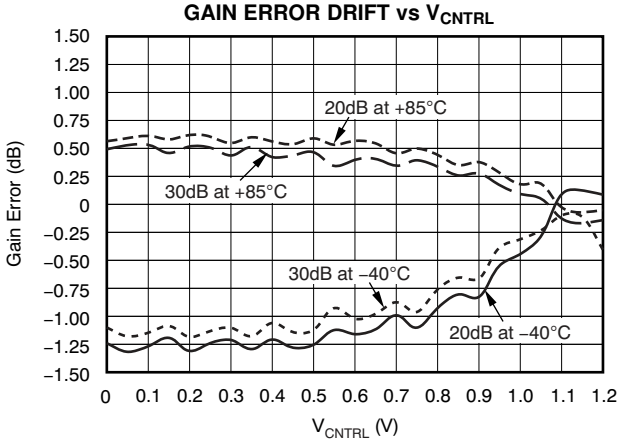


Figure 5.

GAIN vs V_{CNTRL} OVER FREQUENCY

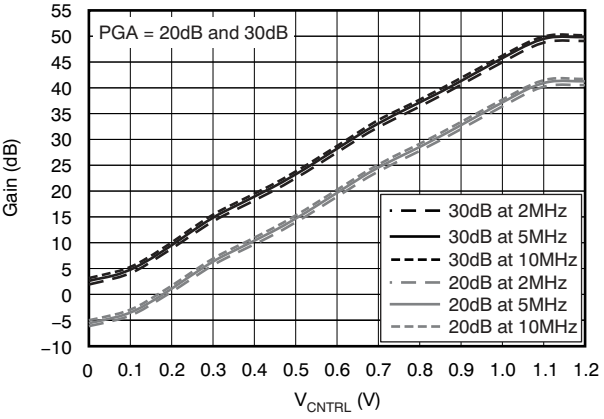


Figure 6.

GAIN MATCHING vs V_{CNTRL}

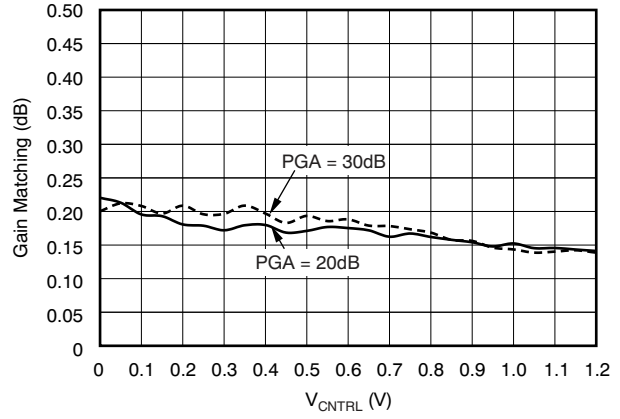


Figure 7.

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, AVDD2 = 5.0V, AVDD1 = DVDD = 3.3V; single-ended, ac-coupled (1µF) input configuration to the preamp (LNA), f_{IN} = 5MHz, V_{CNTL} = 1.0V, clamp disabled (CL = 1), LPF = 15MHz, and R_{LOAD} = 1kΩ on each output to ground, unless otherwise noted.

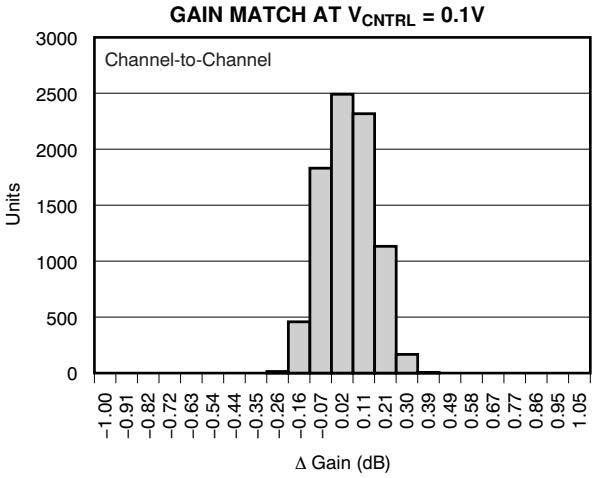


Figure 8.

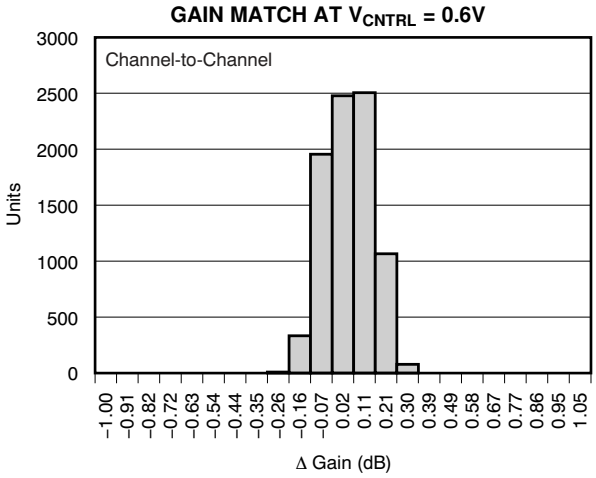


Figure 9.

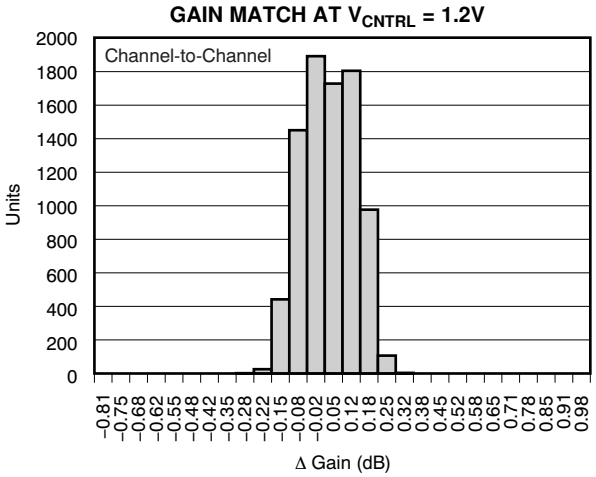


Figure 10.

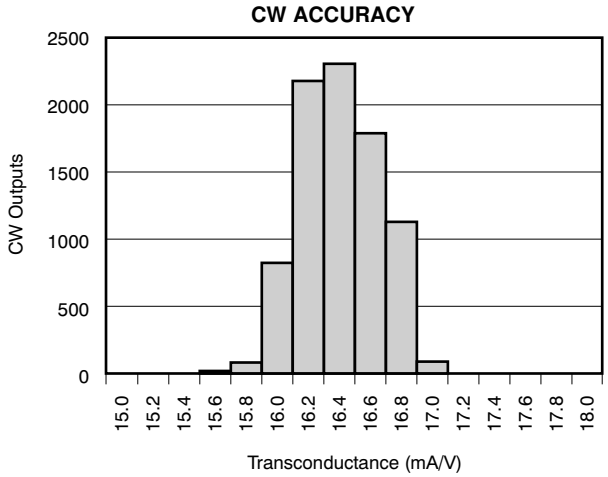


Figure 11.

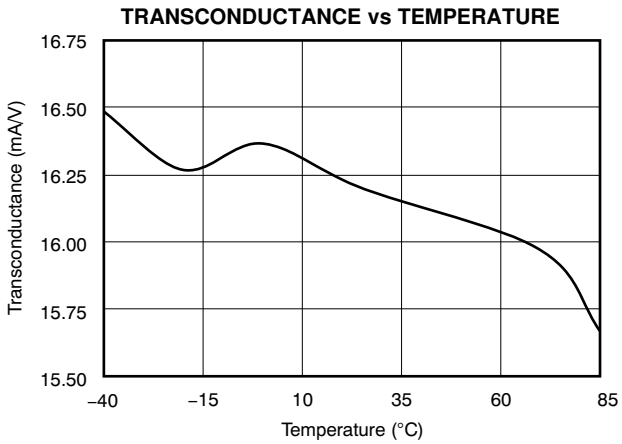


Figure 12.

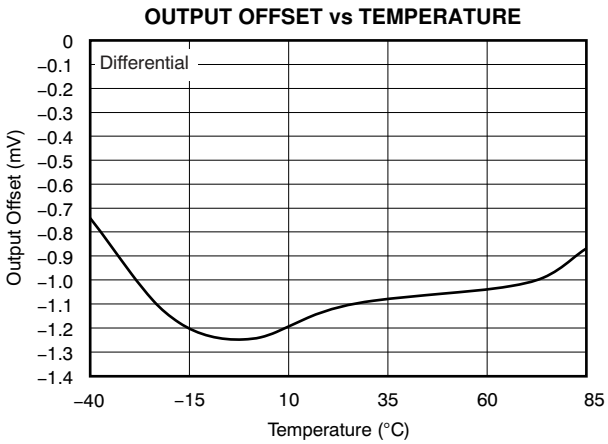


Figure 13.

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, AVDD2 = 5.0V, AVDD1 = DVDD = 3.3V; single-ended, ac-coupled (1µF) input configuration to the preamp (LNA), f_{IN} = 5MHz, V_{CNTL} = 1.0V, clamp disabled (CL = 1), LPF = 15MHz, and R_{LOAD} = 1kΩ on each output to ground, unless otherwise noted.

TGC CURRENT vs TEMPERATURE

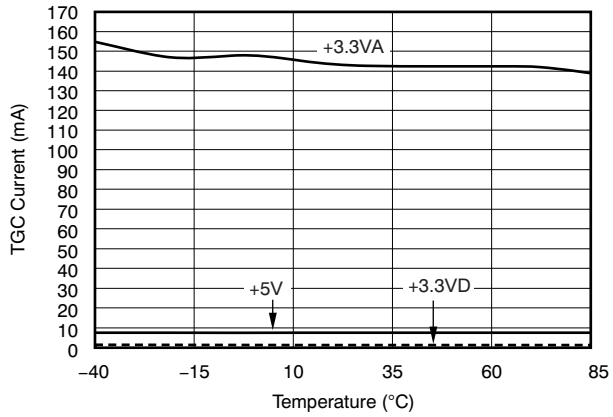


Figure 14.

CW CURRENT vs TEMPERATURE

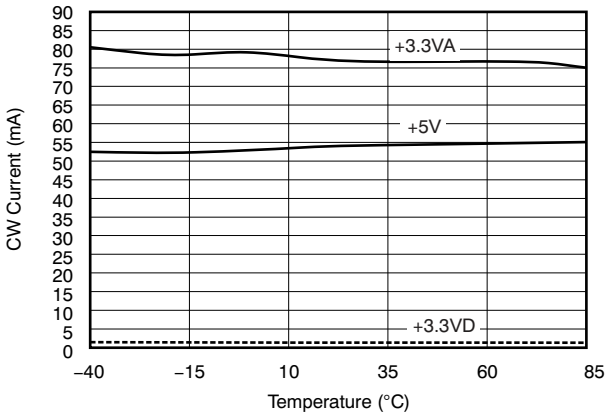


Figure 15.

TOTAL POWER vs TEMPERATURE

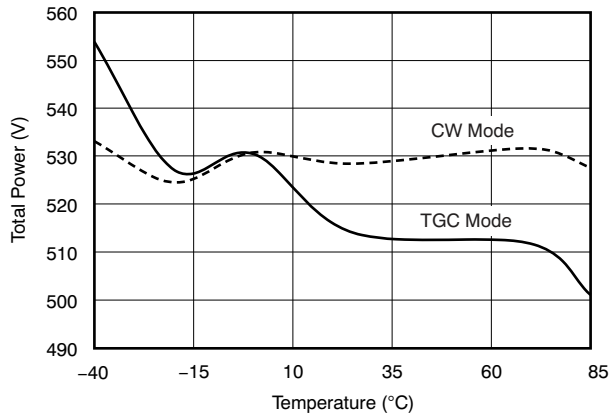


Figure 16.

FREQUENCY RESPONSE vs V_{CNTRL} AT PGA = 20dB (LPF = 15MHz and 10MHz)

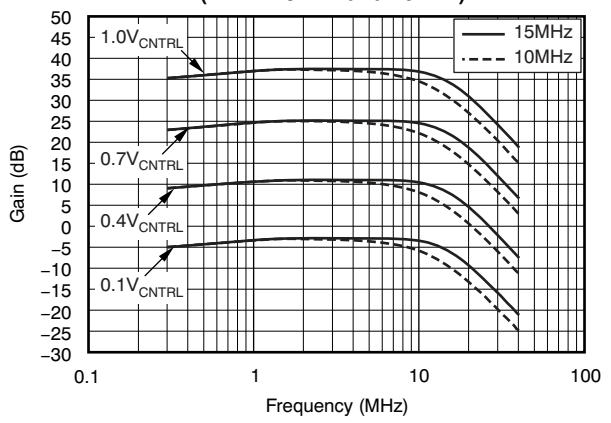


Figure 17.

FREQUENCY RESPONSE vs V_{CNTRL} AT PGA = 30dB (LPF = 15MHz and 10MHz)

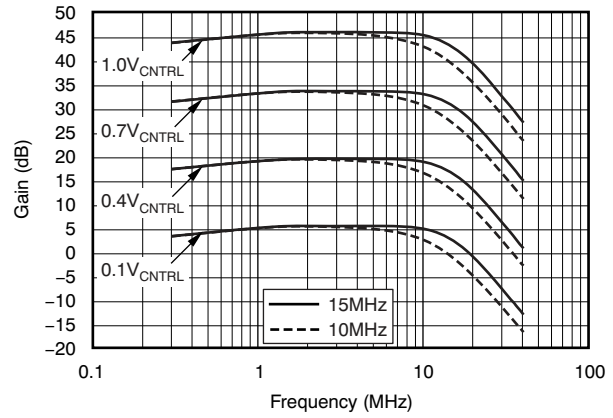


Figure 18.

OUTPUT-REFERRED NOISE vs V_{CNTRL}

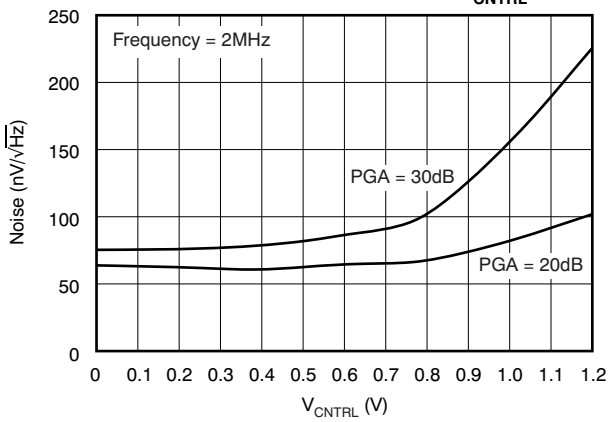


Figure 19.

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, AVDD2 = 5.0V, AVDD1 = DVDD = 3.3V; single-ended, ac-coupled (1µF) input configuration to the preamp (LNA), f_{IN} = 5MHz, V_{CNTL} = 1.0V, clamp disabled (CL = 1), LPF = 15MHz, and R_{LOAD} = 1kΩ on each output to ground, unless otherwise noted.

OUTPUT-REFERRED NOISE vs V_{CNTRL}

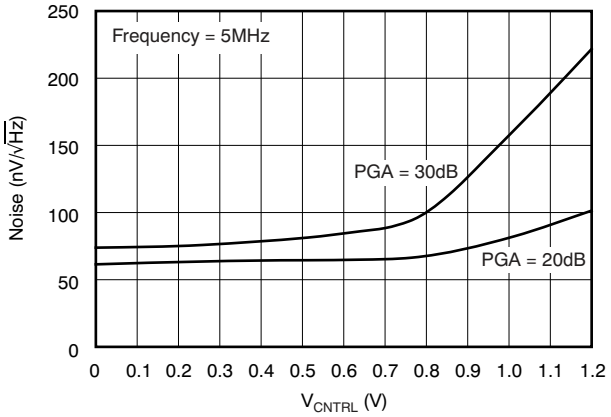


Figure 20.

INPUT-REFERRED NOISE vs V_{CNTRL}

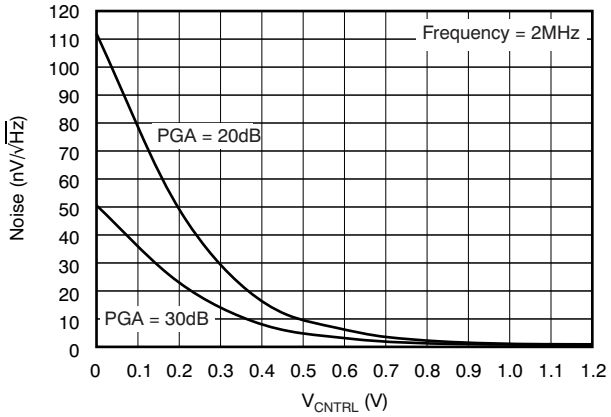


Figure 21.

INPUT-REFERRED NOISE vs V_{CNTRL}

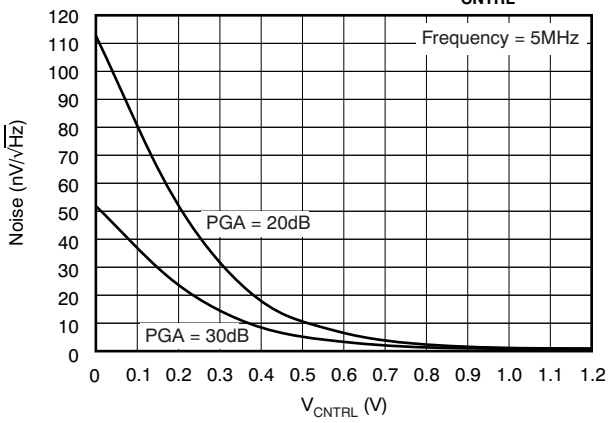


Figure 22.

CURRENT NOISE vs FREQUENCY OVER R_{SOURCE}

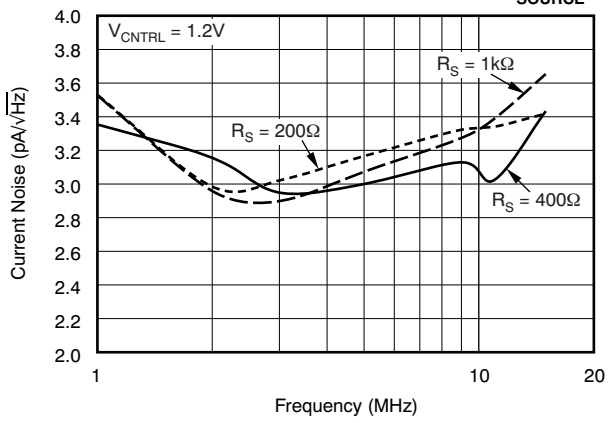


Figure 23.

OUTPUT-REFERRED NOISE vs FREQUENCY OVER R_S

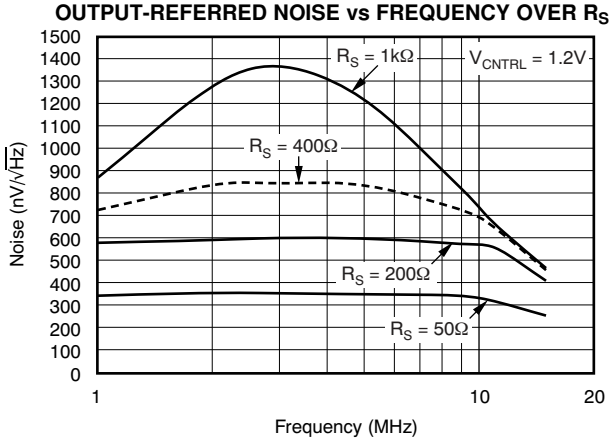


Figure 24.

INPUT-REFERRED NOISE vs FREQUENCY OVER R_S

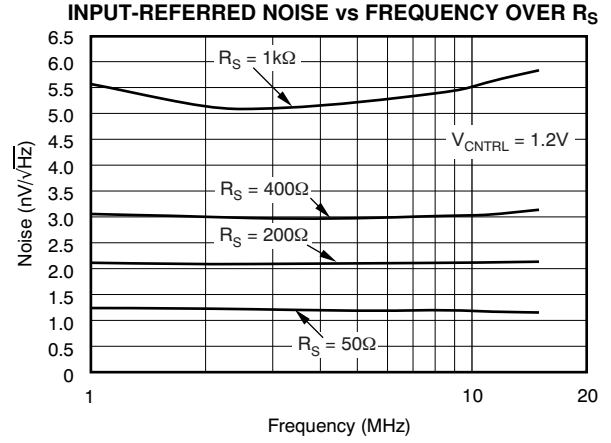


Figure 25.

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, AVDD2 = 5.0V, AVDD1 = DVDD = 3.3V; single-ended, ac-coupled (1µF) input configuration to the preamp (LNA), f_{IN} = 5MHz, V_{CNTL} = 1.0V, clamp disabled (CL = 1), LPF = 15MHz, and R_{LOAD} = 1kΩ on each output to ground, unless otherwise noted.

NOISE FIGURE vs FREQUENCY OVER R_S

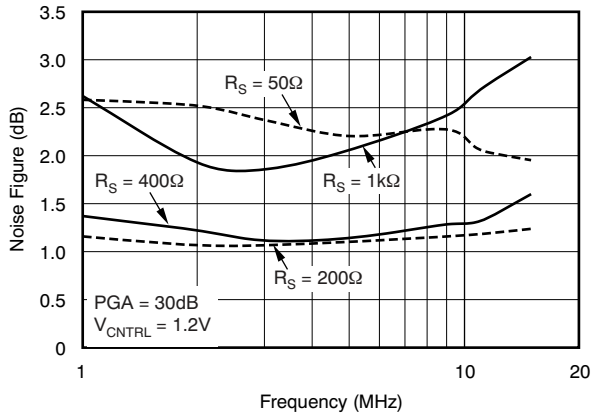


Figure 26.

INPUT-REFERRED NOISE

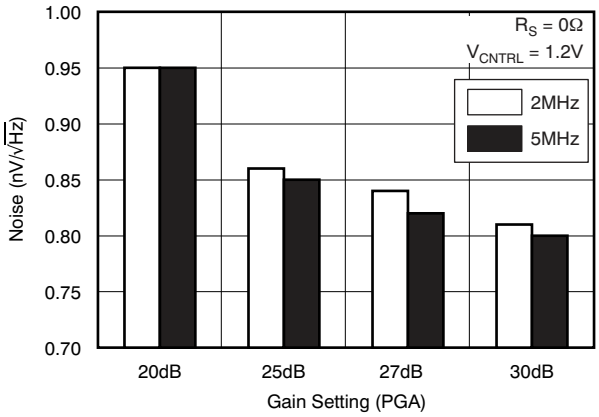


Figure 27.

INPUT-REFERRED NOISE vs FREQUENCY

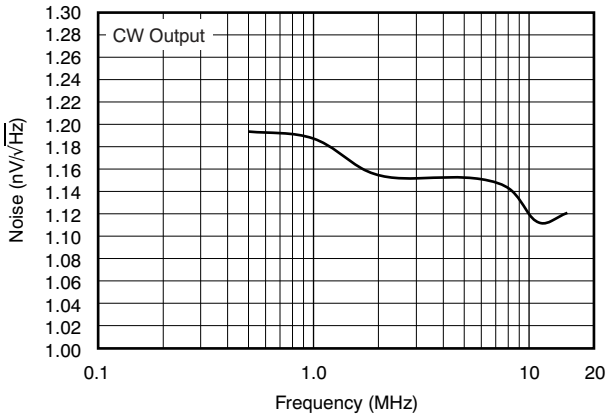


Figure 28.

MAGNITUDE AND PHASE vs FREQUENCY

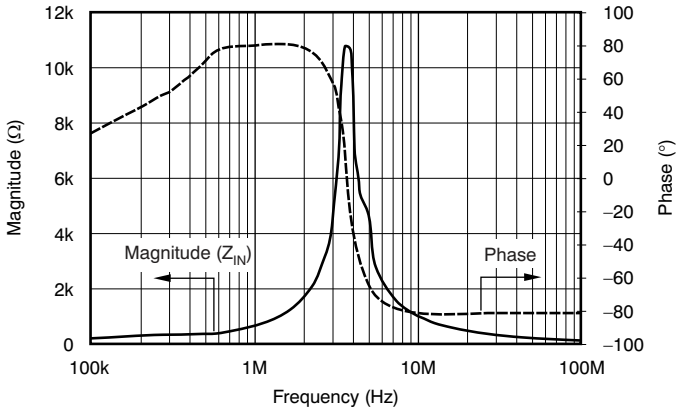


Figure 29.

2ND HARMONIC vs FREQUENCY

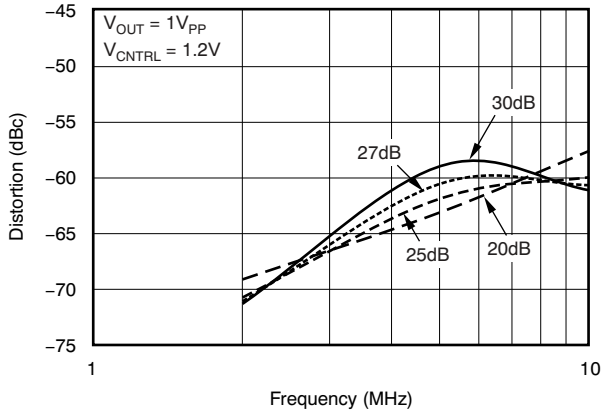


Figure 30.

3RD HARMONIC vs FREQUENCY

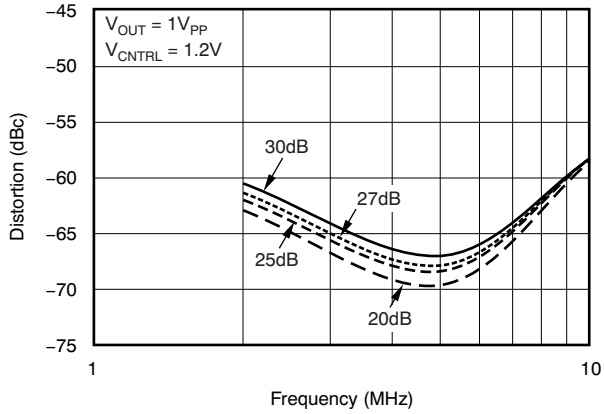


Figure 31.

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, AVDD2 = 5.0V, AVDD1 = DVDD = 3.3V; single-ended, ac-coupled (1μF) input configuration to the preamp (LNA), f_{IN} = 5MHz, V_{CNTL} = 1.0V, clamp disabled (CL = 1), LPF = 15MHz, and R_{LOAD} = 1kΩ on each output to ground, unless otherwise noted.

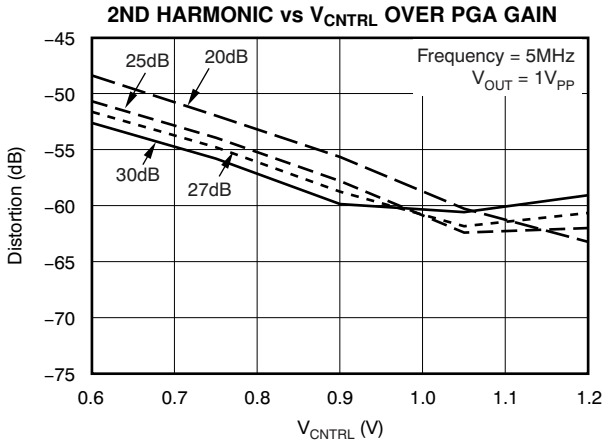


Figure 32.

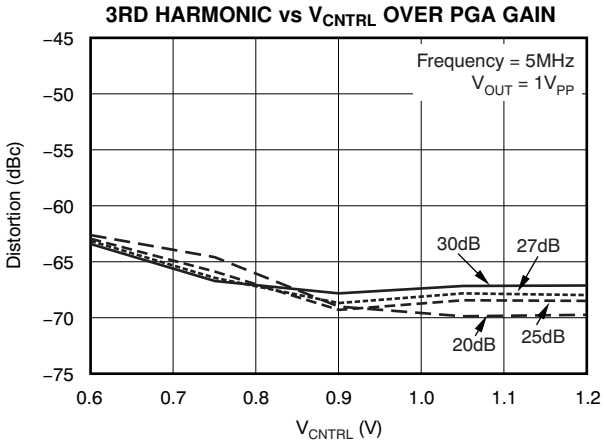


Figure 33.

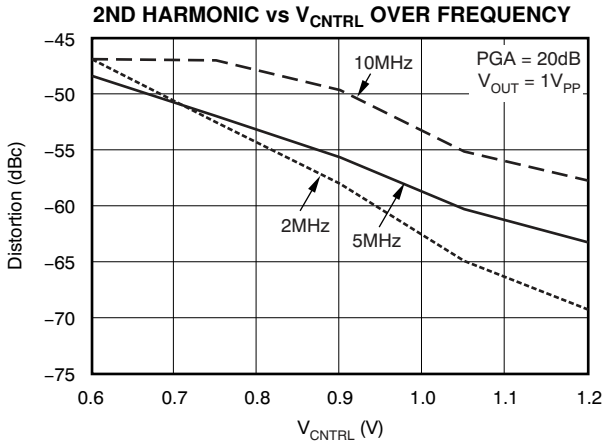


Figure 34.

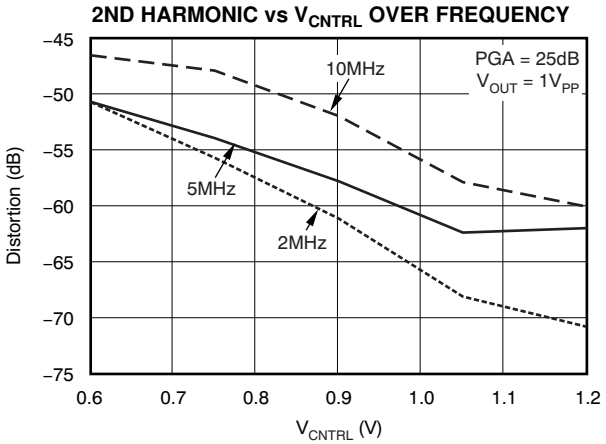


Figure 35.

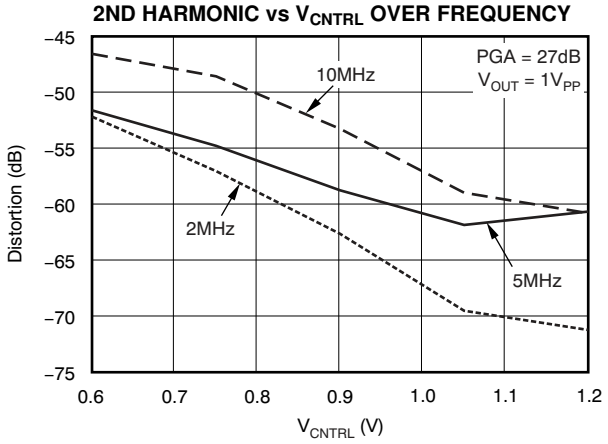


Figure 36.

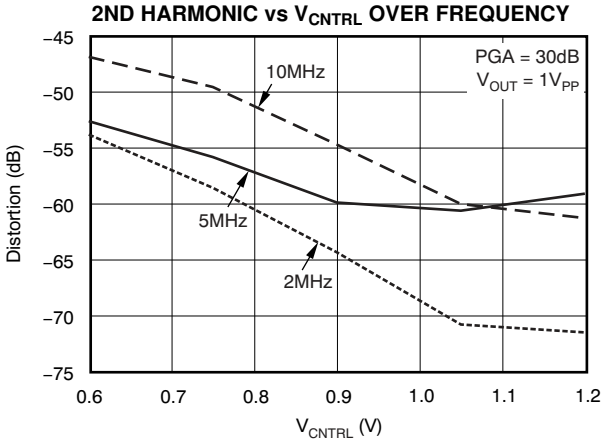


Figure 37.

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, AVDD2 = 5.0V, AVDD1 = DVDD = 3.3V; single-ended, ac-coupled (1µF) input configuration to the preamp (LNA), f_{IN} = 5MHz, V_{CNTL} = 1.0V, clamp disabled (CL = 1), LPF = 15MHz, and R_{LOAD} = 1kΩ on each output to ground, unless otherwise noted.

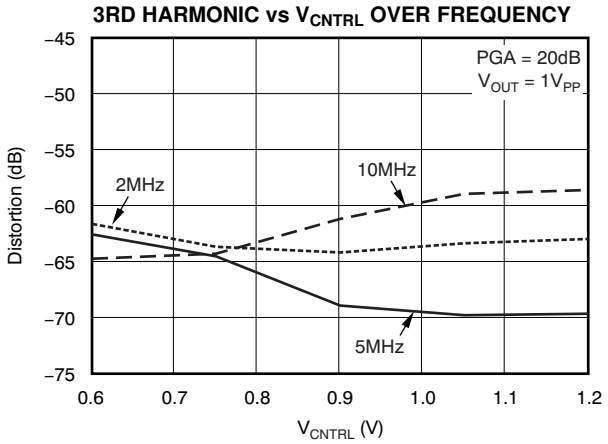


Figure 38.

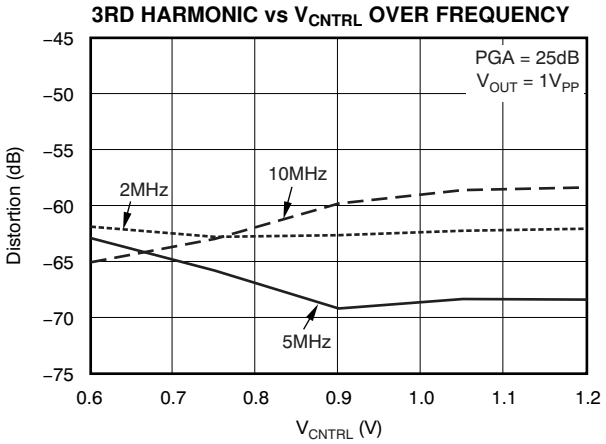


Figure 39.

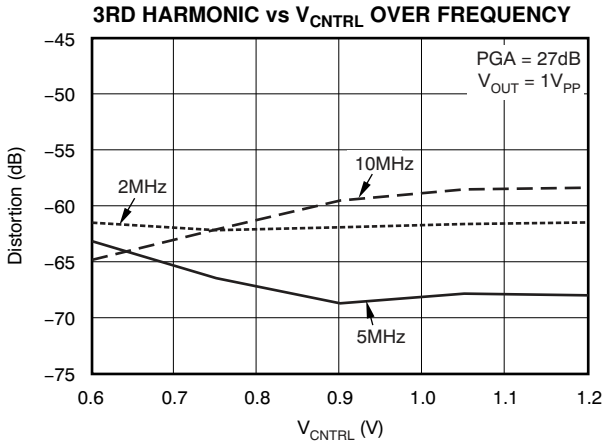


Figure 40.

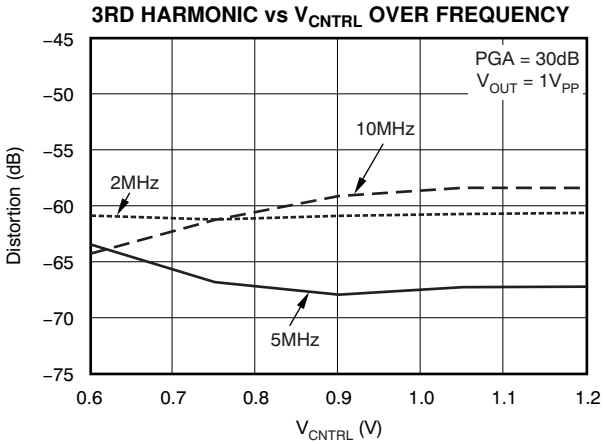


Figure 41.

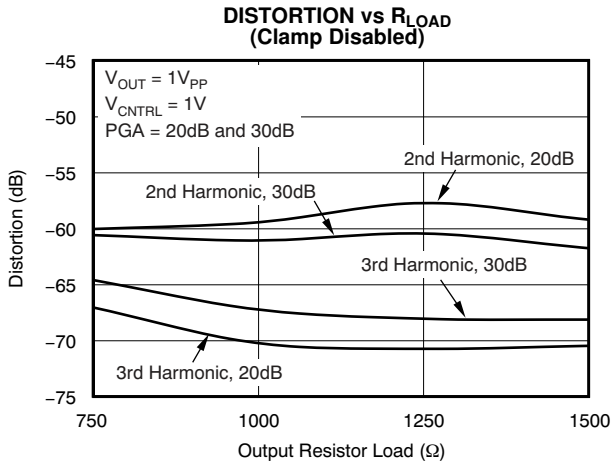


Figure 42.

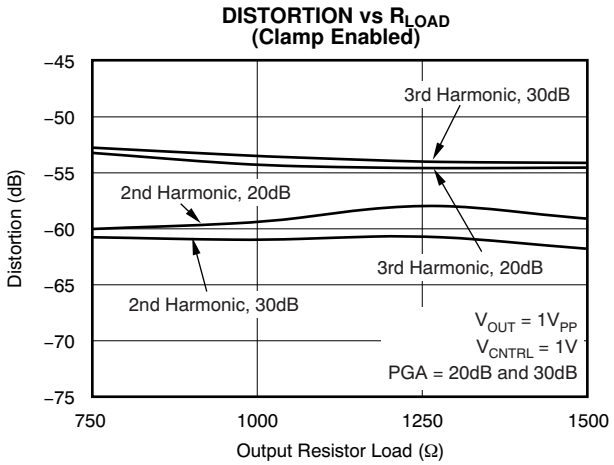


Figure 43.

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, AVDD2 = 5.0V, AVDD1 = DVDD = 3.3V; single-ended, ac-coupled (1µF) input configuration to the preamp (LNA), f_{IN} = 5MHz, V_{CNTL} = 1.0V, clamp disabled (CL = 1), LPF = 15MHz, and R_{LOAD} = 1kΩ on each output to ground, unless otherwise noted.

DISTORTION vs FREQUENCY

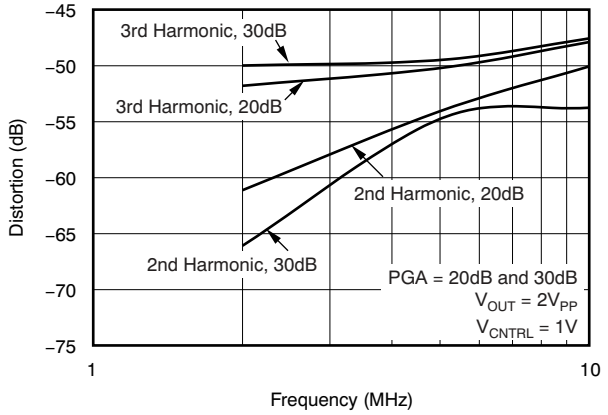


Figure 44.

DISTORTION vs PGA GAIN

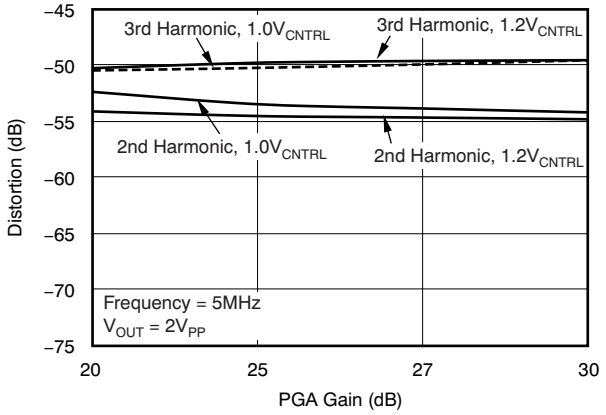


Figure 45.

DISTORTION vs V_{OUT}, PEAK-TO-PEAK

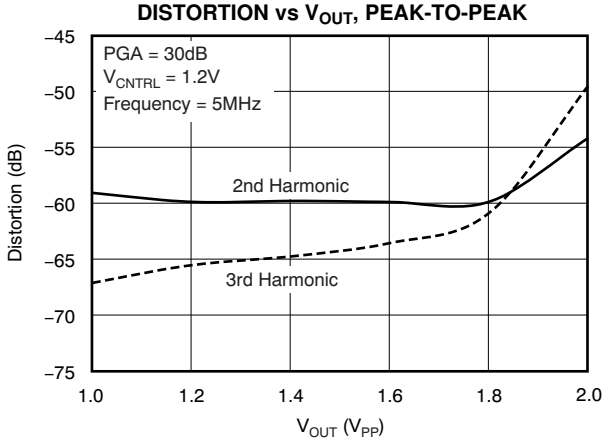


Figure 46.

INTERMODULATION DISTORTION (4.99MHz and 5.01MHz)

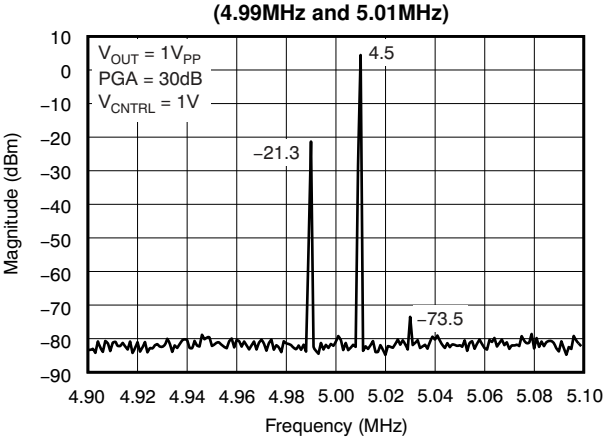


Figure 47.

CROSSTALK vs V_{CNTRL}

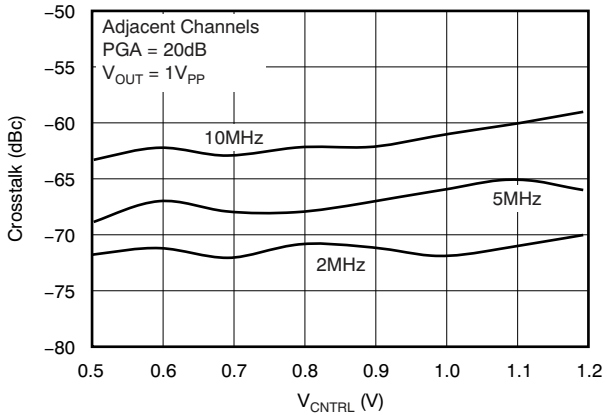


Figure 48.

CROSSTALK vs V_{CNTRL}

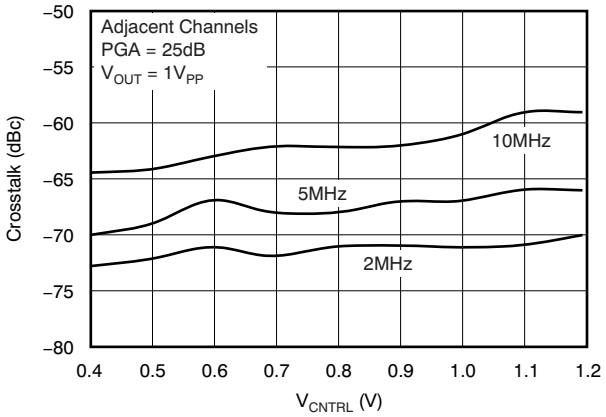


Figure 49.

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, AVDD2 = 5.0V, AVDD1 = DVDD = 3.3V; single-ended, ac-coupled (1µF) input configuration to the preamp (LNA), f_{IN} = 5MHz, V_{CNTL} = 1.0V, clamp disabled (CL = 1), LPF = 15MHz, and R_{LOAD} = 1kΩ on each output to ground, unless otherwise noted.

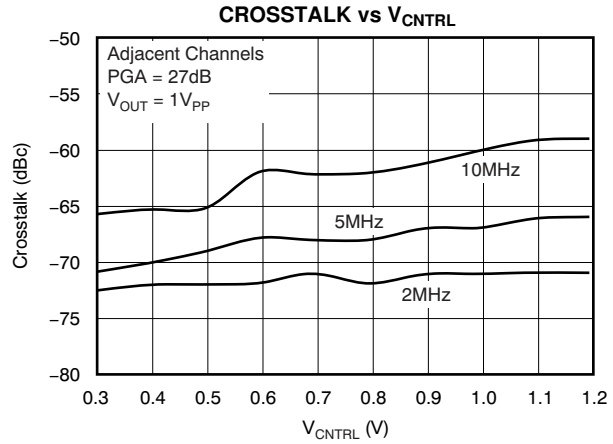


Figure 50.

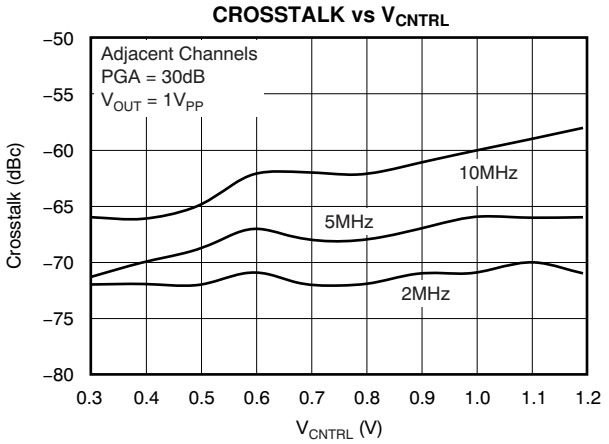


Figure 51.

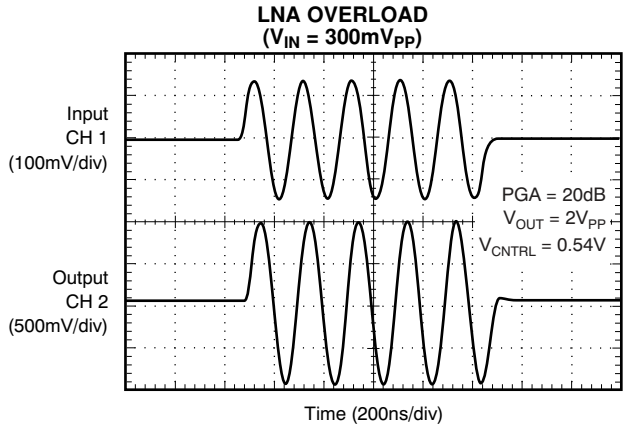


Figure 52.

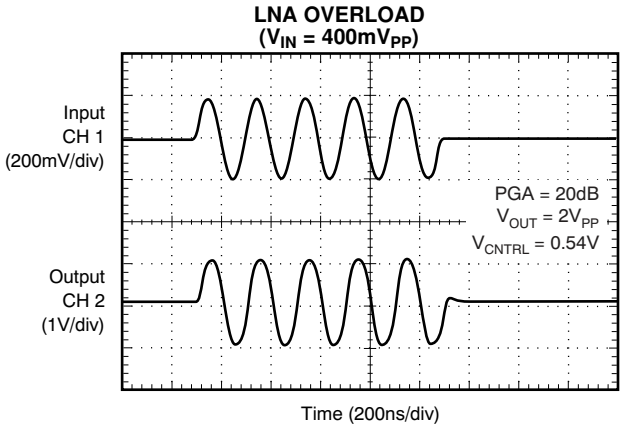


Figure 53.

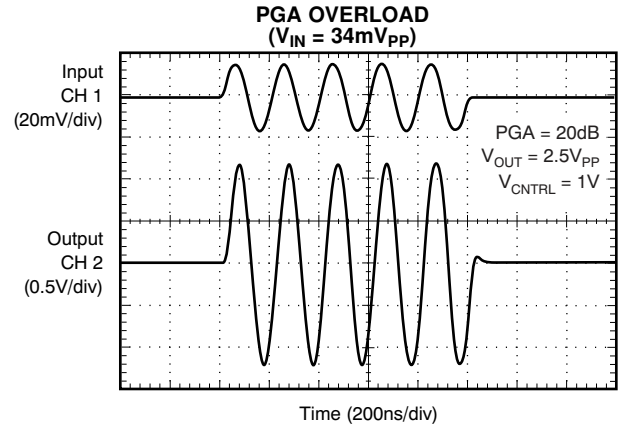


Figure 54.

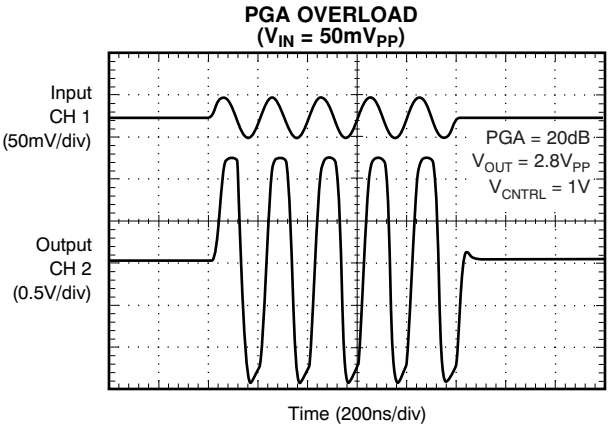


Figure 55.

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, AVDD2 = 5.0V, AVDD1 = DVDD = 3.3V; single-ended, ac-coupled (1μF) input configuration to the preamp (LNA), f_{IN} = 5MHz, V_{CNTL} = 1.0V, clamp disabled (CL = 1), LPF = 15MHz, and R_{LOAD} = 1kΩ on each output to ground, unless otherwise noted.

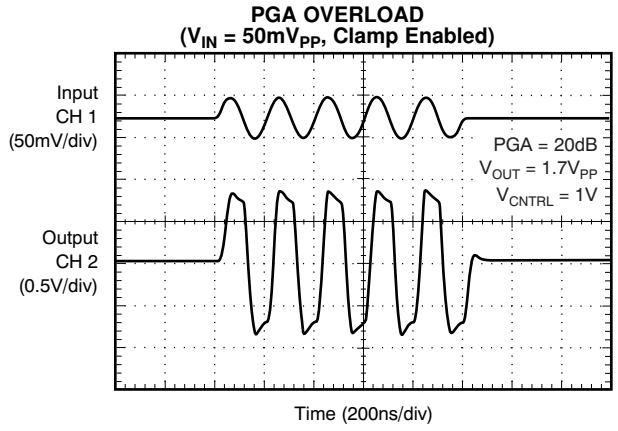


Figure 56.

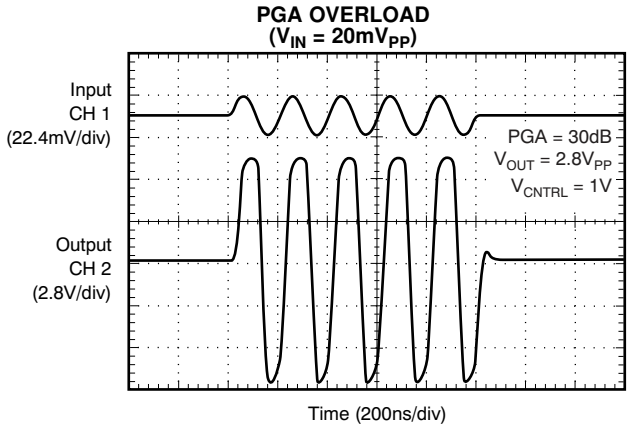


Figure 57.

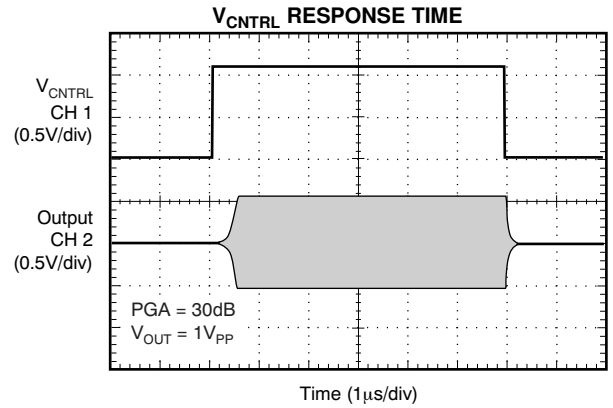


Figure 58.

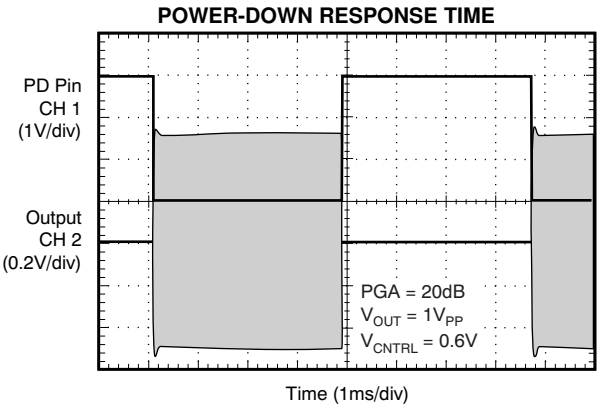


Figure 59.

THEORY OF OPERATION

Built on TI's bipolar-complementary (BiCOM) process, the VCA8500 is a third-generation, octal variable gain amplifier that implements a number of proprietary circuit design techniques to specifically address the performance demands of medical ultrasound systems.

The VCA8500 is an 8-channel VGA that is ideally suited for portable ultrasound applications. It offers unparalleled low-noise and low-power performance at a high level of integration. For the TGC signal path, each channel consists of a 20dB fixed-gain low-noise amplifier (LNA), a linear-in-dB voltage-controlled attenuator (VCA), and a programmable gain amplifier (PGA), as well as a clamping and low-pass filter stage. Digitally controlled through the logic interface, the PGA gain can be set to four different settings: 20dB, 25dB, 27dB, and 30dB. At its highest setting, the total available gain of the VCA8500 is therefore 50dB, sufficient for 10-bit systems. To facilitate the logarithmic time-gain compensation required for ultrasound systems, the VCA is designed to provide a 46dB attenuation range. Here, all channels are simultaneously controlled by an externally-applied control voltage (V_{CNTL}) in the range of 0V to 1.2V.

While the LNA is designed to be driven from a single-ended source, the internal TGC signal path is designed to be fully differential to maximize dynamic range while also optimizing for low, even-order harmonic distortion.

CW doppler signal processing is facilitated by routing the differential LNA outputs to V/I amplifier stages. The resulting signal currents of each channel then connect to an 8×10 switch matrix that is controlled through the serial interface and a corresponding register. The CW outputs are typically routed to a passive delay line that allows coherent summing (beam forming) of the active channels and additional off-chip signal processing, as shown in Figure 60.

Applications that do not utilize the CW path can simply operate the VCA8500 in TGC mode. In this mode, the CW blocks (V/I amplifiers and switch matrix) remain powered down, and the CW outputs can be unconnected.

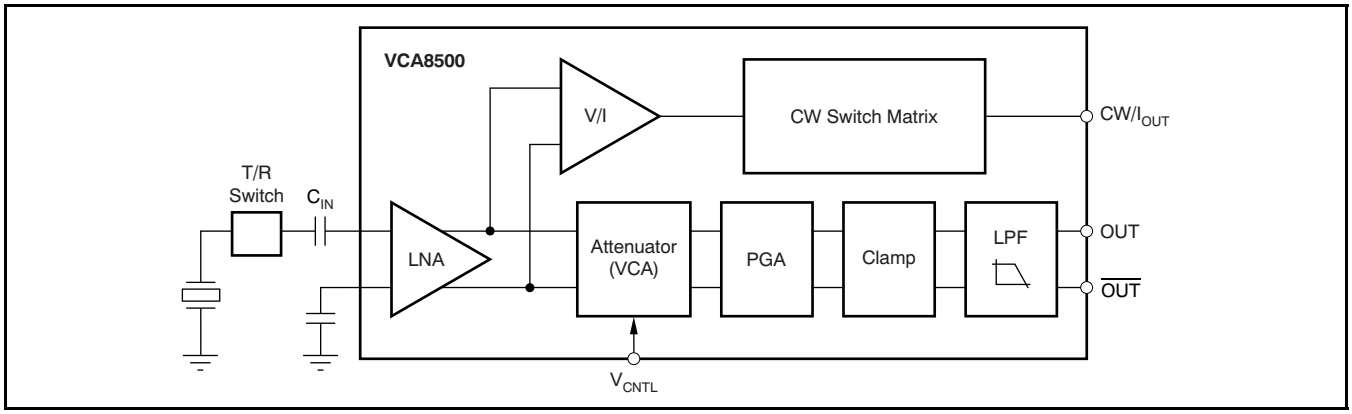


Figure 60. Functional Block Diagram

LOW-NOISE AMPLIFIER (LNA)

As with many high-gain systems, the front-end amplifier is critical to achieve a certain overall performance level. Using a proprietary new architecture, the LNA of the VCA8500 delivers exceptional low-noise performance, while operating on a very low quiescent current of only 8.3mA per channel. This current consumption is significantly lower compared to CMOS-based architectures with similar noise performances.

The LNA performs a single-ended input to differential output voltage conversion and is configured for a fixed gain of 20dB (10V/V). The ultralow input-referred noise of only 0.7nV/$\sqrt{Hz}$, along with the linear input range of 250mV_{PP}, results in a wide dynamic range that supports the high demands of PW and CW ultrasound imaging modes. Larger input signals can be accepted by the LNA, but distortion performance degrades as input signals levels increase. The LNA input is internally biased to approximately 2.4V; the signal source should be ac-coupled to the LNA input by an adequately-sized capacitor. Internally, the LNA directly drives the VCA, avoiding the typical drawbacks of ac-coupled architectures, such as slow overload recovery.

VOLTAGE-CONTROLLED ATTENUATOR (VCA)

The amplified differential signal swing that comes from the LNA is reduced by the subsequent VCA stage. The VCA is designed to have a linear-in-dB attenuation characteristic; that is, the average gain loss in dB is constant for each equal increment of the control voltage (V_{CNTL}). Figure 61 shows the simplified schematic of this VCA stage.

The attenuator is essentially a variable voltage divider that consists of the series input resistor (R_S) and eight identical shunt FETs placed in parallel and controlled by sequentially activated clipping amplifiers (A1 through A8). Each clipping amplifier can be understood as a specialized voltage comparator with a soft transfer characteristic and well-controlled output limit voltage. Reference voltages V1 through V8 are equally spaced over the 0V to 1.2V control voltage range. As the control voltage rises through the input range of each clipping amplifier, the amplifier output rises from 0V (FET completely ON) to $V_{CM} - V_T$ (FET nearly OFF), where V_{CM} is the common source voltage and V_T is the threshold voltage of the FET. As each FET approaches its off state and the control voltage continues to rise, the next clipping amplifier/FET combination takes over for the next portion of the piecewise-linear attenuation characteristic.

Thus, low control voltages have most of the FETs turned on, producing maximum signal attenuation. Similarly, high control voltages turn the FETs off, leading to minimal signal attenuation. Therefore, each FET acts to decrease the shunt resistance of the voltage divider formed by R_S and the parallel FET network.

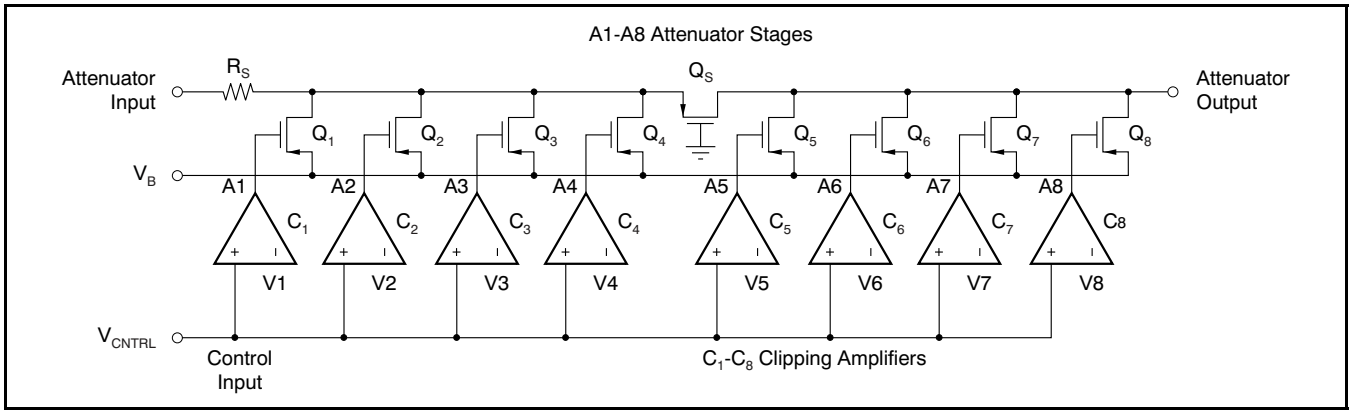


Figure 61. Voltage-Controlled Attenuator Simplified Schematic

PROGRAMMABLE POST-GAIN AMPLIFIER (PGA)

Following the VCA is a programmable post-gain amplifier (PGA). Figure 62 shows a simplified schematic of the PGA, including the clamping stage. The gain of this PGA can be configured to four different gain settings: 20dB, 25dB, 27dB, and 30dB, programmable through the serial port; see Table 8.

The PGA structure consists of a differential, programmable-gain voltage-to-current converter stage followed by transimpedance amplifiers to create and buffer each side of the differential output. Low input noise is also a requirement for the PGA design as a result of the large amount of signal attenuation that can be applied in the preceding VCA stage. At minimum VCA attenuation (used for small input signals), the LNA noise dominates; at maximum VCA attenuation (large input signals), the attenuator and PGA noise dominates.

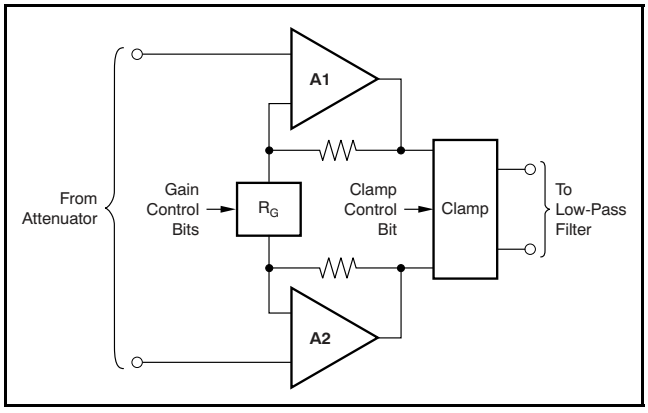


Figure 62. Post-Gain Amplifier (Simplified Schematic)

PROGRAMMABLE CLAMPING

To further optimize the overload recovery behavior of a complete TGC channel, the VCA8500 integrates a programmable clamping stage, as shown in Figure 63. This clamping stage precedes the low-pass filter in order to prevent the filter circuit from being driven into overload, the result of which would be an extended recovery time. Programmable through the serial interface, the clamping level can be either set to clamp the output to approximately $1.7V_{PP}$ differential, or be disabled. Disabling the clamp function increases the current consumption on the 3.3V analog supply (AVDD1) by about 3mA for the full device. Note that with the clamp function enabled, the third-harmonic distortion increases.

LOW-PASS FILTER

As part of a typical data acquisition system, the signal bandwidth generally must be limited by the use of an anti-aliasing filter before the analog-to-digital converter (ADC). The VCA8500 integrates such an anti-aliasing filter in the form of a programmable low-pass filter (LPF) for each channel. The LPF is designed as a differential, active, second-order filter that approximates a Butterworth characteristic, with typically 12dB per octave roll-off. Figure 63 shows the simplified schematic of half the differential active low-pass filter. Programmable through the serial interface, the –3dB frequency corner can be set to either 10MHz or 15MHz. The filter is set for all channels simultaneously.

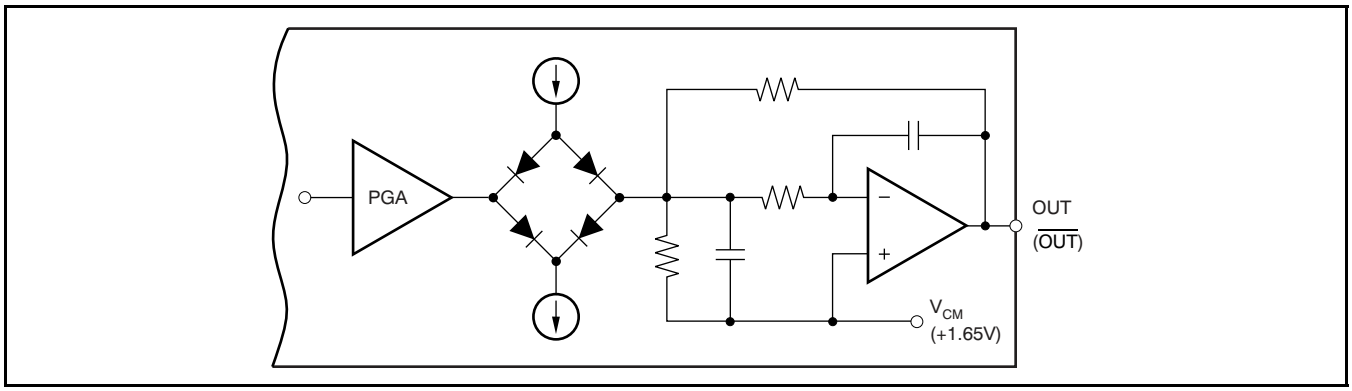


Figure 63. Clamping Stage and Low-Pass Filter (Simplified Schematic)

APPLICATION INFORMATION

ANALOG INPUT AND LNA

While the LNA is designed as a fully differential amplifier, it is optimized to perform a single-ended input to differential output conversion. A simplified schematic of an LNA channel is shown in Figure 64. A bias voltage (V_B) of +2.4V is internally applied to the LNA inputs through 8kΩ resistors. In addition, the dedicated signal input (IN pin) includes a pair of back-to-back diodes that provide a coarse input clamping function in case the input signal rises to very large levels, exceeding $0.7V_{PP}$. This configuration prevents the LNA from being driven into a severe overload state, which may otherwise cause an extended overload recovery time. The integrated diodes are designed to handle a dc current of up to approximately 5mA. Depending on the application requirements, the system overload characteristics may be improved by adding external Schottky diodes at the LNA input, as shown in Figure 64.

As Figure 64 also shows, the complementary LNA input (V_{BL} pin) is internally decoupled by a small capacitor. Furthermore, for each input channel, a separate V_{BL} pin is brought out for external bypassing. This bypassing should be done with a small, 0.1µF (typical) ceramic capacitor placed in close proximity to each V_{BL} pin. Attention should be given to provide a low-noise analog ground for this bypass capacitor. A noisy ground potential may cause noise to be picked up and injected into the signal path, leading to higher noise levels.

The LNA closed-loop architecture is internally compensated for maximum stability without the need of external compensation components (inductors or capacitors). At the same time, the total input capacitance is kept to a minimum with only 30pF. This architecture minimizes any loading of the signal source that may otherwise lead to a frequency-dependent voltage divider. Moreover, the closed-loop design yields very low offsets and offset drift; this consideration is important because the LNA directly drives the subsequent voltage-controlled attenuator.

The LNA of the VCA8500 uses the benefits of a bipolar process technology to achieve an exceptionally low-noise voltage of $0.7nV/\sqrt{Hz}$, and a low current noise of only $3pA/\sqrt{Hz}$. With these input-referred noise specifications, the VCA8500 achieves very low noise figure numbers over a wide range of source resistances and frequencies (see Figure 26 in the Typical Characteristics). The optimal noise power matching is achieved for source impedances of around 200Ω.

Further details of the VCA8500 input and output noise performance are shown in the Typical Characteristic graphs; the input-referred noise voltage is derived by dividing the output-referred noise by the measured gain at each point along the gain control range.

Noise Figure versus Source Resistance (R_S)

R_S (Ω)	NOISE FIGURE (dB)
50	2.21
200	1.10
400	1.14
1000	2.06

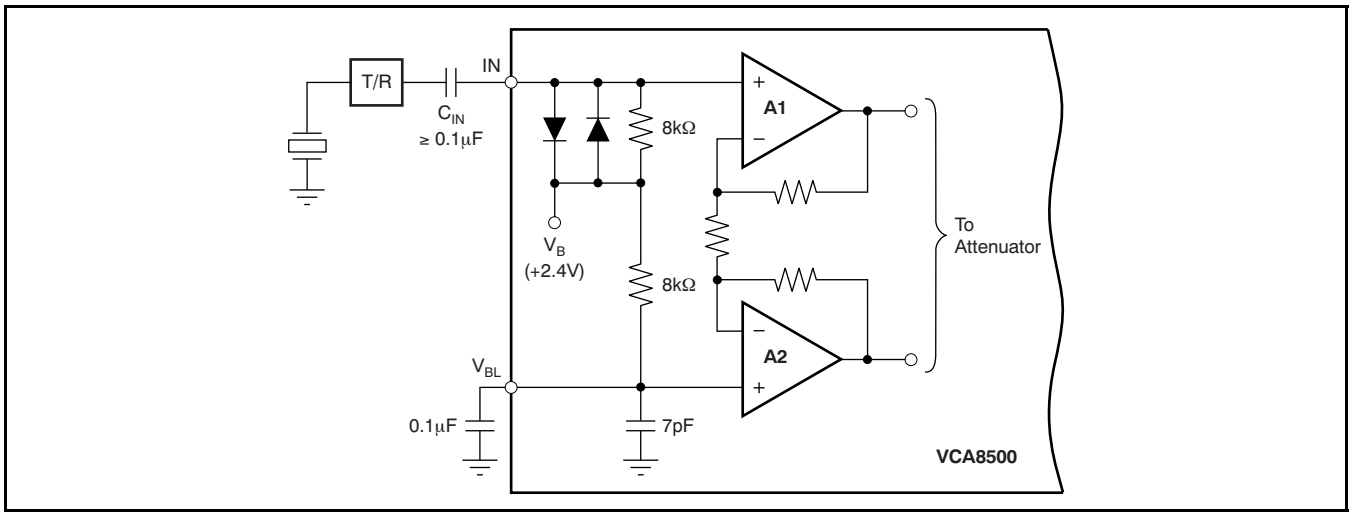


Figure 64. LNA Channel (Simplified Schematic)

OVERLOAD RECOVERY

The VCA8500 is designed in particular for ultrasound applications where the front-end device is required to recover very quickly from an overload condition. Such an overload can either be the result of a transmit pulse feed-through or a strong echo, which can cause overload of the LNA, the PGA, or both. As discussed earlier, the LNA inputs are internally protected by a pair of back-to-back diodes to prevent severe overload of the LNA. Figure 65 illustrates an ultrasound receive channel front-end that includes typical external overload protection elements. Here, four high-voltage switching diodes are configured in a bridge configuration and form the transmit/receive (T/R) switch. During the transmit period, high voltage pulses from the pulser are applied to the transducer elements and the T/R switch isolates the sensitive LNA input from being damaged by the high voltage signal. However, it is common that fast transients up to several volts leak through the T/R switch and potentially overload the receiver. Therefore, an additional pair of clamping diodes is placed between the T/R switch and the LNA input. In order to clamp the over-voltage to small levels, Schottky diodes (such as the BAS40 series by Infineon®) are commonly used. For example, clamping to levels of ±0.3V can significantly reduce the overall overload recovery performance. The T/R switch characteristics are largely determined by the biasing current of the diodes, which can be set by adjusting the 3kΩ resistor values; for example, setting a higher current level may lead to an improved switching characteristic and reduced noise contribution. A typical front-end protection circuitry may add in the order of $2nV/\sqrt{Hz}$ of noise to the signal path. This slight increase also depends on the value of the termination resistor (R_T).

As Figure 65 shows, the front-end circuitry should be capacitively coupled to the LNA signal input (IN). This coupling ensures that the LNA input bias voltage of +2.4V is maintained and decoupled from any other biasing voltage before the LNA.

Within the VCA8500, overload can occur in either the LNA or the PGA. LNA overload can occur as the result of T/R switch feed-through; and the PGA can be driven into an overload condition by a strong echo in the near-field while the signal gain is high. In any case, the VCA8500 is optimized for very short recovery times, as shown in Figure 65.

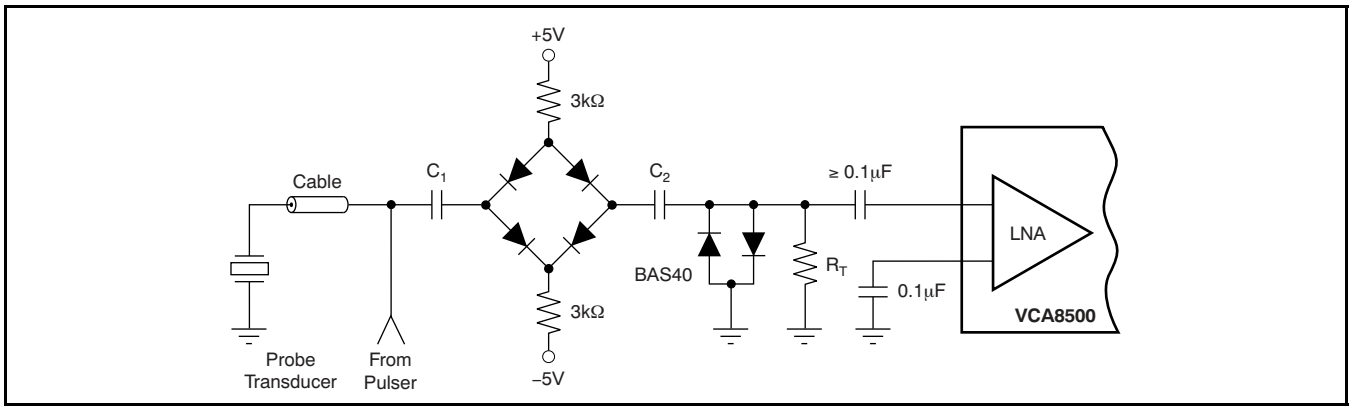


Figure 65. Typical Input Overload Protection Circuit of an Ultrasound System

VCA—GAIN CONTROL

The attenuator (VCA) for each of the eight channels of the VCA8500 is controlled by a single-ended control signal input, the V_{CNTRL} pin. The control voltage range spans from 0V to 1.2V, referenced to ground. This control voltage varies the attenuation of the VCA based on its linear-in-dB characteristic with its maximum attenuation (minimum gain) at V_{CNTRL} = 0V, and minimum attenuation (maximum gain) at V_{CNTRL} = 1.2V. Table 12 shows the nominal gains for each of the four PGA gain settings. The total gain range is typically 46dB and remains constant independent of the PGA selected; the *Max Gain* column reflects the absolute gain of the full signal path comprised of the fixed LNA gain of 20dB and the programmable PGA gain.

Table 12. Nominal Gain Control Ranges for Each of the Four PGA Gain Settings

PGA GAIN	MIN GAIN AT V_{CNTRL} = 0V	MAX GAIN AT V_{CNTRL} = 1.2V
20dB	–4.5dB	41.5dB
25dB	–0.5dB	45.5dB
27dB	1.5dB	47.5dB
30dB	3.5dB	49.5dB

As previously discussed, the VCA architecture uses eight attenuator segments that are equally spaced in order to approximate the linear-in-dB gain-control slope. This approximation results in a monotonic slope; gain ripple is typically less than ±0.5dB.

The VCA8500 gain-control input has a –3dB bandwidth of approximately 1.5MHz. This wide bandwidth, although useful in many applications, can allow high-frequency noise to modulate the gain control input. In practice, this modulation can easily be avoided by additional external filtering (R_F and C_F) of the control input, as Figure 66 shows. Stepping the control voltage from 0V to 1.2V, the gain control response time is typically less than 500ns to settle within 10% of the final signal level of a $1V_{PP}$ output.

The control voltage input (V_{CNTRL} pin) represents a high-impedance input. Multiple VCA8500 devices can be connected in parallel with no significant loading effects using the V_{CNTRL} pin of each device. Note that when the V_{CNTRL} pin is left unconnected, it floats up to a potential of about +3.7V. For any voltage level above 1.2V and up to 5.0V, the VCA continues to operate at its minimum attenuation level; however, it is recommended to limit the voltage to approximately 1.5V or less.

When the VCA8500 operates in CW mode, the attenuator stage remains connected to the LNA outputs. Therefore, it is recommended to set the V_{CNTRL} voltage to +1.2V in order to minimize the internal loading of the LNA outputs. Small improvements in reduced power dissipation and improved distortion performance may also be realized.

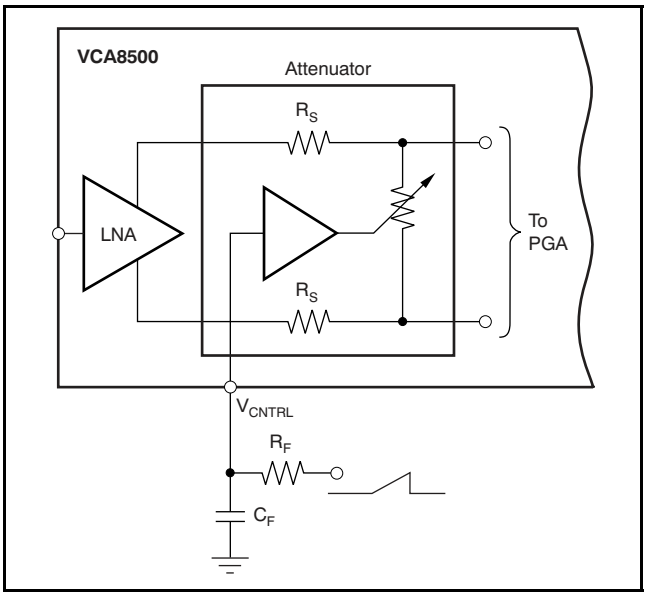


Figure 66. External Filtering of the V_{CNTL} Input

OUTPUT

The output stage of the VCA8500 delivers a differential output signal that swings symmetrically around a fixed common-mode output voltage of +1.65V. The design of the output stage includes a common-mode control loop to hold the output common-mode voltage stable over a wide range of operating conditions. At the same time the output offset and drift are kept to a minimum, allowing the VCA8500 to be dc-coupled directly to other devices (such as an ADC). In cases where the output of the VCA8500 drives devices with a non-matching input common-mode level, small ac-coupling capacitors (for instance, 0.1µF) should be used.

It should be noted, however, that unlike many other high-speed operational amplifiers, the VCA8500 is designed to drive a typical output load of 1kΩ single-ended (from each output to ground) or 2kΩ differentially. For most applications, this consideration should not represent a limitation; many high-speed ADCs have input impedances in the kΩ range. For the VCA8500 to maintain the ability to provide the full $2V_{PP}$ output swing, however, it is recommended to keep the output loading to 800Ω, single-ended (1.6kΩ differential), or higher. In addition, care should be taken to keep the capacitive loading of the outputs to

a minimum (C_{LOAD} ≤ 18pF, differential). The user should examine all factors that contribute to the total load (R_{LTOTAL} = R_L + X_L). Depending on the overall system requirements, trade-offs can be made between the output loading and the desired distortion levels and output swing.

INTERFACING TO ADCs

The VCA8500 is ideally suited to drive the ADS5281, a low-power, octal, 12-bit ADC that can be operated at sampling rates of up to 50MSPS. The VCA outputs can be directly connected the ADC inputs without the need for any external components, as shown in Figure 67. Observing proper layout considerations, the two devices can be placed in close proximity to each other and allow for a very compact printed circuit board (PCB) layout.

The ADS5281 features many performance characteristics that make it an excellent choice for ultrasound systems: low channel power of only 55mW/ch (at 40MSPS); high signal-to-noise ratio of 70dB; and fast overload recovery time of only one clock cycle. The VCA8500 can be configured to complement this level of performance by choosing the most suitable amplification setting of the post-gain amplifier. For example, the ADS5281 has a full-scale input of $2V_{PP}$ and an input-referred noise of approximately 50nV/√Hz. In order to achieve the highest combined dynamic range performance, the PGA gain can be set to 20dB. With this gain setting, the output-referred noise is dominated by the noise contribution of the attenuator and PGA and remains constant over most of the gain control range (approximately 65nV/√Hz). Only at the high end of the gain control range does the LNA and source-related noise contribution become the prevailing factor. Higher gain PGA settings may be chosen to interface to lower resolution ADCs that have a higher noise floor.

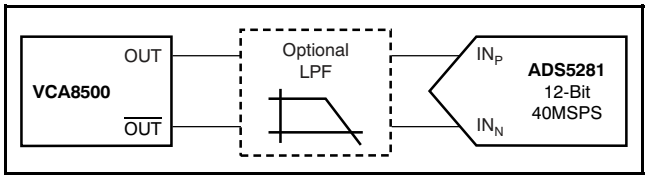


Figure 67. The VCA8500 Can Be Interfaced to the ADS5281 Without the Need for External Components

Figure 68 shows the normalized frequency response of the low-pass filter. The 15MHz bandwidth is intended to be the upper bandwidth for a system that uses sampling rates of up to 40MSPS. Here, the ratio of the bandwidth (BW) to the Nyquist frequency (f_S/2) is approximately 0.75, which provides a good compromise between the passband area and the stop band attenuation. Choosing the lower 10MHz bandwidth setting may be considered if the sampling rate is reduced further, or if the input signal bandwidth is lower. In this case, the reduced noise bandwidth can potentially improve the noise floor.

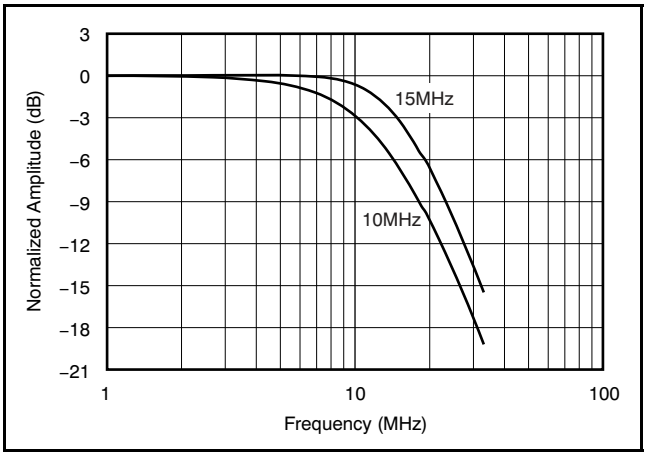


Figure 68. Normalized Frequency Response of the 10MHz and 15MHz Low-Pass Filter

CW DOPPLER PROCESSING

The VCA8500 integrates many of the elements necessary to allow for the implementation of a CW doppler processing circuit, such as a V/I converter for each channel and a cross-point switch matrix with an 8-input into 10-output (8×10) configuration.

In order to switch the VCA8500 from the default TGC mode operation into CW mode, bit D5 of the control register must be updated to low ('0'). This setting also enables access to all other registers that determine the switch matrix configuration (see the Input Register Bit Map tables). In order to process CW signals, the LNA internally feeds into a differential V/I amplifier stage. The transconductance of the V/I amplifier is typically 16.4mA/V with a $100mV_{PP}$ input signal. For proper operation, the CW outputs must be connected to an external bias voltage of +2.5V. Each CW output is designed to sink a small dc current of 0.9mA, and can deliver a signal current up to $2.9mA_{PP}$.

The resulting signal current then passes through the 8×10 switch matrix. Depending on the programmed configuration of the switch matrix, any V/I amplifier current output can be connected to any of 10 CW outputs. This design is a simple current-summing circuit such that each CW output can represent the sum of any or all of the channel currents. The CW outputs are typically routed to a passive LC delay line, allowing coherent summing of the signals.

After summing, the CW signal path further consists of a high dynamic range mixer for down-conversion to I/Q base-band signals. The I/Q signals are then band-limited (that is, low-frequency contents are removed) in a filter stage that precedes a pair of high-resolution, low sample rate ADCs.

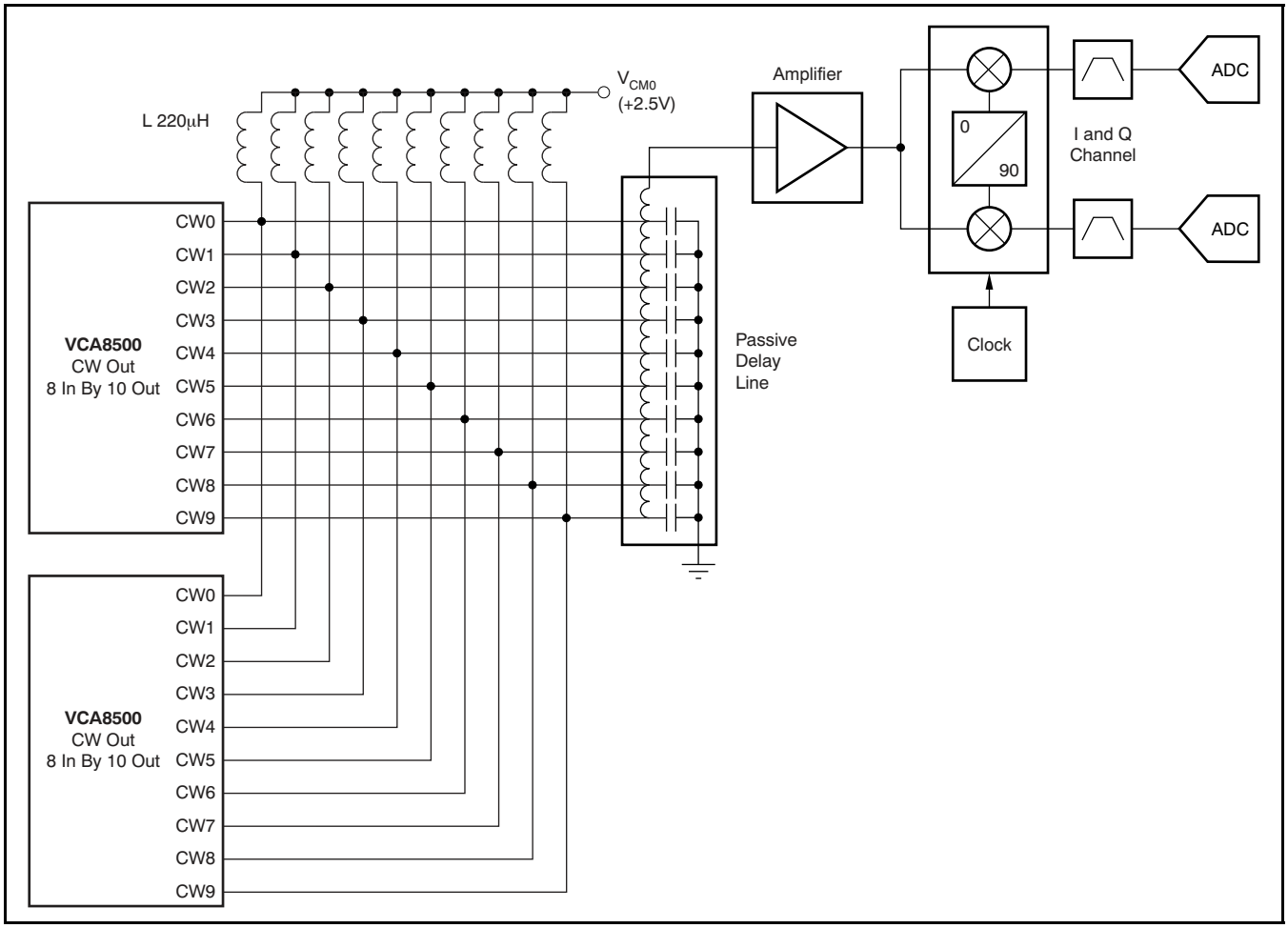


Figure 69. Conceptual CW Doppler Signal Path Using Current Summing and a Passive Delay Line for Beamforming

POWER SUPPLIES

The VCA8500 operates on two supply rails, a +3.3V and a +5V supply. At initial power-up, the part operates in the TGC mode, with the registers in the default configurations (see Table 2).

In TGC mode, only the VCA (attenuator) draws a small current (typically 1.5mA) from the +5V supply. Switching into the CW mode, the internal V/I amplifiers are then powered from the +5V rails as well, raising the operating current on the +5V rail. At the same time, the post-gain amplifiers (PGA) are powered down, reducing the current consumption on the +3.3V rail (refer to the Electrical Characteristics table for details).

All supply rails for the VCA8500 should be clean, low-noise, analog supplies. This consideration includes the +3.3V digital supply DVDD (pin 59) that connects to the internal logic blocks of the VCA8500. It is recommended to tie the DVDD pin to the same +3.3V analog supply as the AVDD1 pins, rather than a different +3.3V rail that may also power other logic devices in the system. Transients and noise generated by those devices can couple into the VCA8500 and degrade performance.

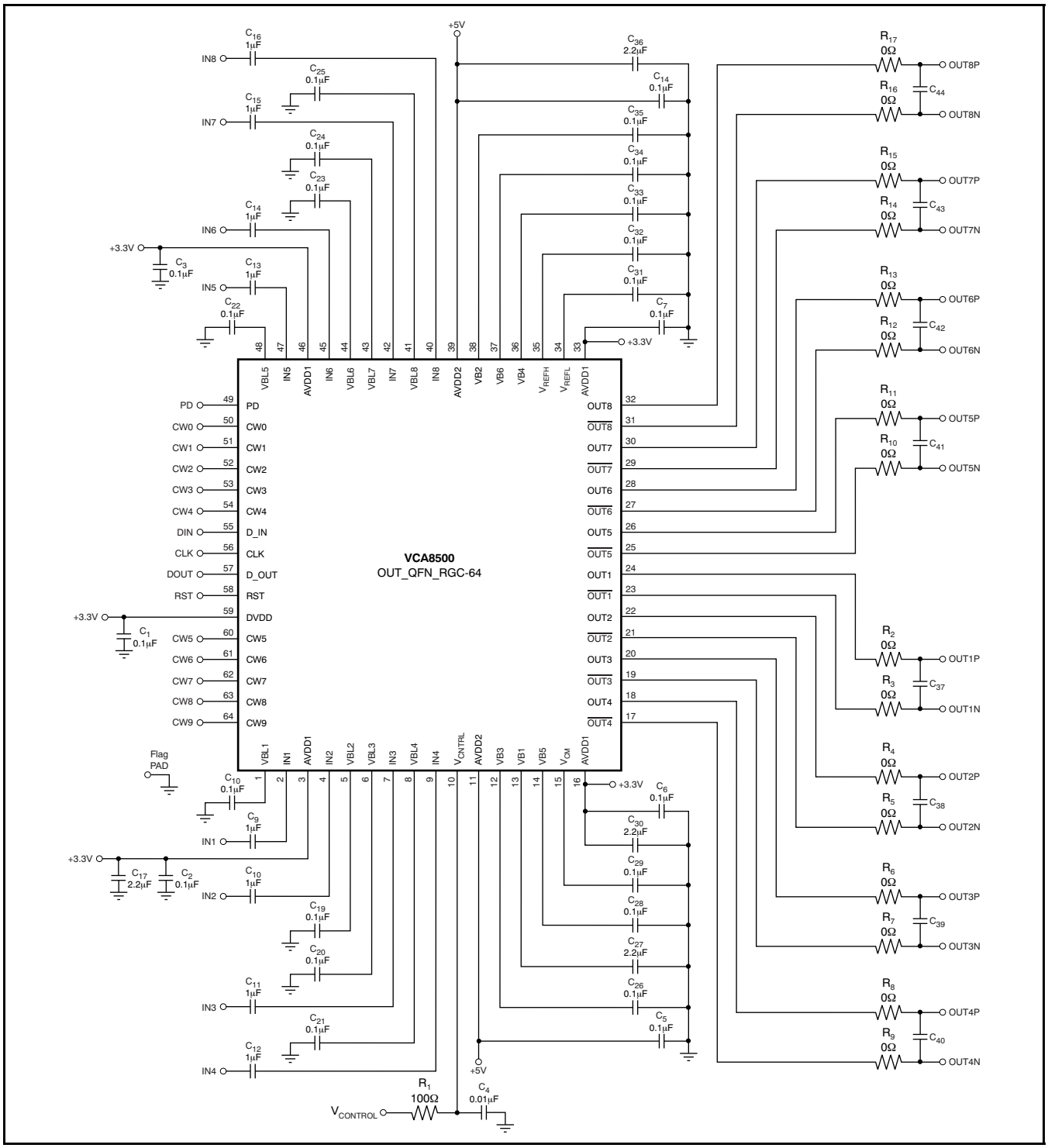
While the VCA8500 uses a thermally-enhanced QFN package that includes a PowerPAD on its backside, the primary function of the PowerPAD is to provide a solid ground reference point. Care should be taken to use this package pad during the PCB layout phase as the main ground return point.

POWER-DOWN MODES

The VCA8500 features two power-down modes—a standby mode and a shutdown mode. The standby mode function allows the VCA8500 to be rapidly placed in a low-power state. When in this mode, most amplifiers in the signal path are powered-down, while the internal references remain active. This state ensures that the external bypass capacitors retain the respective charges, minimizing the wake-up response time. As an example, Figure 59 illustrates the standby power-up/down response when the PD pin is toggled with a period of approximately 7.7ms (130Hz) with a 50% duty cycle. Here, the wake-up response time is approximately 40µs, while the power-down time is instantaneous (≤ 0.2µs). Factors such as the control voltage setting, input signal level, PD pin toggle time, and duty cycle primarily affect the wake-up response time. Therefore, the user should evaluate the VCA8500 performance under the desired system conditions.

When in standby mode, the part typically dissipates only 104mW, representing an 80% power reduction compared to the normal operating mode. This function is controlled through the PD pin (pin 49), which is designed to interface to +3.3V low-voltage logic. For normal operation, the PD pin should be tied to a logic low ('0'); pulling this pin high ('1') places the VCA into standby mode.

To achieve the lowest power dissipation of only 19mW, the VCA8500 can be placed in shutdown mode. This mode is controlled through the serial interface by setting bit D2 (PWR) of the control register to '1'. When in shutdown mode, all circuits (including references) within the VCA8500 are powered-down, causing the bypass capacitors to be discharged. Consequently, the wake-up time depends largely on the time needed to charge the bypass capacitors back up. Another factor is the elapsed time the VCA8500 spends in shutdown mode.



(1) $V_{CONTROL}$: Values for R_1 and C_4 should be selected for a desired time constant.

(2) Optional components: Values for R_2 to R_{17} and C_{37} to C_{44} should be selected based on the analog-to-digital converter selected.

(3) The +3.3V supply connections for DVDD and AVDD1 should be joined to a low-noise +3.3V system supply. Consider filtering any supply noise with an LC filter.

Figure 70. Typical Connection Diagram

GROUNDING AND BYPASSING

The VCA8500 uses a thermally-enhanced QFN package, with an exposed PowerPAD on the back side of the package. This backside pad is the only ground reference point of the VCA8500, and it should be connected to a low-noise system ground plane. All bypassing and power supplies for the VCA8500 should be referenced to this ground point.

All supply pins should be bypassed with 0.1μF ceramic chip capacitors (size 0603 or smaller). In order to minimize lead and trace inductance, the capacitors should be located as close to the supply pins as possible. Where double-sided component mounting is allowed, these capacitors are best placed directly under the package. In addition, larger bipolar decoupling capacitors (2.2μF to 10μF), effective at lower frequencies, may also be used on the main supply pins. They can be placed on the PCB in proximity to (less than 0.5in, or 12.7mm from) the VCA8500.

The VCA8500 internally generates a number of reference voltages, such as the bias voltages (VB1 through VB6). Note that in order to achieve the best low-noise performance, VB1 (pin 13) must be bypassed with a capacitor value of at least 1μF; the recommended value is 2.2μF. All other designated reference pins can be bypassed with smaller capacitor values, typically 0.1μF. For best results choose low-inductance ceramic chip capacitors (size 402) and place them as close to the device pins as possible.

BOARD LAYOUT

Proper grounding and bypassing, short lead length, and the use of ground planes are particularly important for high-frequency designs. Achieving optimum performance with a high gain amplifier such as the VCA8500 requires careful attention to the PCB layout to minimize the effect of board parasitics and optimize component placement. A multilayer PCB usually ensures best results and allows convenient component placement.

More details on the PowerPAD PCB layout and assembly process can be found in the Texas Instruments Application Reports, *Power-Pad Thermally-Enhanced Package* (SLMA002), and *QFN/SON PCB Attachment* (SLUA271A). These documents can be downloaded from the TI web site (www.ti.com).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
VCA8500IRGCT	ACTIVE	VQFN	RGC	64	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	VCA8500	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

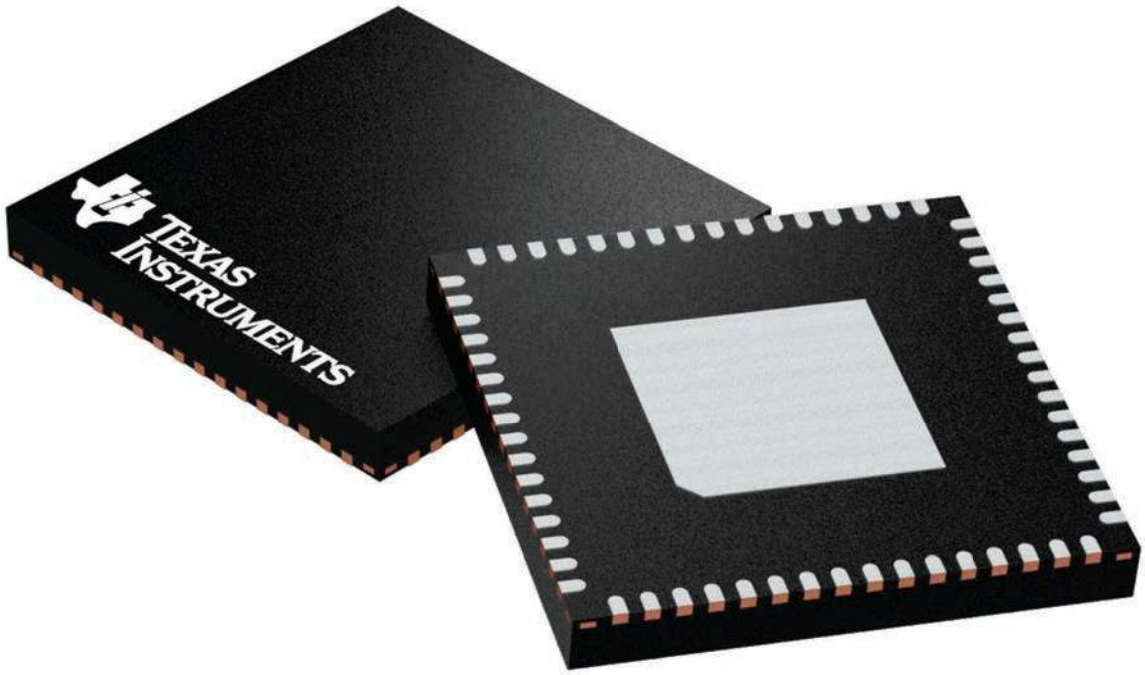
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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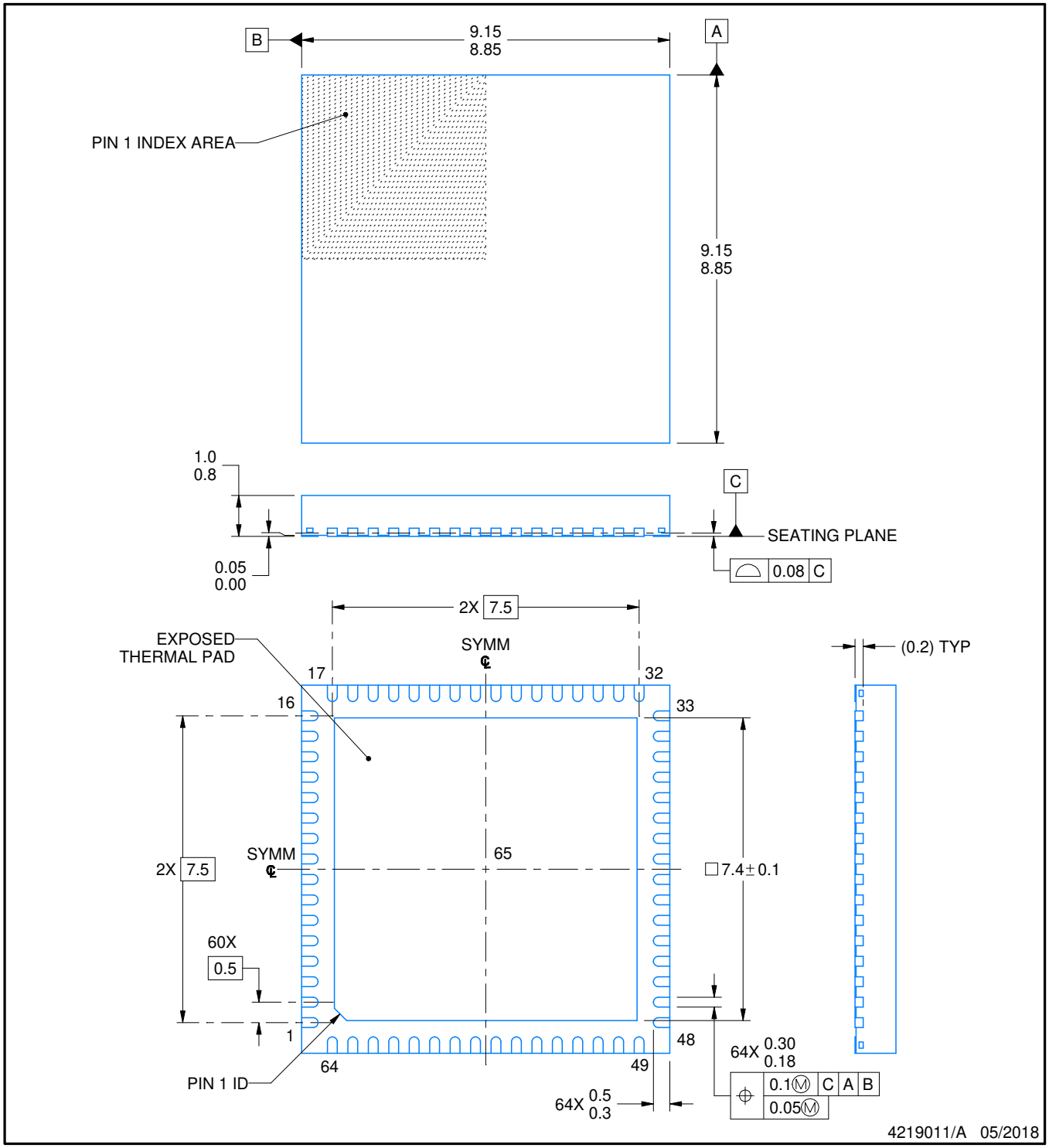
RGC0064H

PACKAGE OUTLINE

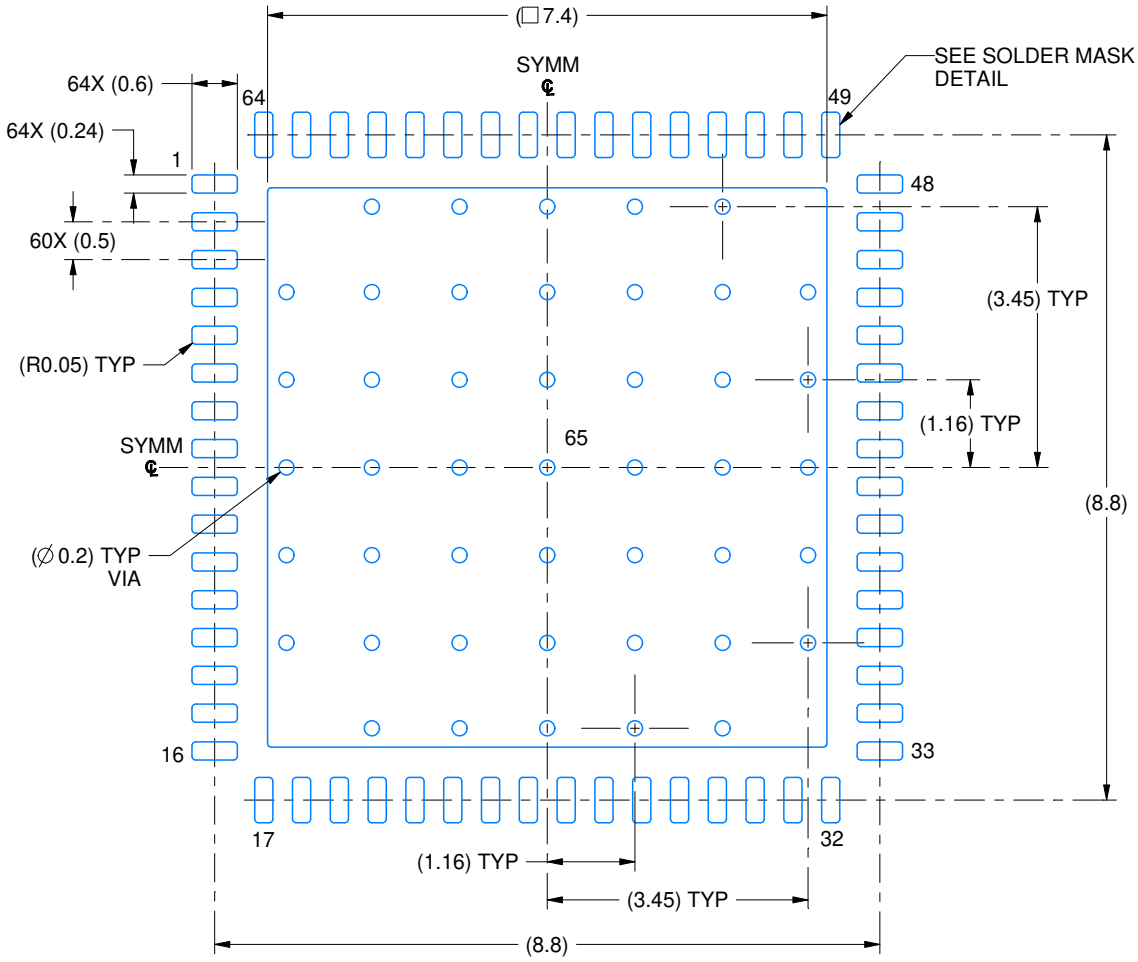
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

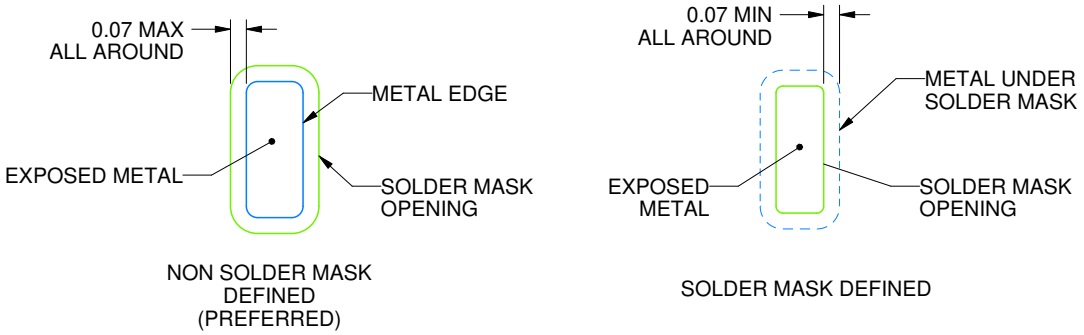


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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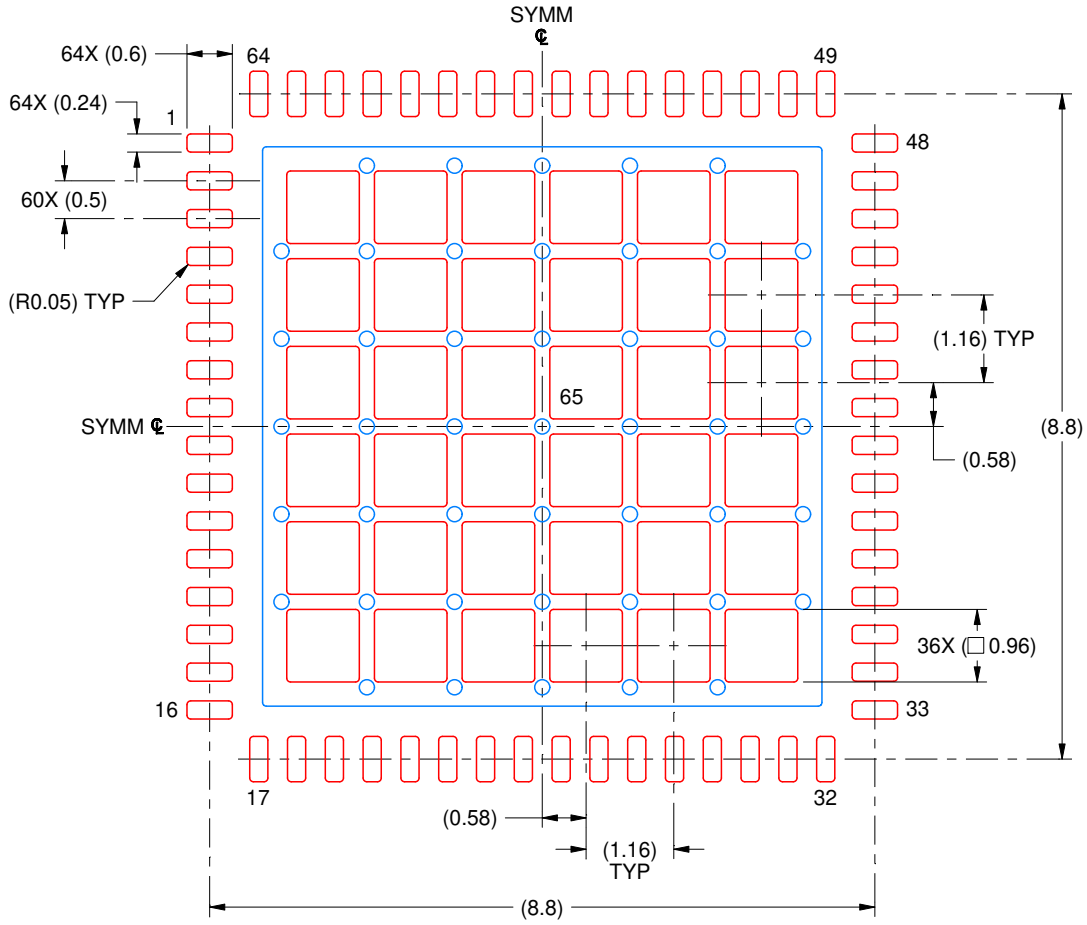
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
61% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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