

DM74LS395

4-Bit Shift Register with 3-STATE Outputs

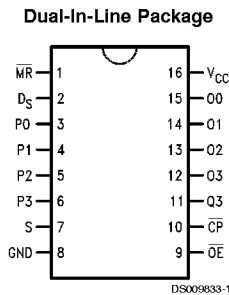
General Description

The LS395 is a 4-bit shift register with 3-STATE outputs and can operate in either a synchronous parallel load or a serial shift-right mode, as determined by the Select input. An asynchronous active LOW Master Reset (\overline{MR}) input overrides the synchronous operations and clears the register. An active LOW Output Enable (\overline{OE}) input controls the 3-STATE output buffers, but does not interfere with the other operations. The fourth stage also has a conventional output for linking purposes in multi-stage serial operations.

Features

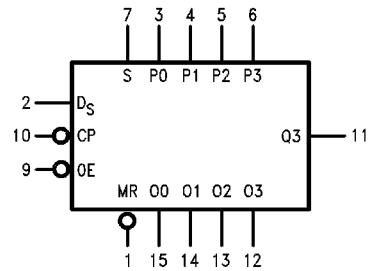
- Shift right or parallel 4-bit register
- 3-STATE outputs
- Input clamp diodes limit high speed termination effects
- Fully CMOS and TTL compatible

Connection Diagram



Order Number DM74LS395WM or DM74LS395N
See Package Number M16B or N16E

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Mode Select Table

Operating Mode	Inputs @ t _n					Outputs @ t _{n+1}			
	\overline{MR}	\overline{CP}	S	D _S	P _n	O0	O1	O2	O3
Asynchronous Reset	L	X	X	X	X	L	L	L	L
Shift, SET First Stage	H	~	L	H	X	H	O0 _n	O1 _n	O2 _n
Shift, RESET First Stage	H	~	L	L	X	L	O0 _n	O1 _n	O2 _n
Parallel Load	H	~	H	X	P _n	P0	P1	P2	P3

t_n, t_{n+1} = Time before and after CP HIGH-to-LOW transition
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Absolute Maximum Ratings (Note 1)

Supply Voltage
Input Voltage

7V
7V

Operating Free Air Temperature
Range
Storage Temperature Range

0°C to +70°C
-65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V _{CC}	Supply Voltage	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			V
V _{IL}	Low Level Input Voltage			0.8	V
I _{OH}	High Level Output Current			-0.4	mA
I _{OL}	Low Level Output Current			8	mA
T _A	Free Air Operating Temperature	0		70	°C
t _s (H)	Setup Time HIGH or LOW	20			ns
t _s (L)	S, D _S or P _n to CP	20			
t _h (H)	Hold Time HIGH or LOW	5			ns
t _h (L)	S, D _S or P _n to \overline{CP}	5			
t _w (L)	\overline{CP} Pulse Width LOW	18			ns
t _w (L)	\overline{MR} Pulse Width LOW	20			ns

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = -18 mA			-1.5	V
V _{OH}	High Level Output Voltage	V _{CC} = Min, I _{OH} = Max V _{IL} = Max	2.7			V
V _{OL}	Low Level Output Voltage	V _{CC} = Min, I _{OL} = Max V _{IH} = Min		0.35	0.5	V
		I _{OL} = 4 mA, V _{CC} = Min		0.25	0.4	
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 7V			0.1	mA
I _{IH}	High Level Input Current	V _{CC} = Max, V _I = 2.7V			20	μA
I _{IL}	Low Level Input Current	V _{CC} = Max, V _I = 0.4V			-0.4	mA
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 3)	-20		-100	mA
I _{CC}	Supply Current with Outputs OFF	V _{CC} = Max, \overline{OE} , D _S , S = 4.5V \overline{CP} = \sim , P _n = GND			29	mA
	Supply Current with Outputs ON	V _{CC} = Max, D _S , S = 4.5V \overline{OE} , \overline{CP} , P _n = GND			25	mA
I _{OZH}	3-STATE Output Off Current HIGH	V _{CC} = V _{CCH} V _{OZH} = 2.7V			20	μA
I _{OZL}	3-STATE Output Off Current LOW	V _{CC} = V _{CCH} V _{OZL} = 0.4V			-20	μA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

$V_{CC} = +5.0V, T_A = +25^\circ C$

Symbol	Parameter	$R_L = 2\text{ k}\Omega, C_L = 15\text{ pF}$		Units
		Min	Max	
f_{max}	Maximum Shift Frequency	30		MHz
t_{PLH}	Propagation Delay		35	ns
t_{PHL}	\overline{CP} to O_n		25	ns
t_{PHL}	Propagation Delay		35	ns
t_{PHL}	\overline{MR} to O_n		35	ns
t_{PZH}	Output Enable Time		20	ns
t_{PZL}			20	ns
t_{PHZ}	Output Disable Time		17	ns
t_{PLZ}			23	ns

Functional Description

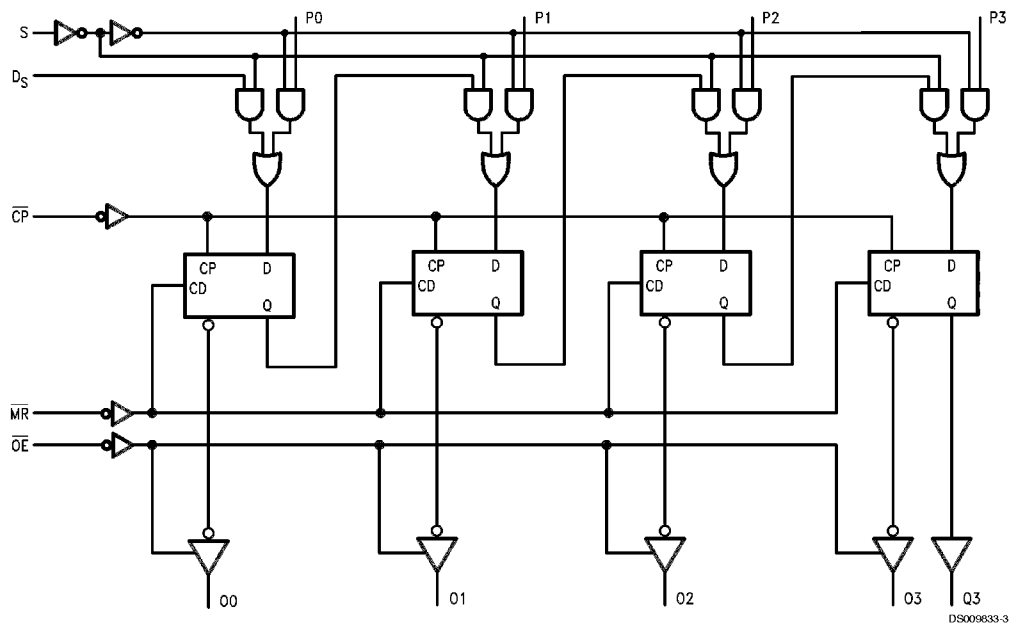
The 'LS395 contains four D-type edge-triggered flip-flops and auxiliary gating to select a D input either from a Parallel (P_n) input or from the preceding stage. When the Select input is HIGH, the P_n inputs are enabled. A LOW signal in the S input enables the serial inputs for shift-right operations, as indicated in the Truth Table.

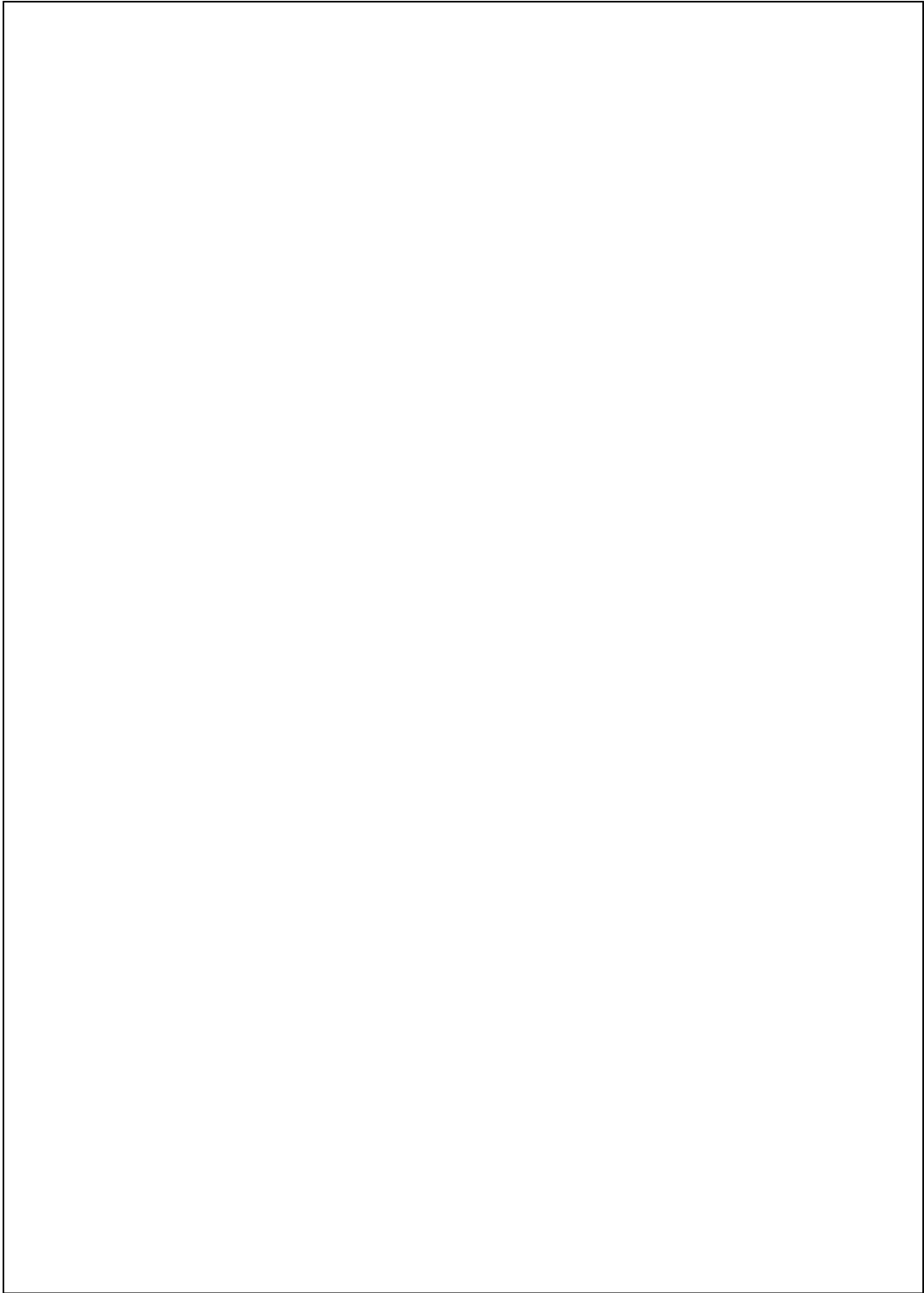
State changes are initiated by HIGH-to-LOW transitions on the Clock Pulse (\overline{CP}) input. Signals on the P_n , D_S and S inputs can change when the Clock is in either state, provided that the recommended setup and hold times are observed.

When the S input is LOW, a \overline{CP} HIGH-LOW transition transfers data in O_0 to O_1 , O_1 to O_2 , and O_2 to O_3 . A left-shift is accomplished by connecting the outputs back to the P_n inputs, but offset one place to the left, i.e., O_3 to P_2 , O_2 to P_1 , and O_1 to P_0 , with P_3 acting as the linking input from another package.

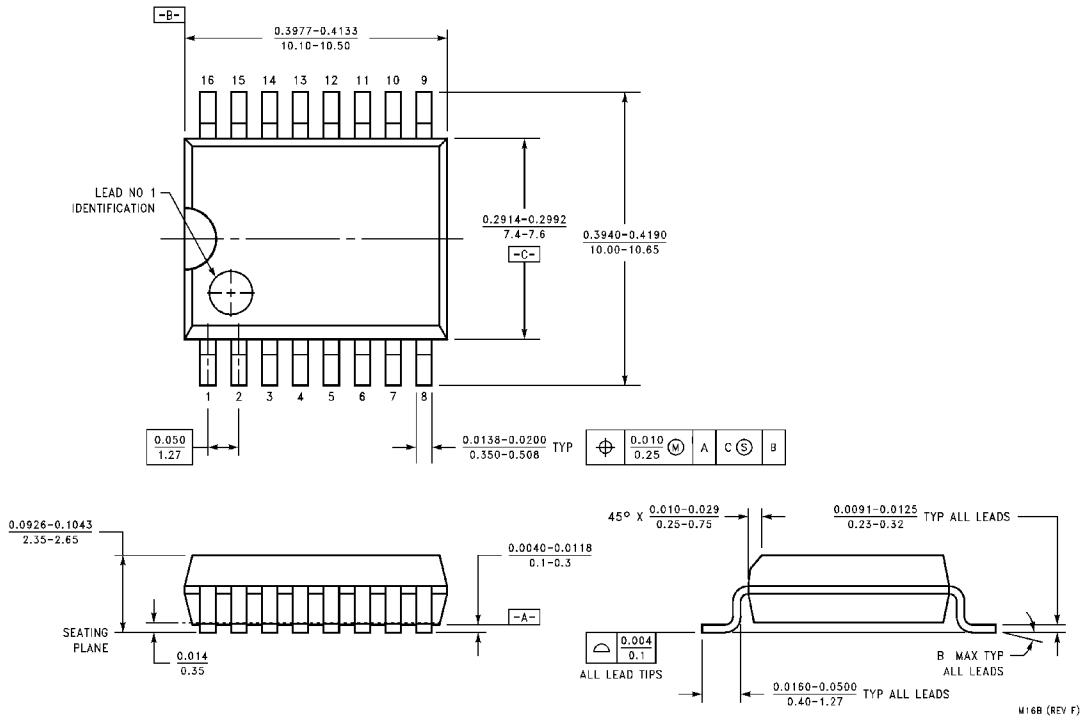
When the \overline{OE} input is HIGH, the output buffers are disabled and the O_0 – O_3 outputs are in a high impedance condition. The shifting, parallel loading or resetting operations can still be accomplished, however.

Logic Diagram

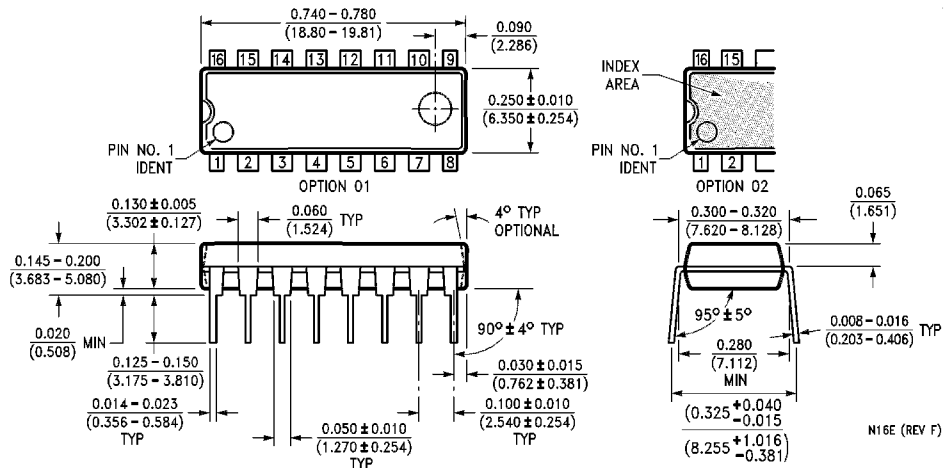




Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Wide Small Outline Molded Package (M)
Order Number DM74LS395WM
Package Number M16B



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS395N
Package Number N16E