HD3SS215 6.0 Gbps HDMI DisplayPort 2:1/1:2 Differential Switch

1 Features

- General purpose 2:1/1:2 differential switch
- Compatible with displayport electrical standard
- Compatible with hdmi electrical standards
- 2:1 and 1:2 switching supporting data rates up to 6 Gbps
- Supports HPD switching
- Supports AUX and DDC switching
- Wide –3-dB differential bandwidth of 7 GHz
- Excellent dynamic characteristics (at 3 GHz)
  - Crosstalk = –35 dB
  - Isolation = –21 dB
  - Insertion Loss = –1.6 dB
  - Return Loss = –12 dB
  - Max Bit-Bit Skew = 5 ps
- VDD operating range 3.3 V ±10%
- Commercial temperature range: 0°C to 70°C (HD3SS215)
- Industrial temperature range: –40°C to 85°C (HD3SS215I)
- Package options:
  - 5 mm x 5 mm, 50-ball ZXH
  - 8 mm × 8 mm, 56-pin RTQ
- Output enable (OE) pin disables switch to save power
- Power consumption:
  - Active < 9 mW typical
  - Standby < 30 µW maximum (when OE = L)

2 Applications

- Desktop and Notebook Applications:
  - PCI Express Gen 1, Gen 2 Switching
  - DP Switching
  - HDMI Switching
  - LVDS Switching
- Connected peripherals & printers
- Home theater & entertainment
- TV
- Gaming
- Pro audio, video & signage

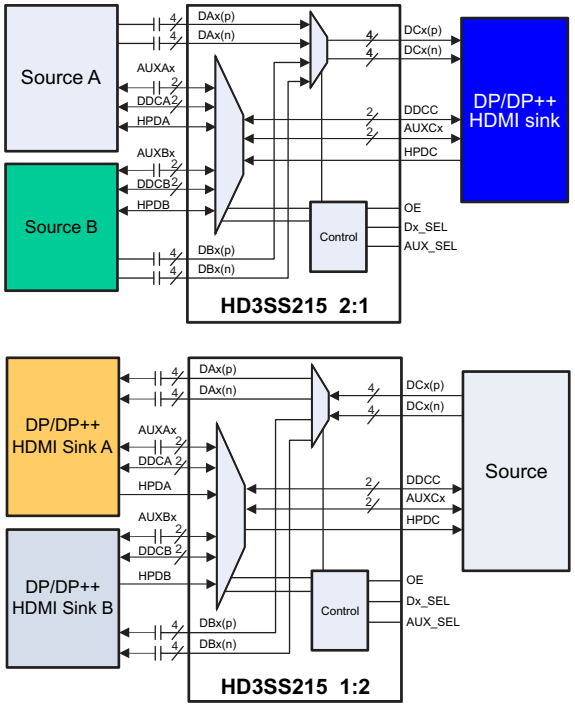
3 Description

HD3SS215 is a high-speed wide common mode passive switch capable of supporting DisplayPort HBR2 and high definition multimedia interface (HDMI) applications requiring 4k2k 60Hz refresh rates. The HD3SS215 can be configured to support two sources to one sink or one source to two sinks. To support these video standards the HD3SS215 also switches the display data channel (DDC) and hot plug detect (HPD) signals for HDMI or digital video interface (DVI) applications. It also switches the auxiliary (AUX) and hot plug detect (HPD) signals for DisplayPort applications. The flexibility the HD3SS215 provides by supporting both wide common mode and AC or DC coupled links makes it ideal for many applications.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
HD3SS215, HD3SS215I	nFBGA (50)	5.00 mm x 5.00 mm
	QFN (56)	8.00 mm × 8.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



Application Schematic

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (September 2015) to Revision E (December 2020) **Page**

- NOTE: The device in the MicroStar Jr. BGA packaging were redesigned using a laminate nFBGA package. This nFBGA package offers datasheet-equivalent electrical performance. It is also footprint equivalent to the MicroStar Jr. BGA. The new package designator in place of the discontinued package designator will be updated throughout the datasheet....1
- Changed u*jr ZQE to nFBGA ZXH....1
- Changed u*jr ZQE to nFBGA ZXH....4
- Changed u*jr ZQE to nFBGA ZXH....4
- Changed u*jr ZQE to nFBGA ZXH....4
- Changed u*jr ZQE to nFBGA ZXH....7
- Changed u*jr ZQE to nFBGA ZXH. Updated thermal data....9
- Changed u*jr ZQE to nFBGA ZXH....11
- Changed u*jr ZQE to nFBGA ZXH....16

Changes from Revision C (August 2015) to Revision D (September 2015) **Page**

- Changed Section 3 text string from "....DisplayPort 1.2a..." to "...DisplayPort HBR2..." and from "..HDMI2.0.." to "...HDMI..." 1
- Deleted $R_{\theta JC(bot)}$ spec from Thermal Information table as N/A....9
- Deleted "Operating free air temperature" spec from Electrical Characteristics table....10
- Changed Figure 9-5 20
- Changed Section Power Supply Recommendations text string from "Decoupling capacitors may be used to reduce noise and improve power supply integrity" to "Decoupling capacitors must be used to reduce power supply noise"....0

Changes from Revision B (July 2015) to Revision C (July 2015) **Page**

- Added $t_{on(OE\_L\text{-}H)}$, $t_{off(OE\_H\text{-}L)}$, and t_{SWITCH_OVER} to the *Section 7.7* 11

Changes from Revision A (May 2014) to Revision B (July 2015) **Page**

- Changed the title From: "2.0/DisplayPort 1.2A" To: "DisplayPort"....1

- Changed *Section 1* list item From: Compatible With DisplayPort 1.2a Electrical Standard To: Compatible With DisplayPort Electrical Standard 1
- Changed *Section 1* list item From: Compatible With HDMI 1.4b and HDMI 2.0 Electrical Standards To: Compatible With HDMI Electrical Standards 1
- Added *Section 1* item: Commercial Temperature Range: –40°C to 70°C (HD3SS215) 1
- Added *Section 1* item: Inductrial Temperature Range: –40°C to 85°C (HD3SS215I) 1
- Added *Section 1*, Package Options: 8 mm × 8 mm, 56-Pin RTQ 1
- Changed the *Section 2* list item From: TV and Monitors To: UHDTV, HDTV and Monitors 1
- Added Section 5 paragraph. 4
- Added the 56-Pin QFN image 4
- Added RTQ column to the *Pin Functions* table 4
- Added RTQ column to the *Pin Functions* table 7
- Moved T_{stg} From: *Section 7.2* To: *Section 7.1* 9
- Changed the *Handling Ratings* table to *Section 7.2* table 9
- Added HD3SS2151I, Operating free-air temperature *Section 7.3* 9
- Added RTQ 56 PIN values to the *Section 7.4* 9
- Added table Note " This pin can be driven.." to the *Section 7.5* table 10
- Changed the *Section 7.6* table to include ZQE and RTQ package values 11
- Added the *Section 7.7* table 11
- Added section: *Section 9.2.4* 20
- Added Figure 10-3 22

Changes from Revision * (May 2014) to Revision A (May 2014) **Page**

- Changed Section 3 section 1
- Changed Figure 9-1 16

5 Description (continued)

One typical application would be a mother board that includes two GPUs that need to drive one DisplayPort sink. The GPU is selected by the Dx_SEL pin. Another application is when one source needs to switch between one of two sinks, such as a side connector an a docking station connector. The switching is controlled using the Dx_SEL and AUX_SEL pins. The HD3SS215I operates from a single supply voltage of 3.3 V, over full industrial temperature range –40°C to 85°C, in the ZXH package and 56 pin RTQ package.

6 Pin Configuration and Functions

	1	2	3	4	5	6	7	8	9
A	Dx_SEL	VDD		DA0(n)	DA1(n)	DA2(n)		DA3(p)	DA3(n)
B	DC0(n)	DC0(p)	GND	DA0(p)	DA1(p)	DA2(p)	OE	DB0(p)	DB0(n)
C		AUX_SEL						GND	
D	DC1(n)	DC1(p)						DB1(p)	DB1(n)
E	DC2(n)	DC2(p)						DB2(p)	DB2(n)
F	DC3(n)	DC3(p)						DB3(p)	DB3(n)
G		GND						GND	
H	AUXC(n)	AUXC(p)	HPDB	GND	DDCCLK_B	AUXB(p)	GND	DDCCLK_A	AUXA(p)
J	HPDC	HPDA	DDCCLK_C	VDD	DDCDAT_B	AUXB(n)	DDCDAT_C	DDCDAT_A	AUXA(n)

Figure 6-1. 50-Pin µBGA ZXH Package (Top View)

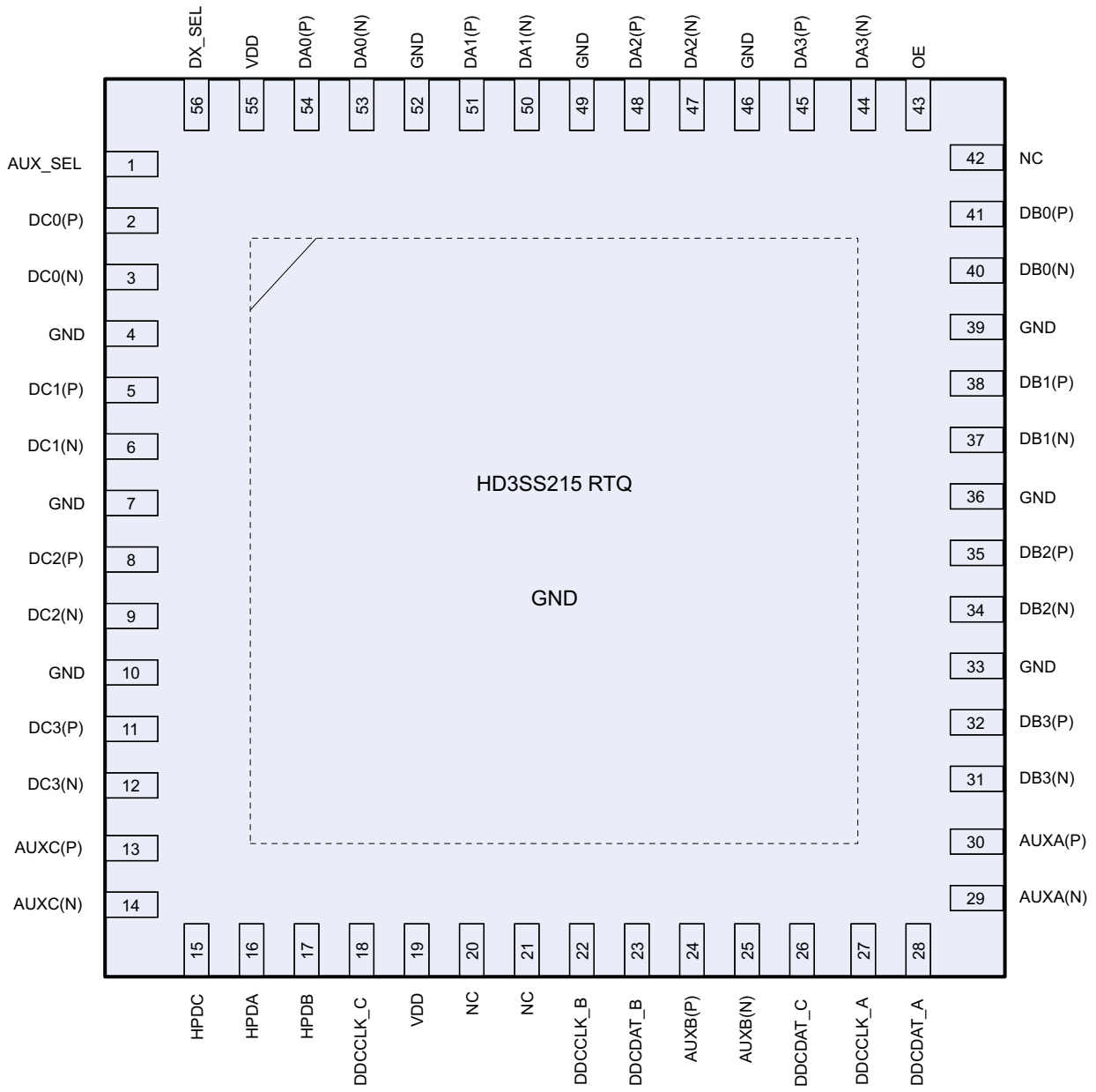


Figure 6-2. 56-Pin QFN RTQ Package (Top View)

Table 6-1. Pin Functions

PIN			I/O	DESCRIPTION[1]
NAME	NO.			
	ZXH	RTQ		
Dx_SEL	A1	56	2 Level Control I	High Speed Port Selection Control Pins
AUX_SEL	C2	1	3 Level Control I	AUX/DDC Selection Control Pin in Conjunction with Dx_SEL Pin
DA0(p)	B4	54	I/O	Port A, Channel 0, High Speed Positive Signal
DA0(n)	A4	53		Port A, Channel 0, High Speed Negative Signal
DA1(p)	B5	51	I/O	Port A, Channel 1, High Speed Positive Signal
DA1(n)	A5	50		Port A, Channel 1, High Speed Negative Signal
DA2(p)	B6	48	I/O	Port A, Channel 2, High Speed Positive Signal
DA2(n)	A6	47		Port A, Channel 2, High Speed Negative Signal

Table 6-1. Pin Functions (continued)

PIN			I/O	DESCRIPTION[1]
NAME	NO.			
	ZXH	RTQ		
DA3(p)	A8	45	I/O	Port A, Channel 3, High Speed Positive Signal
DA3(n)	A9	44		Port A, Channel 3, High Speed Negative Signal
DB0(p)	B8	41	I/O	Port B, Channel 0, High Speed Positive Signal
DB0(n)	B9	40		Port B, Channel 0, High Speed Negative Signal
DB1(p)	D8	38	I/O	Port B, Channel 1, High Speed Positive Signal
DB1(n)	D9	37		Port B, Channel 1, High Speed Negative Signal
DB2(p)	E8	35	I/O	Port B, Channel 2, High Speed Positive Signal
DB2(n)	E9	34		Port B, Channel 2, High Speed Negative Signal
DB3(p)	F8	32	I/O	Port B, Channel 3, High Speed Positive Signal
DB3(n)	F9	31		Port B, Channel 3, High Speed Negative Signal
DC0(p)	B2	2	I/O	Port C, Channel 0, High Speed Positive Signal
DC0(n)	B1	3		Port C, Channel 0, High Speed Negative Signal
DC1(p)	D2	5	I/O	Port C, Channel 1, High Speed Positive Signal
DC1(n)	D1	6		Port C, Channel 1, High Speed Negative Signal
DC2(p)	E2	8	I/O	Port C, Channel 2, High Speed Positive Signal
DC2(n)	E1	9		Port C, Channel 2, High Speed Negative Signal
DC3(p)	F2	11	I/O	Port C, Channel 3, High Speed Positive Signal
DC3(n)	F1	12		Port C, Channel 3, High Speed Negative Signal
AUXA(p)	H9	30	I/O	Port A AUX Positive Signal
AUXA(n)	J9	29		Port A AUX Negative Signal
AUXB(p)	H6	24	I/O	Port B AUX Positive Signal
AUXB(n)	J6	25		Port B AUX Negative Signal
AUXC(p)	H2	13	I/O	Port C AUX Positive Signal
AUXC(n)	H1	14		Port C AUX Negative Signal
DDCCLK_A	H8	27	I/O	Port A DDC Clock Signal
DDCDAT_A	J8	28		Port A DDC Data Signal
DDCCLK_B	H5	22	I/O	Port B DDC Clock Signal
DDCDAT_B	J5	23		Port B DDC Data Signal
DDCCLK_C	J3	18	I/O	Port C DDC Clock Signal
DDCDAT_C	J7	26		Port C DDC Data Signal
HPDA/B/C	J2, H3, J1	16, 17, 15	I/O	Port A/B/C Hot Plug Detect
OE	B7	43	I	Output Enable: OE = VIH: Normal Operation OE = VIL: Standby Mode
VDD	A2, J4	19, 55	Supply	3.3 V Positive power supply voltage
GND	B3, C8, G2, G8 H4, H7	4, 7, 10, 33, 36, 39, 46, 49, 52	Supply	Ground
NC		20, 21, 42		Not connected
Thermal Pad	–	–	GND	Supply Ground

(1) Only the high speed data DAz/DBz ports incorporate 20kΩ pull down resistors that are switched in when a port is not selected and switched out when the port is selected.

Pin Functions

PIN			I/O	DESCRIPTION[1]
NAME	NO.			
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AUX_SEL	C2	1	3 Level Control I	AUX/DDC Selection Control Pin in Conjunction with Dx_SEL Pin
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DA0(n)	A4	53		Port A, Channel 0, High Speed Negative Signal
DA1(p)	B5	51	I/O	Port A, Channel 1, High Speed Positive Signal
DA1(n)	A5	50		Port A, Channel 1, High Speed Negative Signal
DA2(p)	B6	48	I/O	Port A, Channel 2, High Speed Positive Signal
DA2(n)	A6	47		Port A, Channel 2, High Speed Negative Signal
DA3(p)	A8	45	I/O	Port A, Channel 3, High Speed Positive Signal
DA3(n)	A9	44		Port A, Channel 3, High Speed Negative Signal
DB0(p)	B8	41	I/O	Port B, Channel 0, High Speed Positive Signal
DB0(n)	B9	40		Port B, Channel 0, High Speed Negative Signal
DB1(p)	D8	38	I/O	Port B, Channel 1, High Speed Positive Signal
DB1(n)	D9	37		Port B, Channel 1, High Speed Negative Signal
DB2(p)	E8	35	I/O	Port B, Channel 2, High Speed Positive Signal
DB2(n)	E9	34		Port B, Channel 2, High Speed Negative Signal
DB3(p)	F8	32	I/O	Port B, Channel 3, High Speed Positive Signal
DB3(n)	F9	31		Port B, Channel 3, High Speed Negative Signal
DC0(p)	B2	2	I/O	Port C, Channel 0, High Speed Positive Signal
DC0(n)	B1	3		Port C, Channel 0, High Speed Negative Signal
DC1(p)	D2	5	I/O	Port C, Channel 1, High Speed Positive Signal
DC1(n)	D1	6		Port C, Channel 1, High Speed Negative Signal
DC2(p)	E2	8	I/O	Port C, Channel 2, High Speed Positive Signal
DC2(n)	E1	9		Port C, Channel 2, High Speed Negative Signal
DC3(p)	F2	11	I/O	Port C, Channel 3, High Speed Positive Signal
DC3(n)	F1	12		Port C, Channel 3, High Speed Negative Signal
AUXA(p)	H9	30	I/O	Port A AUX Positive Signal
AUXA(n)	J9	29		Port A AUX Negative Signal
AUXB(p)	H6	24	I/O	Port B AUX Positive Signal
AUXB(n)	J6	25		Port B AUX Negative Signal
AUXC(p)	H2	13	I/O	Port C AUX Positive Signal
AUXC(n)	H1	14		Port C AUX Negative Signal
DDCCLK_A	H8	27	I/O	Port A DDC Clock Signal
DDCDAT_A	J8	28		Port A DDC Data Signal
DDCCLK_B	H5	22	I/O	Port B DDC Clock Signal
DDCDAT_B	J5	23		Port B DDC Data Signal
DDCCLK_C	J3	18	I/O	Port C DDC Clock Signal
DDCDAT_C	J7	26		Port C DDC Data Signal
HPDA/B/C	J2, H3, J1	16, 17, 15	I/O	Port A/B/C Hot Plug Detect
OE	B7	43	I	Output Enable: OE = VIH: Normal Operation OE = VIL: Standby Mode
VDD	A2, J4	19, 55	Supply	3.3 V Positive power supply voltage
GND	B3, C8, G2, G8 H4, H7	4, 7, 10, 33, 36, 39, 46, 49, 52	Supply	Ground
NC		20, 21, 42		Not connected

PIN			I/O	DESCRIPTION(1)
NAME	NO.			
	ZXH	RTQ		
Thermal Pad	–	–	GND	Supply Ground

(1) Only the high speed data DAz/DBz ports incorporate 20kΩ pull down resistors that are switched in when a port is not selected and switched out when the port is selected.

7 Specifications

7.1 Absolute Maximum Ratings (1) (2)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Supply voltage	V_{DD}	–0.5	4	V
Voltage	Differential I/O	–0.5	4	V
	AUX_SEL, Dx_SEL	–0.5	4	
	HPDx, DDCCLK_X, DDCDAT_X	–0.5	6	
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential voltages, are with respect to network ground pin.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1250	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Main power supply		3	3.3	3.6	V
T_A	Operating free-air temperature	HD3SS215	0		70	°C
		HD3SS215I	–40		85	°C
C_{AC}	AC coupling capacitor		75	100	200	nF

7.4 Thermal Information

THERMAL METRIC(1)		HD3SS215		UNIT
		RTQ (56 PIN)	ZXH (50 PIN)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90.5	69.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.9	35.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	53.9	40.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.4	40.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Typical values for all parameters are at V_{DD} = 3.3 V and T_A = 25°C. All temperature limits are specified by design.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage		3	3.3	3.6	V
V_{IH}	Input high voltage	Control Pins, Signal Pins (Dx_SEL, AUX_SEL, OE)	2		V_{DD}	V
		HPD and DDC	2		5.5	
V_{IM}	Input mid level voltage	AUX_SEL Pin (1)	$V_{DD}/2$ – 300mV	$V_{DD}/2$	$V_{DD}/2$ + 300mV	V
V_{IL}	Input low voltage	Control Pins, Signal Pins (Dx_SEL, AUX_SEL, OE)	–0.1		0.8	V
V_{I/O_Diff}	Differential voltage (Dx, AUXx)	Switch I/O diff voltage	0		1.8	Vpp
V_{CM}	Common voltage (Dx, AUXx)	Switch common mode voltage	0		3.3	V
I_{IH}	Input high current (Dx_SEL, AUX_SEL)	V_{DD} = 3.6 V, V_{IN} = V_{DD}			1	µA
I_{IM}	Input mid current (AUX_SEL)	V_{DD} = 3.6 V, V_{IN} = $V_{DD}/2$			1	
I_{IL}	Input low current (Dx_SEL, AUX_SEL)	V_{DD} = 3.6 V, V_{IN} = GND		0.01	1	
I_{LK}	Leakage current (Dx_SEL, AUX_SEL)	V_{DD} = 3.6 V, V_{IN} = 2 V, OE = 3.3 V		0.01	2	
		V_{DD} = 3.6 V, V_{IN} = 2 V, OE = 0 V		0.01	2	
	Leakage current (HPDx/DDCx)	V_{DD} = 3.6 V, V_{IN} = 2 V, OE = 0 V; Dx_SEL = 3.3 V		0.01	5	
		V_{DD} = 3.6 V, V_{IN} = 2 V, OE = 3.3 V; Dx_SEL = GND		0.01	5	
I_{OFF}	Device shut down current	V_{DD} = 3.6 V, OE = GND			8	
I_{DD}	Supply current	V_{DD} = 3.6 V, Dx_SEL= V_{DD}; AUX_SEL = GND; Outputs Floating		2.5	3.2	mA
DA, DB, DC HIGH SPEED SIGNAL PATH						
R_{ON}	ON resistance	V_{CM} = 0 V–3.3 V, I_O = –1mA		8	14	Ω
ΔR_{ON}	On resistance match between pairs of the same channel	V_{CM} = 0 V–3. 3V, I_O = –1 mA			1.5	Ω
R_{FLAT_ON}	On resistance flatness ($R_{ON(MAX)}$ – $R_{ON(MAIN)}$)	V_{CM} = 0 V–3.3 V		1.3		Ω
AUXx, DDC, SIGNAL PATH						
$R_{ON(AUX)}$	ON resistance on AUX channel	V_{CM} = 0 V–3.3 V, I_O = –8 mA		5	8	Ω
$R_{ON(DDC)}$	ON resistance on DDC channel	V_{CM} = 0.4 V, I_O = -3 mA		30	40	Ω

(1) This pin can be driven to the specified level or 10 kΩ. Pull up and pull downs can be used. It cannot be left floating.

7.6 Electrical Characteristics, Device Parameters (1)

Under recommended operating conditions; R_{LOAD}, R_{SC} = 50 Ω (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
RL	Dx Differential return loss	ZXH package	1.35 GHz		–15		dB
			3 GHz		–12		
		RTQ package	1.35 GHz		–17		
			3 GHz		–13		
X_{TALK}	Dx Differential crosstalk	ZXH package	2.7 GHz		–35		dB
		RTQ package			–35		
O_{IRR}	Dx Differential off-isolation	ZXH package	3 GHz		–21		dB
		RTQ package			–16		
I_L	Dx Differential insertion loss	ZXH package	f = 1.35 GHz		–1.2		dB
			f = 3 GHz		–1.6		
		RTQ package	f = 1.35 GHz		–2		dB
			f = 3 GHz		–2.4		
BW_{Dx}	Dx Differential -3-dB bandwidth	ZXH package			7		GHz
		RTQ package			5		
BW_{AUX}	AUX –3-dB bandwidth				720		MHz

(1) For Return Loss, Crosstalk, Off-Isolation, and Insertion Loss values the data was collected on a Rogers material board with minimum length traces on the input and output of the device under test.

7.7 Switching Characteristics

Under recommended operating conditions; R_{LOAD}, R_{SC} = 50 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Switch propagation delay	R_{SC} and R_{LOAD} = 50 Ω, See Figure 7-2			200	ps
$t_{on(OE\_L-H)}$	Time from OE toggling High and valid data at the outputs	R_{SC} and R_{LOAD} = 50 Ω, V_{CM} = 3 V - 3.3 V		1	2	µs
$t_{off(OE\_H-L)}$	Time from OE toggling Low and outputs are in Z-state			15	50	
t_{SWITCH_OVER}	Time to switch between ports when DX_SEL or AUX_SEL state is changed for Data, AUX, DDC signals	R_{SC} and R_{LOAD} = 50 Ω, See Figure 7-1		0.7	1	µs
t_{on}	Dx_SEL/AUX_SEL-to-Switch t_{on} (HPD)	R_{LOAD} = 125k Ω, See Figure 7-1		0.7	1	µs
t_{off}	Dx_SEL/AUX_SEL-to-Switch t_{off} (HPD)			0.7	20	
$t_{SK(O)}$	Inter-Pair output skew (CH-CH)	R_{SC} and R_{LOAD} = 50 Ω, See Figure 7-2			30	ps
$t_{SK(b-b)}$	Intra-Pair output skew (bit-bit)			1	5	

7.8 Timing Diagrams

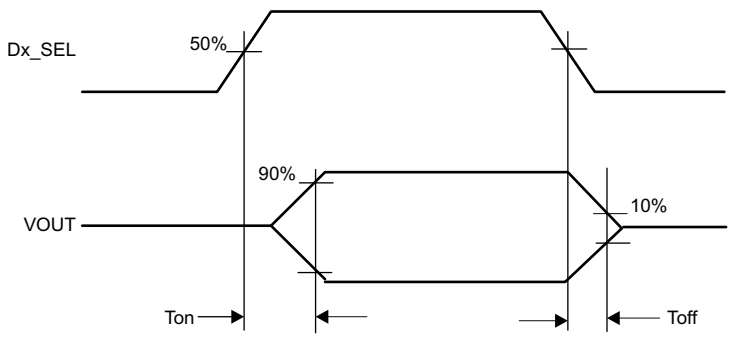
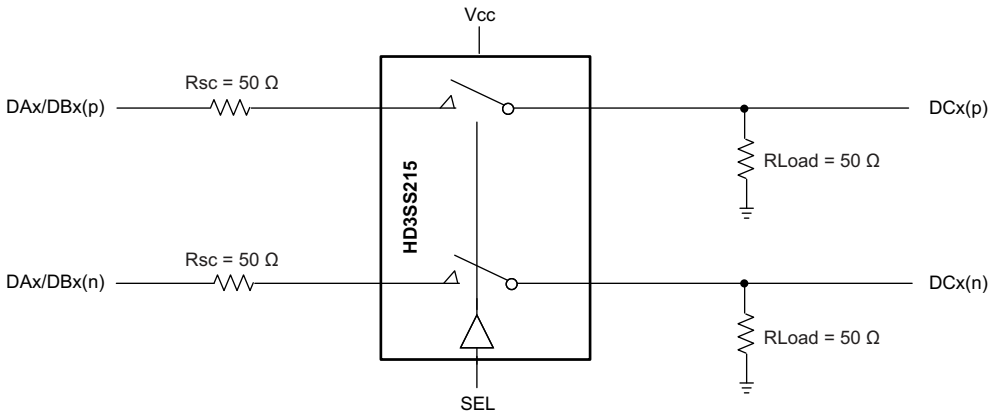
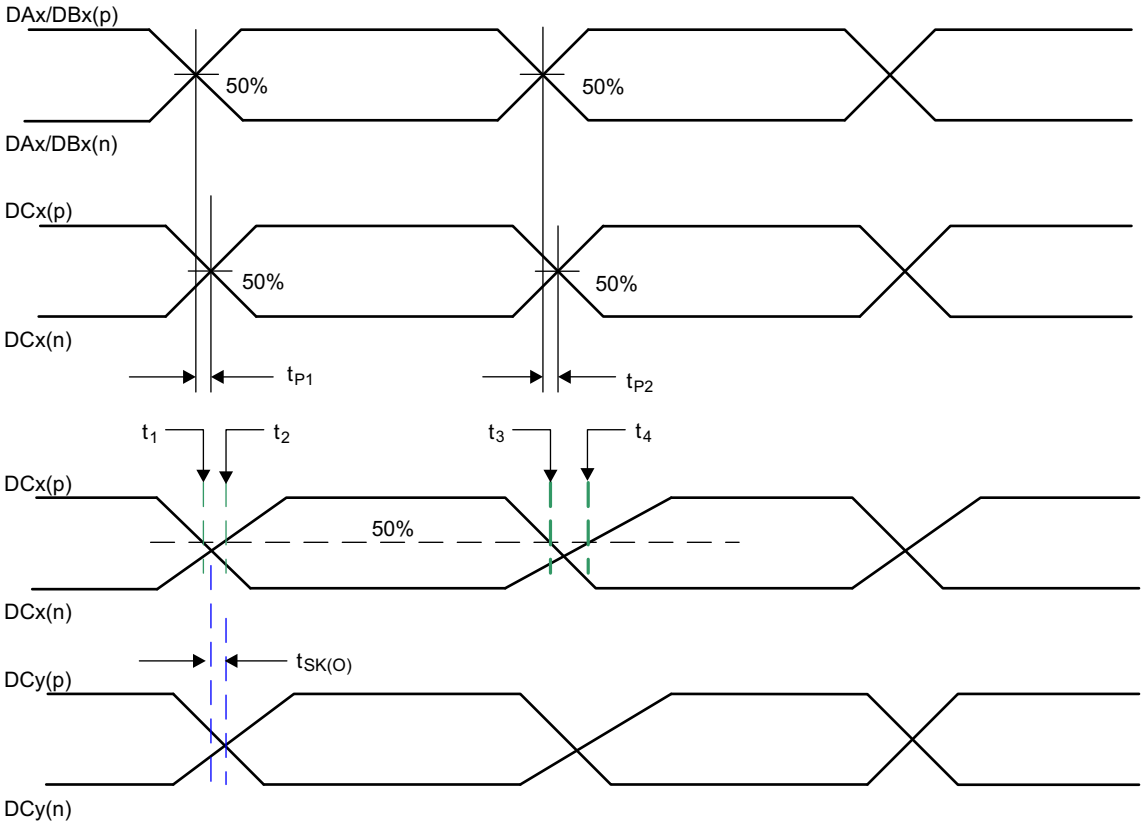


Figure 7-1. Select to Switch t_{on} and t_{off}





t_{PD} = Max(t_{p1}, t_{p2})

$t_{SK(O)}$ = Difference between t_{PD} for any two pairs of outputs

$t_{SK(b\text{-}b)}$ = 0.5 X |(t_4 – t_3) + (t_1 – t_2)|

Figure 7-2. Propagation Delay and Skew

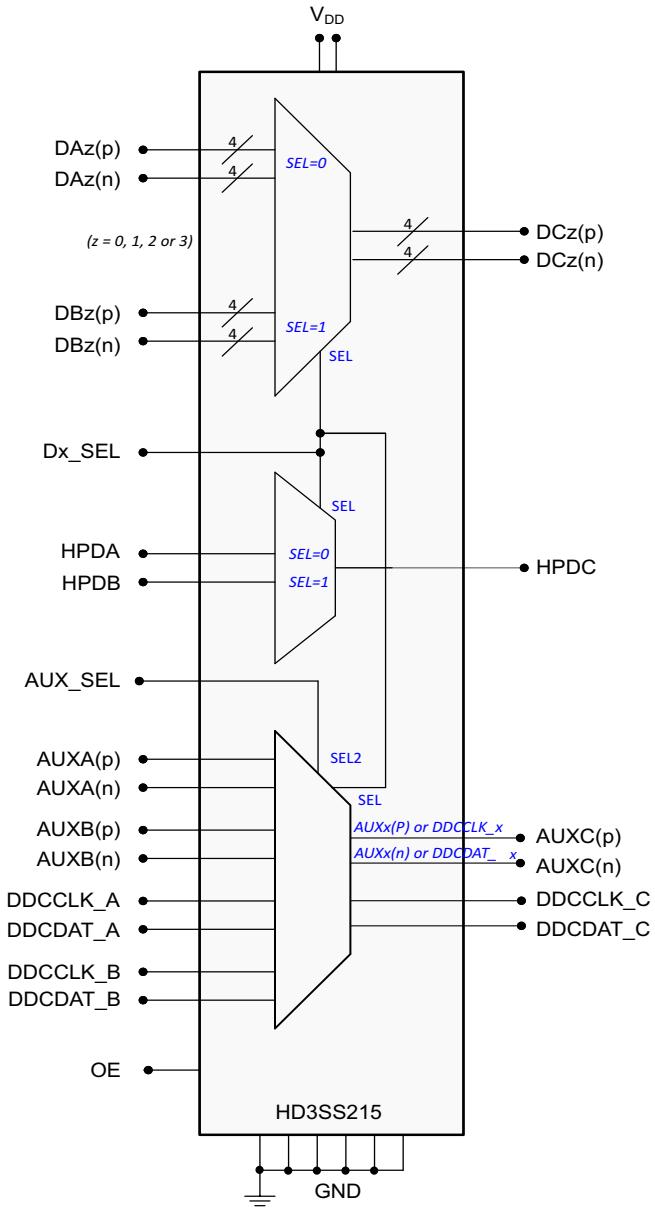
8 Detailed Description

8.1 Overview

The HD3SS215 is a generic analog, differential passive switch that can work for any high speed interface applications, as long as it is biased at a common mode voltage range of 0 V to 3.3 V and has differential signaling with differential amplitude up to 1800 mV_{pp}. It employs adaptive tracking that maintains the high speed channel impedance over the entire common mode voltage range. In high-speed applications and data paths, signal integrity is an important concern. The switch offers excellent dynamic performance such as high isolation, crosstalk immunity, and minimal bit-bit skew. These characteristics allow the device to function seamlessly in the system without compromising signal integrity. The 2:1/1:2, mux/de-mux device operates with ports A or B switched to port C, or port C switched to either port A or B. This flexibility allows an application to select between one of two Sources on ports A and B and send the output to the sink on port C. Similarly, a Source on port C can select between one of two Sink devices on ports A and B to send the data. To comply with DisplayPort, DP++ and HDMI applications, the HD3SS215 also switches AUX, HPD, and DDC along with the high-speed differential signals. The HPD and data signals are both switched through the Dx_SEL pin. AUX and DDC are controlled with AUX_SEL and Dx_SEL. The Functional Modes section contains information on how to set the control pins.

With an OE control pin, the HD3SS215 is operational, with low active current, when this pin is high. When OE is pulled lowed, the device goes into standby mode and draws very little current in order to save power consumption in the application.

8.2 Functional Block Diagram



The high speed data ports incorporate 20kΩ pull down resistors that are switched in when a port is not selected and switched out when the port is selected.

Figure 8-1. Functional Block Diagram

8.3 Feature Description

8.3.1 High Speed Switching

The HD3SS215 supports switching of 6 Gbps data rates. The wide common mode of the device enables it to support TMDS signal levels and DisplayPort signals. The high speed muxing is designed with a wide –3dB differential bandwidth of 7 GHz and industry leading dynamic characteristics. All of these attributes help maintain signal integrity in the application. Each high speed port incorporates 20kΩ pull down resistors that are switched in when the port is not selected and switched out when the port is selected.

8.3.2 HPD, AUX, and DDC Switching

HPD, AUX and DDC switching is supported through the HD3SS215. This enables the device to work in multiple application scenarios within multiple electrical standards. The AUXA/B and DDCA/B lines can both be switched to the AUXC port. This feature supports DP++ or AUX only adapters. For HDMI applications, the DDC channels are switched to the DDC_C port only and the AUX channel can remain active or the end user can make it float.

8.3.3 Output Enable and Power Savings

The HD3SS215 has two power modes, active/normal operating mode, and standby mode. During standby mode, the device consumes very little current to save the maximum power. To enter standby mode, the OE control pin is pulled low and must remain low. For active/normal operation, the OE control pin should be pulled high to VDD through a resistor.

8.4 Device Functional Modes

8.4.1 Switch Control Modes

Refer to the *Section 8.2*.

The HD3SS215 behaves as a two to one or one to two differential switch using high bandwidth pass gates. The input ports are selected using the AUX_SEL pin and Dx_SEL pin which are shown in Table 8-1.

Table 8-1. Switch Control Logic (1) (2) (3)

CONTROL LINES(4)		SWITCHED I/O PINS								
AUX_SEL	Dx_SEL	DCz(p) Pin z = 0, 1, 2 or 3	DCz(n) Pin z = 0, 1, 2 or 3	HPDC Pin	AUXA	AUXB	AUXC	DDCA	DDCB	DDCC
L	L	DAz(p)	DAz(n)	HPDA	To/From AUXC	Z	To/From AUXA	Z	Z	Z
L	H	DBz(p)	DBz(n)	HPDB	Z	To/From AUXC	To/From AUXB	Z	Z	Z
H	L	DAz(p)	DAz(n)	HPDA	Z	Z	To/From DDCA	To/From AUXC	Z	Z
H	H	DBz(p)	DBz(n)	HPDB	Z	Z	To/From DDCB	Z	To/From AUXC	Z
M(4)	L	DAz(p)	DAz(n)	HPDA	To/From AUXC	Z	To/From AUXA	To/From DDCC	Z	To/From DDCA
M(4)	H	DBz(p)	DBz(n)	HPDB	Z	To/From AUXC	To/From AUXB	Z	To/From DDCC	To/From DDCB

(1) Z = High Impedance
(2) OE pin - For normal operation, drive OE high. Driving the OE pin low will disable the switch.
(3) The ports which are not selected by the control lines will be in high impedance status.
(4) For HDMI application, keep the AUX_SEL at middle level voltage. The AUX channel is still active, and the end user can make the lines float.

9 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

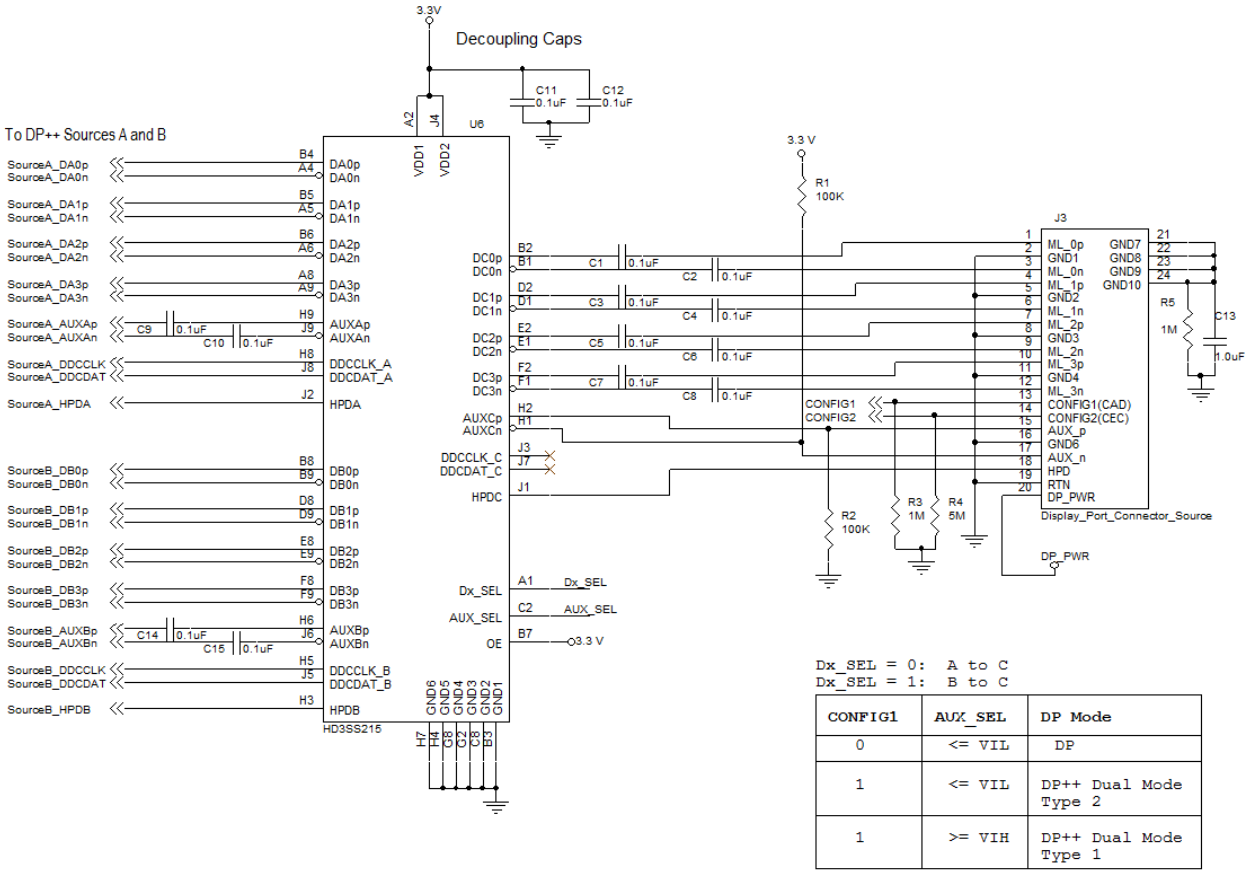
9.1 Application Information

The HD3SS215 can be used in a variety of applications. This section shows the typical applications for DisplayPort , DP++, and HDMI. The example diagrams illustrate using the HD3SS215 in a two source to one sink application and a one source to two sinks application. All schematics are using the ZXH pin-out.

9.2 Typical Applications

9.2.1 DisplayPort and Dual Mode Adapter with Two Sources

The application schematic below shows the HD3SS215 in the 2:1 configuration for DisplayPort switching. The HD3SS215 receives inputs from DP Source A and DP Source B. The control pins of the device can be set to select Source A/B inputs and transfer them to port C through the Dx_SEL control pin. The schematic also shows the CONFIG1 and AUX_SEL settings to configure the HD3SS215 to work with DP++ Type 2 and Type1 adapters. For this specific schematic, the AC capacitors needed on the MainLink signal lines are shown on the Sink side of the HD3SS215. This is done to decrease the BOM. If desired the AC capacitors maybe placed in the signal path on the Source A/B side of HD3SS215. Additional diagrams are provided to show the configuration of the AUX channel for 2:1 and 1:2 DisplayPort only applications.



CONFIG1	AUX_SEL	DP Mode
0	<= VIL	DP
1	<= VIL	DP++ Dual Mode Type 2
1	>= VIH	DP++ Dual Mode Type 1

Figure 9-1. HD3SS215 Application Diagram for DisplayPort or Dual Mode Adapter Configuration

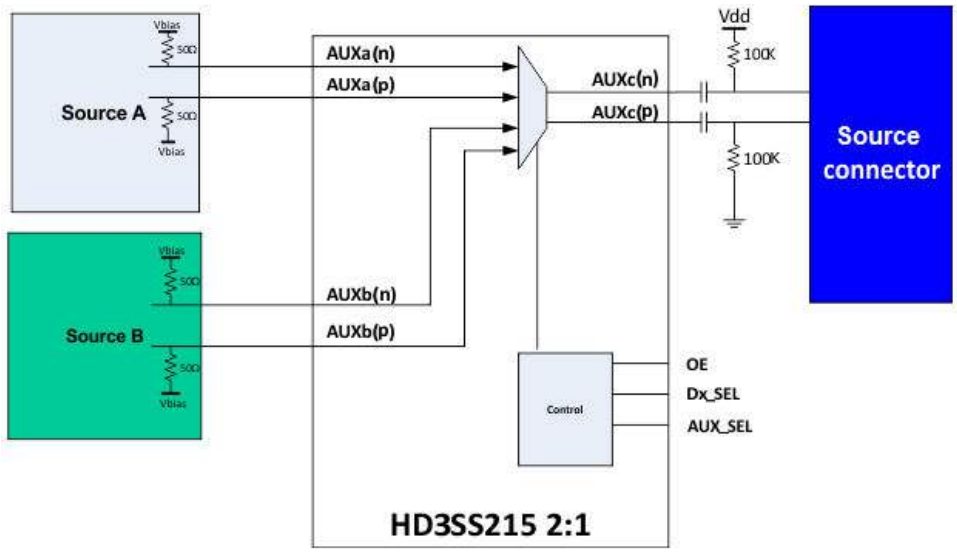


Figure 9-2. HD3SS215 AUX Channel in 2:1 DisplayPort Application

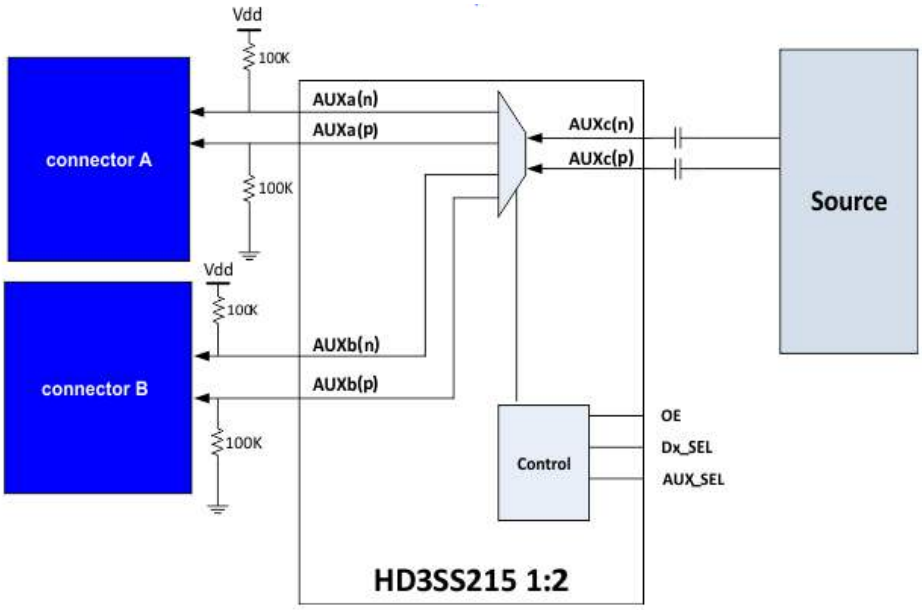


Figure 9-3. HD3SS215 AUX Channel in 1:2 DisplayPort Application

9.2.1.1 Design Requirements

Table 9-1. Design Parameters

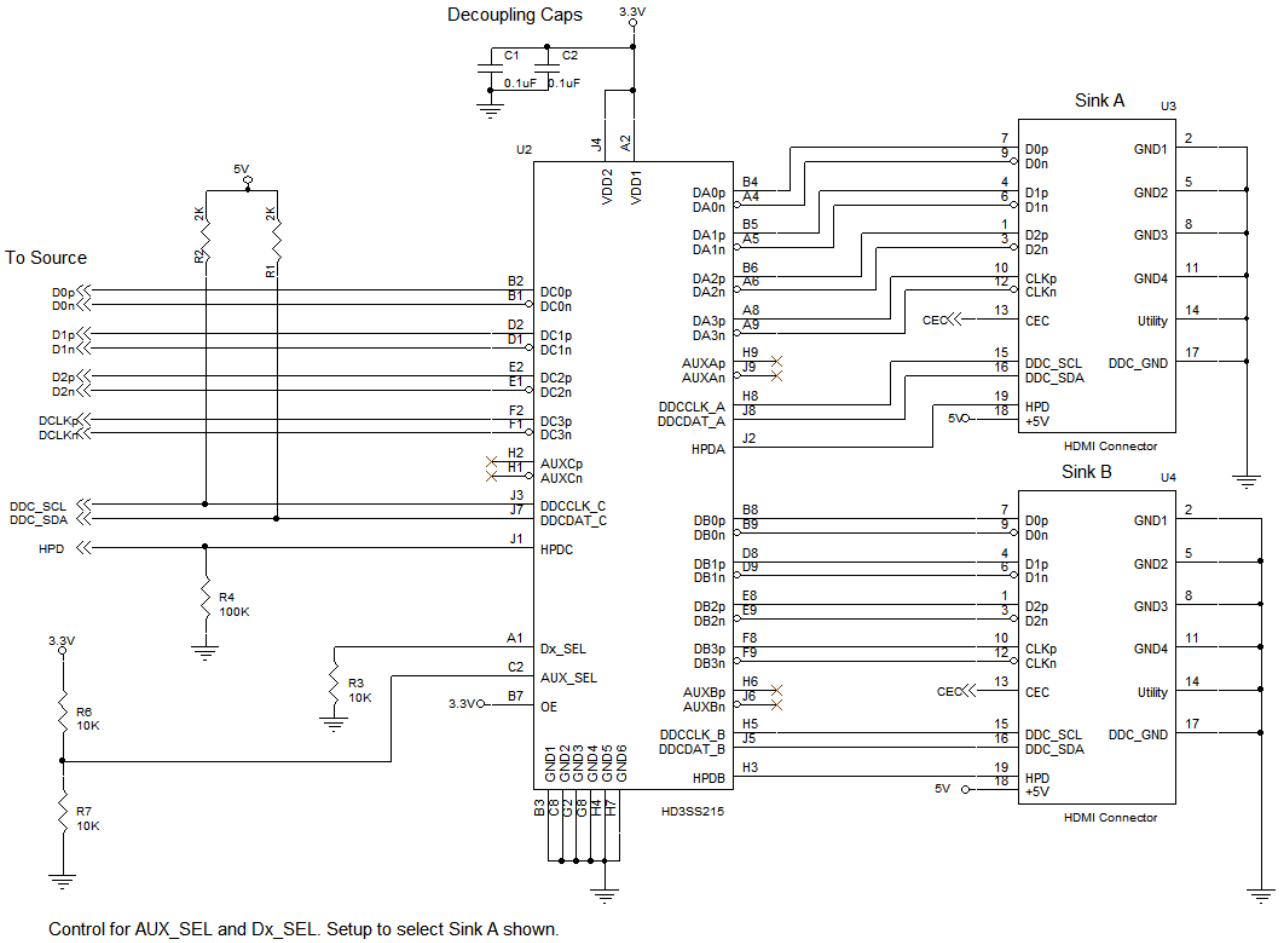
DESIGN PARAMETER	EXAMPLE VALUE
VDD	3.3 V
Decoupling Capacitors	0.1 µF
AC Capacitors	75 nF to 200 nF (100 nF shown)
AUX Pull-Up/Pull-Down Resistors	10 kΩ to105 kΩ (100 kΩ shown)
Pull-Up/Pull-Down Resistors for Control Pins	10 kΩ
CONFIG1/CONFIG2 Pull-Down Resistors	1 MΩ and 5 MΩ

9.2.1.2 Detailed Design Procedure

The HD3SS215 is designed to operate with a 3.3 V power supply. Levels above those listed in the Absolute Ratings table should not be used. If using a higher voltage system power supply, a voltage regulator can be used to step down to 3.3 V. Decoupling capacitors may be used to reduce noise and improve power supply integrity. AC capacitors must be placed on the MainLink lines. Additionally, AC capacitors are placed on the AUXC lines. After the blocking capacitors, the AUXCp line must be pulled down weakly through a resistor to ground, and the AUXCn line must be pulled up weakly through a resistor to VDD. The voltage level of the control pins, AUX_SEL and Dx_SEL should be set according to the application and muxing desired. For a DisplayPort connector, the CONFIG1 and CONFIG2 pins should be pulled to ground through resistors. For Dual Mode adapter implementation, the CONFIG1 line may be used to perform cable adapter detection. The CONFIG2 line can be configured for an HDMI adaptor or left as a no connect for a DVI adapter. The CONFIG2 pin on the connector should be pulled up or left floating accordingly for Dual Mode adapter configuration.

9.2.2 HDMI Application with Two Sinks

The HD3SS215 can be placed in applications needing to switch between two sinks. In this example, the HDMI source selects between Sink A or Sink B in the 1:2 configuration.



Control for AUX_SEL and Dx_SEL. Setup to select Sink A shown.

Figure 9-4. Application Diagram for a 1:2 Configuration with HDMI Source and Connectors

9.2.2.1 Design Requirements

Table 9-2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VDD	3.3 V
Decoupling Capacitors	0.1 µF
DDC Pull-Up Resistors	1.5 kΩ to 2 kΩ to 5 V (2 kΩ shown)
Pull-Up/Pull-Down Resistors for Control Pins	10 kΩ
HPD Pull-Down Resistor	100 kΩ

9.2.2.2 Detailed Design Procedure

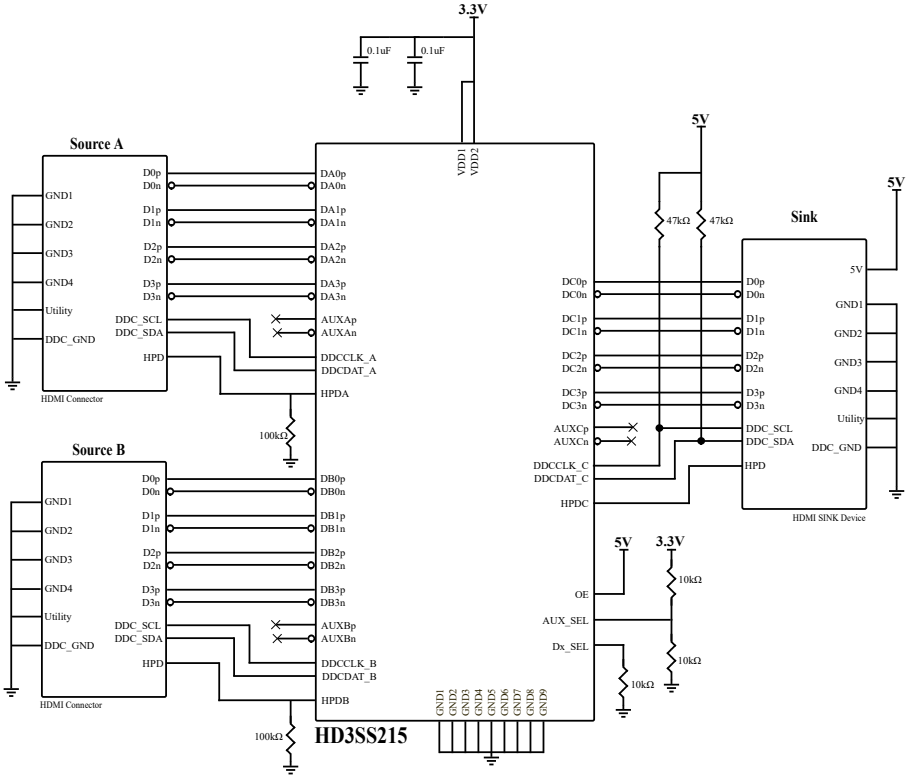
The HD3SS215 is designed to operate with a 3.3 V power supply. Levels above those listed in the Absolute Ratings table should not be used. If using a higher voltage system power supply, a voltage regulator can be used to step down to 3.3 V. Decoupling capacitors may be used to reduce noise and improve power supply integrity. Pull-up resistors to 5 V must be placed on the source side DDC clock and data lines according to the HDMI2.0 Standard. A weak pull down resistor should be placed on the source side HPD line. This is to ensure the source

can differentiate between when HPD is disconnected or at a high voltage level. The AUX_SEL and Dx_SEL control pins should be set according to the application and desired muxing.

9.2.3

9.2.4 HDMI 2:1 Sink Application Using the RTQ Package

The HD3SS215 can be placed in applications needing to switch between two HDMI connectors and one Generic HDMI sink.



AUX_SEL and Dx_SEL configured for A to C

Figure 9-5. HDMI 2:1 Sink Application Using the RTQ Package

Note

According to the HDMI specification the DDC 2-kΩ pullup resistors can be replaced by 47-kΩ pullups. Figure 9-5 schematic and Figure 10-3 PCB layout example shows 47-kΩ pullup resistors.

Power Supply Recommendations

The HD3SS215 is designed to operate with a 3.3-V power supply. Levels above those listed in the Absolute Ratings table should not be used. If using a higher voltage system power supply, a voltage regulator can be used to step down to 3.3 V. Decoupling capacitors must be used to reduce power supply noise.

10 Layout

10.1 Layout Guidelines

- The ESD and EMI protection devices (if used) should be placed as close as possible to the connector.
- Place voltage regulators as far away as possible from the high-speed differential pairs.
- It is recommended that small decoupling capacitors for the HD3SS215 power rail be placed close to the device.
- The high-speed differential signal traces should be routed on the top layer to avoid the use of vias and allow clean interconnects to the mux.
- The high speed differential signal traces should be routed parallel to each other as much as possible. It is recommended the traces be symmetrical.
- In order to control impedance for transmission lines, a solid ground plane should be placed next to the high-speed signal layer. This also provides an excellent low-inductance path for the return current flow.
- The power plane should be placed next to the ground plane to create additional high-frequency bypass capacitance.
- Adding test points will cause impedance discontinuity and will therefore negatively impact signal performance. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes stubs on the differential pair.
- Avoid 90 degree turns in traces. The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥135 degrees. This will minimize any length mismatch caused by the bends and therefore minimize the impact bends have on EMI.

10.2 Layout Example

An example layout for the HD3SS215 shows the device implemented on a 4-layer board. The layout figures follow the DisplayPort application schematic above. The top layer layout view shows the signal routing for two sources and one sink. The bottom layer layout view shows the remaining signal routing and a copper pour implemented for the decoupling capacitors.

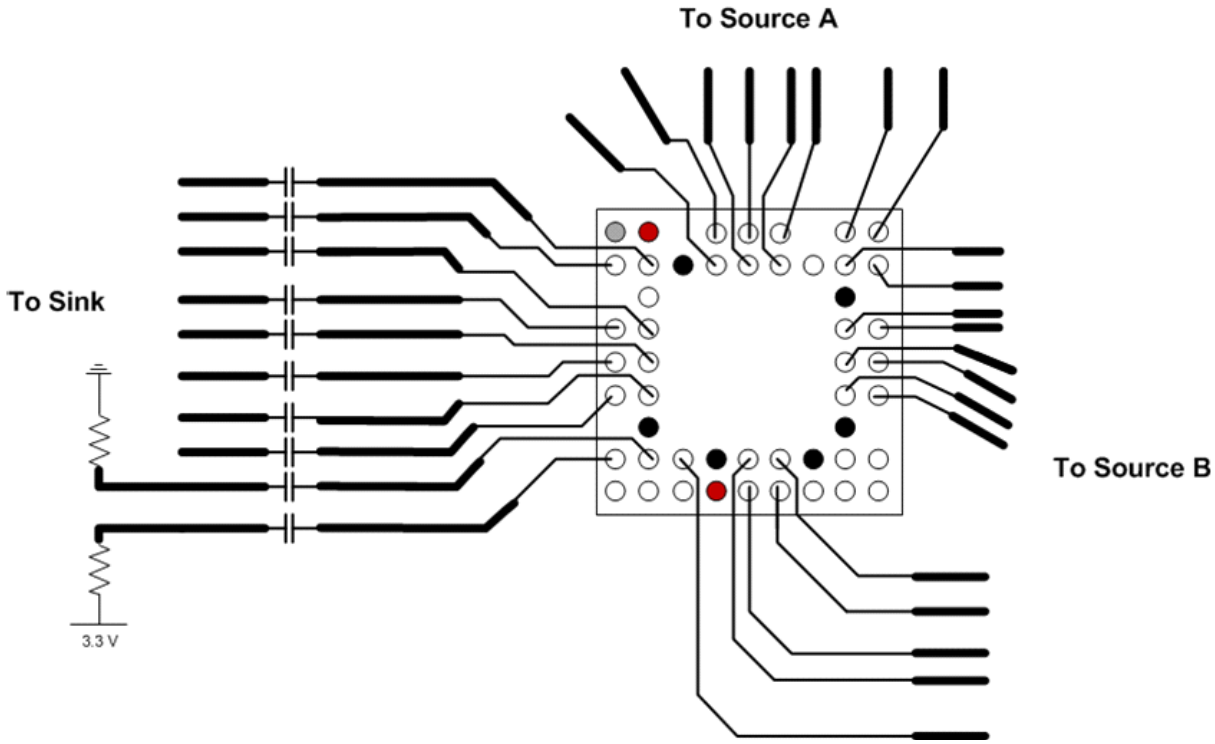


Figure 10-1. Top Layer Layout View

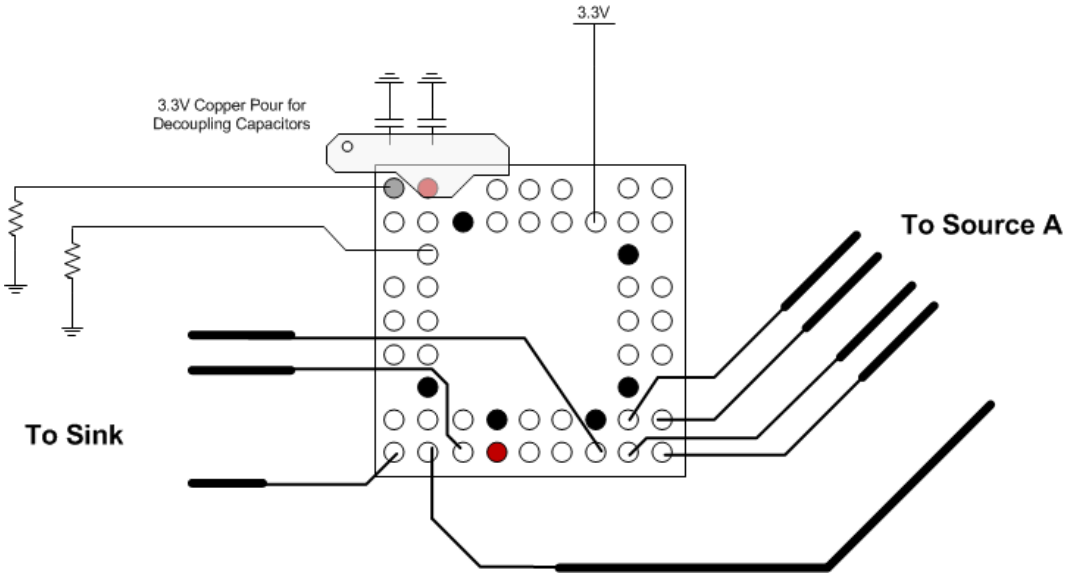


Figure 10-2. Bottom Layer Layout View

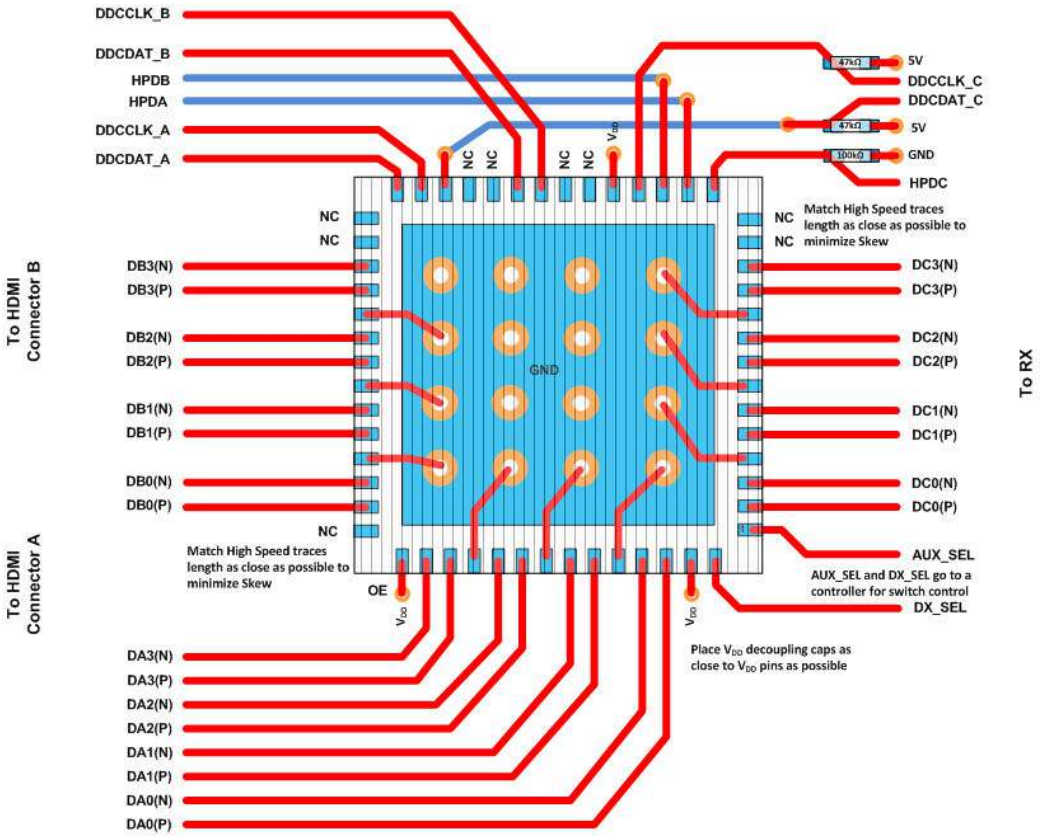


Figure 10-3. RTQ Layout for 2:1 HDMI Sink Application

11 Device and Documentation Support

11.1 Community Resources

11.2 Trademarks

All trademarks are the property of their respective owners.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HD3SS215IRTQR	ACTIVE	QFN	RTQ	56	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	HD3SS215I	Samples
HD3SS215IRTQT	ACTIVE	QFN	RTQ	56	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	HD3SS215I	Samples
HD3SS215IZXHR	ACTIVE	NFBGA	ZXH	50	2500	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	HD3SS215I	Samples
HD3SS215IZXHT	ACTIVE	NFBGA	ZXH	50	250	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	HD3SS215I	Samples
HD3SS215RTQR	ACTIVE	QFN	RTQ	56	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	HD3SS215	Samples
HD3SS215RTQT	ACTIVE	QFN	RTQ	56	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	HD3SS215	Samples
HD3SS215ZXHR	ACTIVE	NFBGA	ZXH	50	2500	RoHS & Green	SNAGCU	Level-3-260C-168 HR	0 to 70	HD3SS215	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

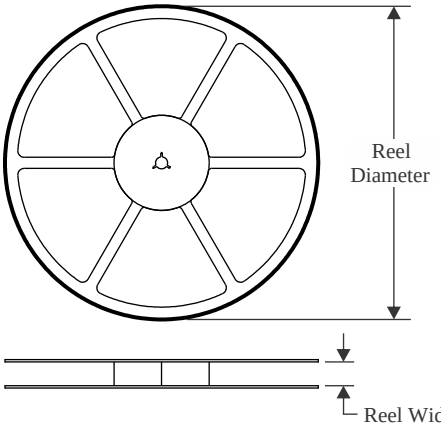
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

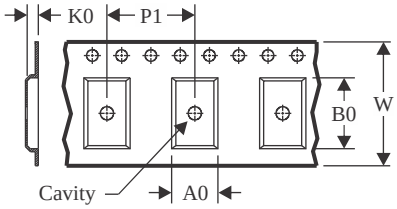
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

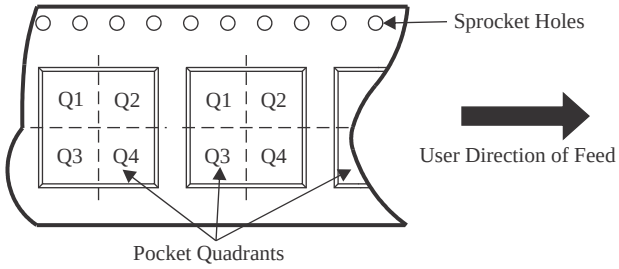


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

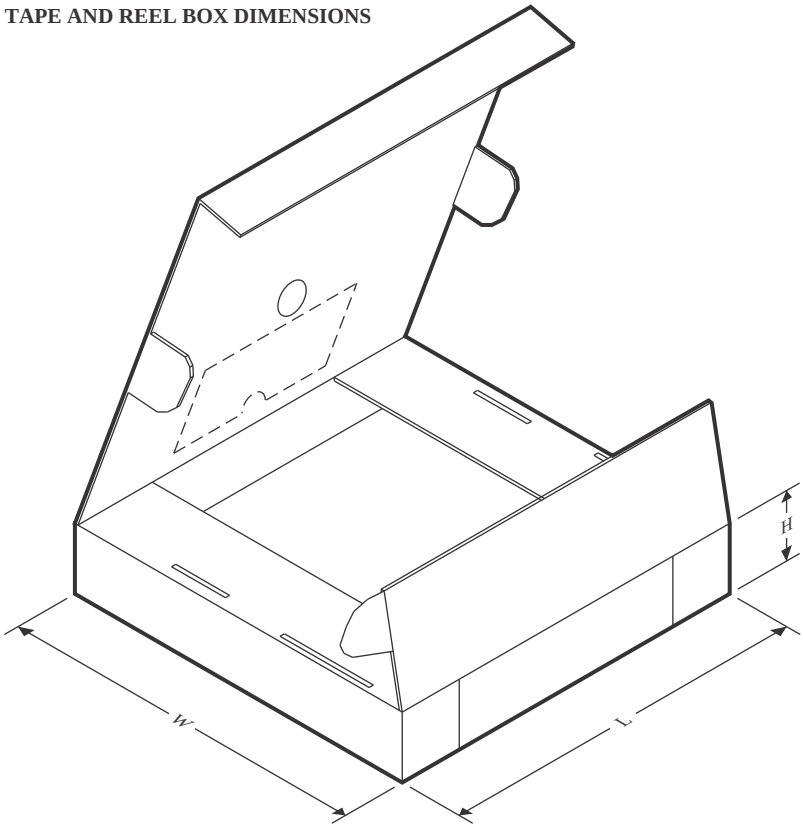
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
HD3SS215IRTQR	QFN	RTQ	56	2000	330.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2
HD3SS215IRTQT	QFN	RTQ	56	250	180.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2
HD3SS215IZXHR	NFBGA	ZXH	50	2500	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q1
HD3SS215IZXHT	NFBGA	ZXH	50	250	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q1
HD3SS215RTQR	QFN	RTQ	56	2000	330.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2
HD3SS215RTQT	QFN	RTQ	56	250	180.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2
HD3SS215ZXHR	NFBGA	ZXH	50	2500	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

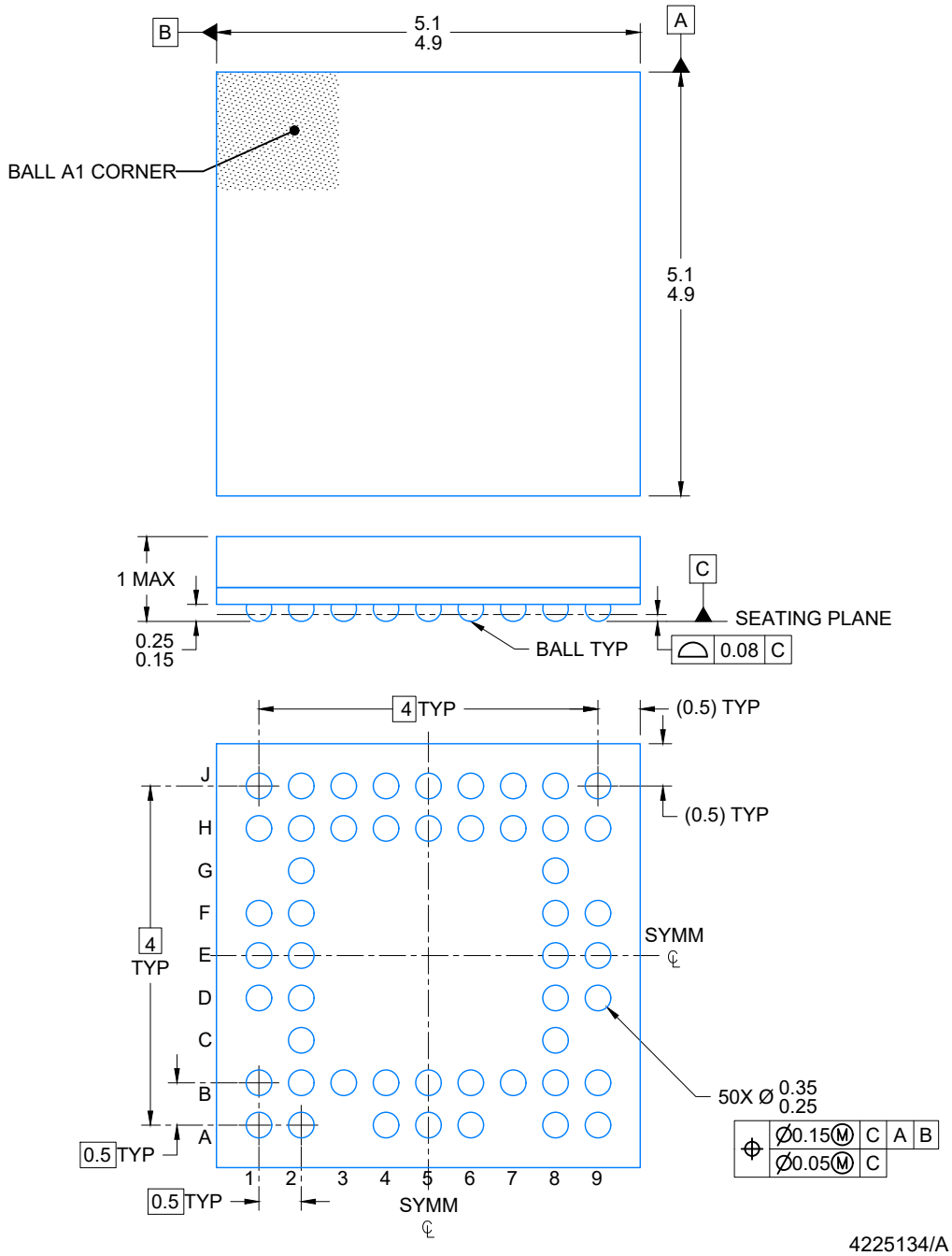
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
HD3SS215IRTQR	QFN	RTQ	56	2000	367.0	367.0	38.0
HD3SS215IRTQT	QFN	RTQ	56	250	210.0	185.0	35.0
HD3SS215IZXHR	NFBGA	ZXH	50	2500	336.6	336.6	31.8
HD3SS215IZXHT	NFBGA	ZXH	50	250	336.6	336.6	31.8
HD3SS215RTQR	QFN	RTQ	56	2000	367.0	367.0	38.0
HD3SS215RTQT	QFN	RTQ	56	250	210.0	185.0	35.0
HD3SS215ZXHR	NFBGA	ZXH	50	2500	336.6	336.6	31.8

PACKAGE OUTLINE

ZXH0050A

NFBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



NOTES:

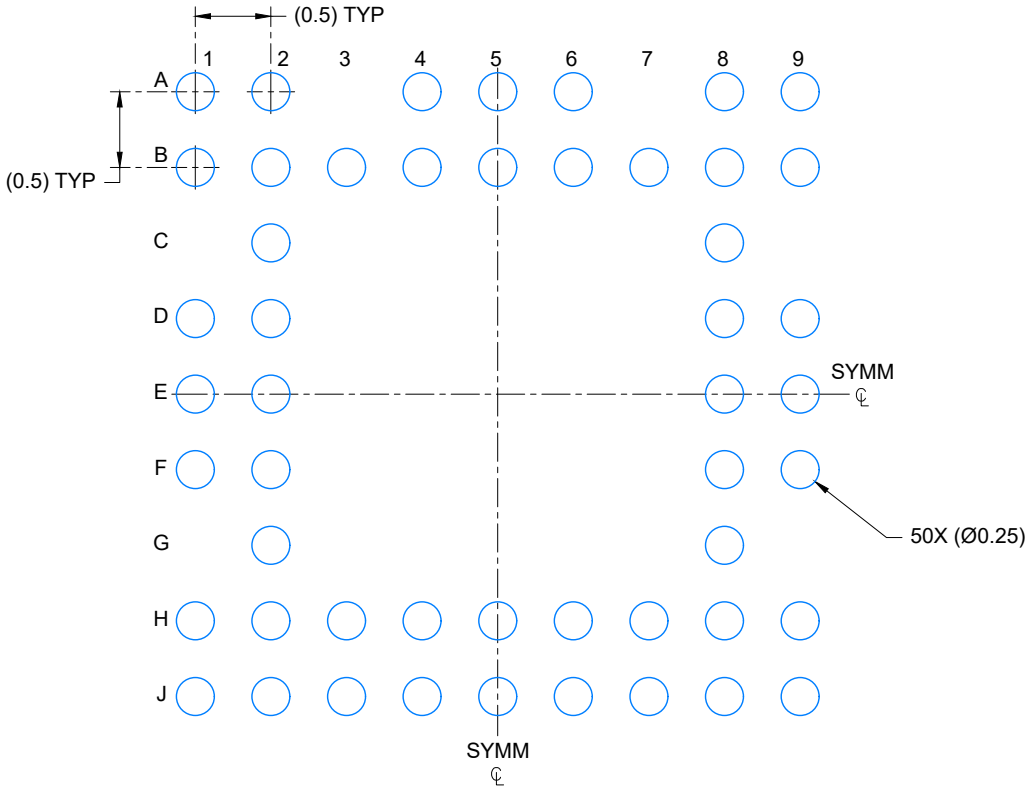
NanoFree is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

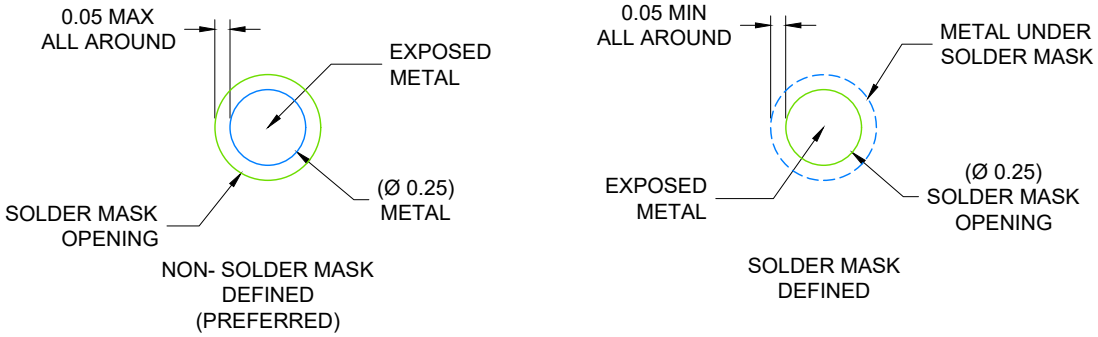
EXAMPLE BOARD LAYOUT

NFBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE: 20X

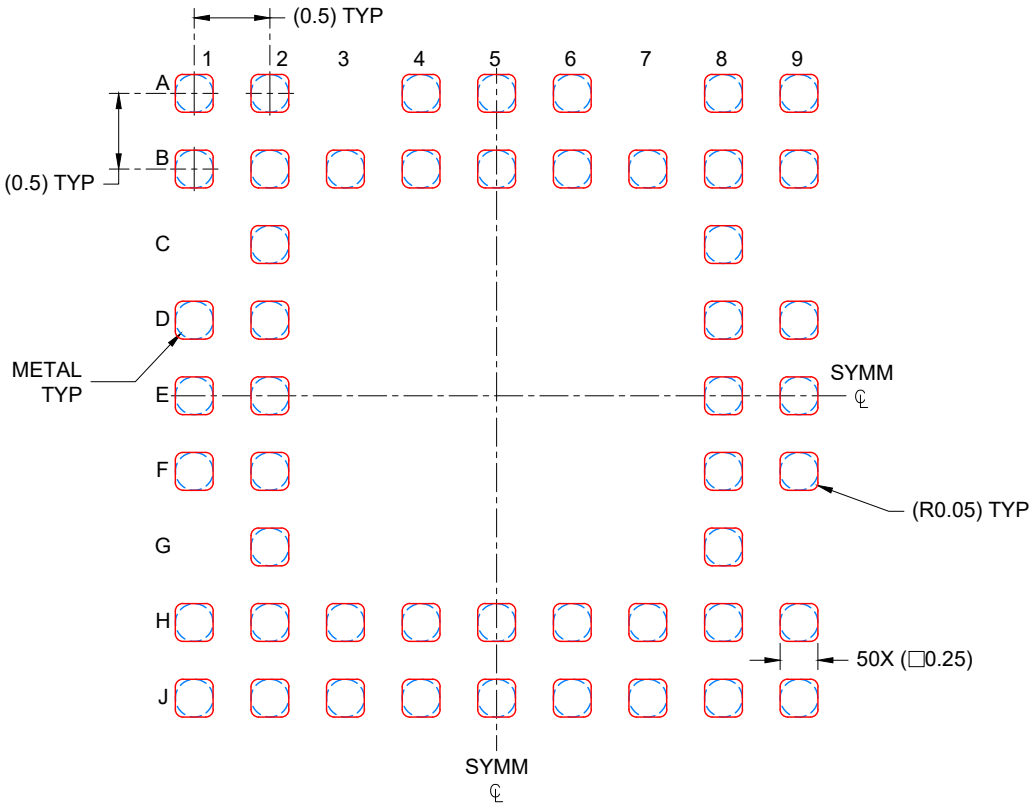


SOLDER MASK DETAILS
NOT TO SCALE

4225134/A 08/2019

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL
SCALE: 20X

4225134/A 08/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

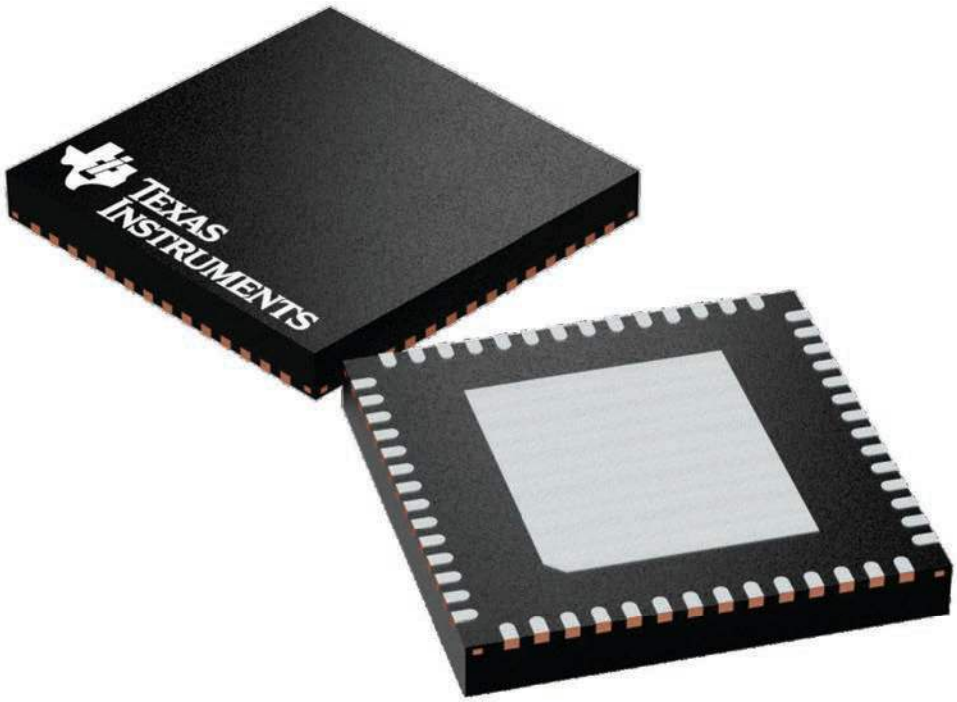
GENERIC PACKAGE VIEW

RTQ 56

VQFN - 1 mm max height

8 x 8, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

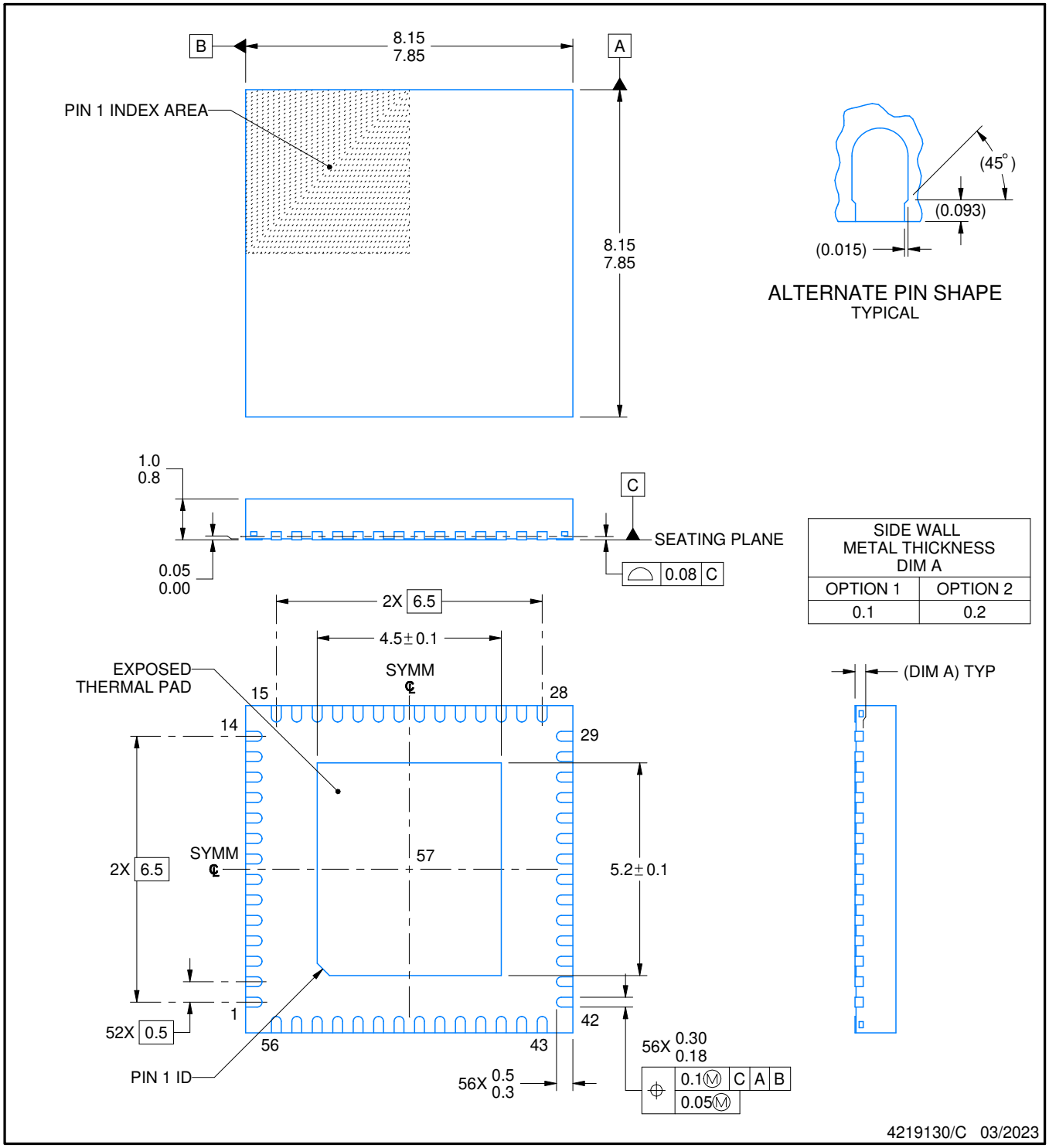
4224653/A

RTQ0056B

PACKAGE OUTLINE

VQFN - 1 mm max height

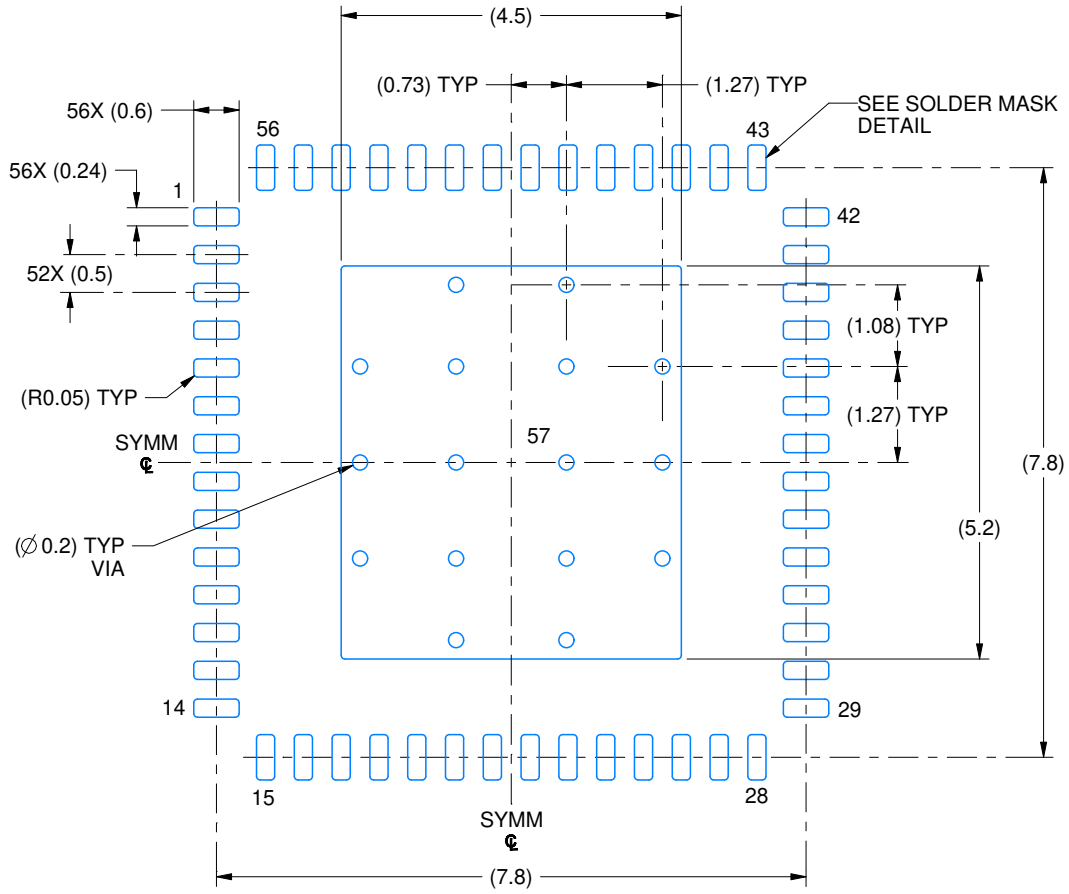
PLASTIC QUAD FLATPACK - NO LEAD



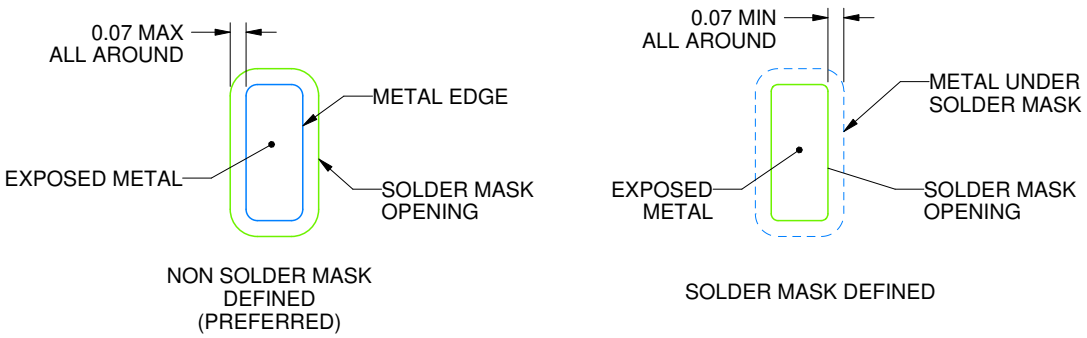
SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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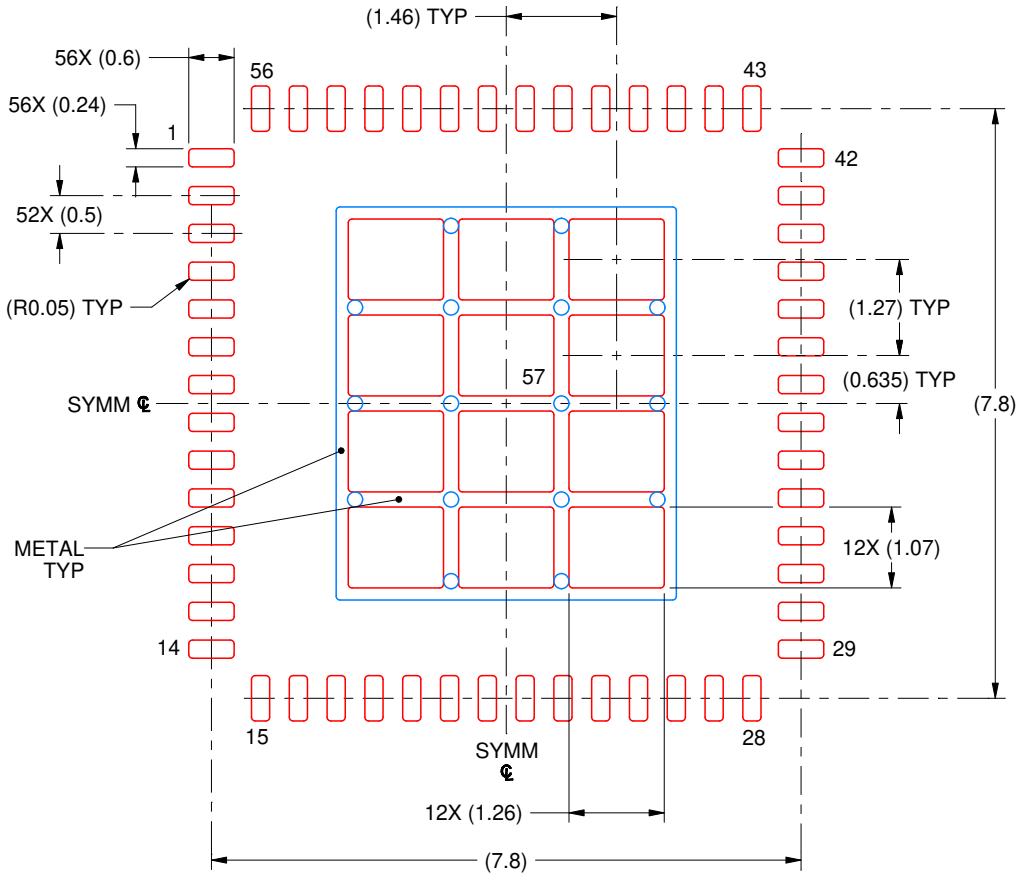
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 57
69% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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