# TPS65086x Evaluation Module

This user's guide describes the characteristics, operation, and use of the TPS65086x evaluation module (EVM). The TPS65086x EVM is a prototyping platform for evaluating the performance of the TPS65086x power management device. The EVM will require modification of the inductors, capacitors, ILIM resistors, and input sources in order to operate optimally for a given use case.

**Contents**



**List of Figures**

## List of Tables

# 1 Introduction

The TPS65086x is a highly integrated power management solution for multi-core processors, FPGAs and other System on Chips (SoCs).

Features of the TPS65086x include:

- Three Variable-Output Voltage Step-Down Controllers
  - Wide $V_{IN}$ range from 5 V to 21 V
  - Scalable output current using external FETs with external current limit resistors at ILIMx pins
  - $I^2C$ DVS Control (0.41 V to 1.67 V in 10-mV steps, 1 V to 3.575 V in 25-mV steps)
- Three variable-output voltage synchronous step-down converters
  - $V_{IN}$ range from 3.0 V to 5.5 V
  - Up to 3 A of output current
  - $I^2C$ DVS control from 0.425 V to 3.575 V in 25-mV steps
- Three LDO regulators with $I^2C$-adjustable-output voltage
  - LDOA1: from 1.35 V to 3.3 V for up to 200 mA of output current
  - LDOA2 and LDOA3: from 0.7 V to 1.5 V for up to 600 mA of output current
- VTT LDO for DDR3 and DDR4 memory termination
  - Fixed-output voltage of 0.5 × $V_{BUCK6}$
  - Can sink and source output current up to 500 mA
- Three load switches with slew-rate control
  - Up to 300 mA of output current with voltage drop less than 1.5% of nominal input voltage
  - $R_{DSON}$ < 96 mΩ at input voltage of 1.8 V
- Built-in flexibility and configurability
  - Six input pins (CTL1–CTL6) configurable to Enable or Sleep Mode (CTL3 and CTL6) of any selected rails
  - Four output pins configurable to power good of any selected rails or controllable by $I^2C$
  - Open-drain interrupt output pin
- $I^2C$ interface (Device Address 0x5E) supports standard mode (100 kHz), fast mode (400 kHz), and fast mode plus (1 MHz)
- 64-Pin, single-row, 0.4-mm pitch QFN package

**NOTE:** The TPS65086x EVM is designed to demonstrate some of the potential uses of the TPS65086x family. The EVM has more limitations than the TPS65086x device.

The limitations of the EVM follow:

- The FET for BUCK1 and BUCK6, the CSD87381P, has a maximum power dissipation of 4 W. The FET for BUCK2, the CSD87588N, has a maximum power dissipation of 6 W.
  - Care must be taken to ensure that this power dissipation limit is not exceeded
  - Higher input voltages reduce system efficiency so less output current can be provided
  - If the power dissipation limit is exceeded, the most common symptom is a short between the VIN and VOUT nodes
  - Replacing the FET and any non-ceramic capacitors should fix the issue

  .
- Inductor values are optimized for the given parameters with a 12-V input for controllers, 5-V input for converters:
  - BUCK1 - 470 nH - 1.05 V - 7 A (matches default)
  - BUCK2 - 220 nH - 1 V - 20 A (default voltage of 3.3 V is not optimized)
  - BUCK3 - 470 nH - 2.5 V - 3 A (matches default)

  - BUCK4 - 470 nH - 2.8 V - 3 A (matches default)
  - BUCK5 - 470 nH - 1.8 V - 3 A (matches default)
  - BUCK6 - 470 nH - 1.5 V - 10 A (matches default)
- BUCK2 has tantalum capacitors in order to demonstrate that the DCAP2 architecture can support these. An all ceramic solution would work as well here.
- BUCK1 - BUCK5 and LDOA2/A3 sleep state values are all assigned to CTL3. Sleep states are disabled for BUCK1 - BUCK3 by default, enabled for the remainder. They can be enabled or disabled by writing to the BUCKx_SLP_EN bits. Once enabled, if CTL3 is low, the BUCKx_SLP_VID group will determine the output voltage on these regulators. If CTL3 is high, the BUCKx_VID group will determine te output voltage on these regulators. BUCK6 is similarly assigned to CTL6 and the sleep state is enabled by default.

Finally, the sequence and rail assignments can be seen in Figure 1. Note that the CTL pins do not need to be switched in any particular order.

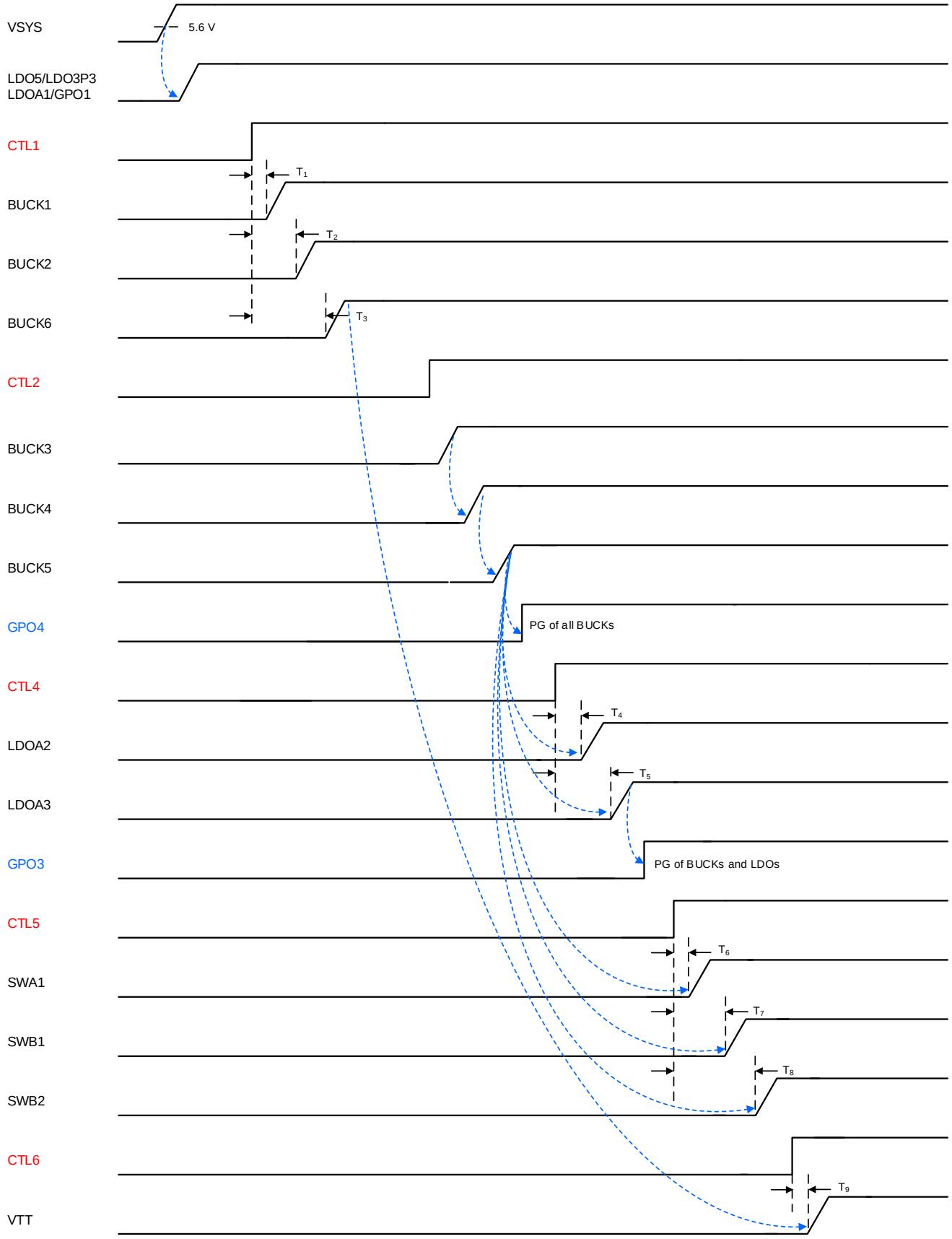


**Figure 1. TPS650860 Power Up Sequencing**

# 2 Requirements

## 2.1 Software

The EVM will power-up and operate without use of software. A GUI is supplied to provide a simple way to communicate to the device via $I^2C$. The GUI can be downloaded from:
http://www.ti.com/tool/IPG-UI

The EVM has a built-in USB2ANY module utilizing an MSP430. The GUI uses this to communicate with the device.

## 2.2 Host Computer

A computer with an available USB port is required to make use of the EVM software. The EVM software runs on the computer and communicates with the EVM via a USB-A to micro-B cable.

## 2.3 Power Supply

A DC power supply capable of delivering at least 5.6 V and 1 A is required to power on the EVM. If loading the EVM, a power supply with a 10 A limit or higher is recommended.

### 2.4 EVM Kit

The EVM kit contains the following items:

- TPS65086x HVL116A evaluation board
- USB A to micro-B cable

## 3 Terminal Block Descriptions

The EVM features 14 terminal blocks around the perimeter of the EVM. These are used for providing VSYS (J1) and loading the outputs. Each terminal block is labeled with the input or output on one side and GND on the other. Each terminal block also has a pair of test points for sense line probing.

## 4 Test Point Descriptions

Numerous test points are provided for sensing voltages on the EVM. The CTL1–6 test points also provide a way to override the on-board switches, when desired. Note that to override the switches, they must be in the 'OFF' position (not shorted to GND).

**Table 1. Test Points(1)**

| Test Point | Description |
|---|---|
| CTL1 | Controller Enable |
| CTL2 | Converter Enable |
| CTL3 | Sleep |
| CTL4 | LDO Enable |
| CTL5 | Load Switch Enable |
| CTL6 | VTT Enable |
| GPO1 | Push-Pull Output (Default '1') |
| GPO2 | Open Drain Output (Default '0') |
| GPO3 | Open Drain Global PGOOD |
| GPO4 | Open Drain BUCK PGOOD |
| V5ANA | External 5-V supply input to internal load switch that connects this pin to LDO5P0 pin. |
| LDO5V | 5-V internal LDO (LDO5P0) sense |
| LDO3P3 | 3.3-V internal LDO sense |
| VREF | Bandgap reference output |
| GND | Connected to GND planes |
| DIG_1P8V | 1.8-V external LDO sense |
| USB_3P3V | 3.3-V external LDO sense for USB2ANY onboard MSP430 |
| BUCK3P3V | 3.3-V external BUCK sense |
| BUCK5V | 5-V external BUCK sense |
| EPGOOD | Power good indicator of external dual controller (requires pull-up to indicate properly) |
| Output Sense+ (Unlabeled) | Each rail has a sense+ line connected to the central output cap |
| Output Sense– (Unlabeled) | Each rail has a sense– line connected to the central output cap |
| Input Sense+ (TP1) | VSYS sense+ line connected to input cap of PMIC |
| Input Sense– (TP2) | VSYS sense– line connected to input cap of PMIC |

(1) Test points are not designed to carry current. They are intended for measuring voltage.

## 5 Header Descriptions

There are 7 sets of headers which are used to provide greater access to several signals.

**Table 2. Headers**

| Jumper | Description | Jumper Default Position |
|---|---|---|
| **J21** | Option to bypass the on-board 5-V external buck for the input to BUCK3, BUCK4, BUCK5, and V5ANA. 4 GND pins provided here as well. | VIN_BUCK345_ANA connected to BUCK5V with two jumpers to accommodate high current |
| **J22** | Option to bypass LDO5V for the input to DRV5V_2_A1 and DRV5V_1_6 | VIN_DRV connected to LDO5V |
| **J23** | Option to bypass the on-board 3.3-V external buck for the input to SWA1. 2 GND pins provided here as well. | VIN_SWA1 connected to BUCK3P3V |
| **J24** | Option to bypass BUCKX_1P8V (1.8 V) for the input to LDOA2_A3 | VIN_LDOA2_A3 connected to BUCKX_1P8V |
| **J25** | Option to bypass BUCKX_1P8V (1.8 V) for the input to SWB | VIN_SWB connected to BUCKX_1P8V |
| **J33** | SDA, SCL, and GND | Not intended for a jumper |

## 6 Control, GPO, and External VRs

The EVM features a set of DIP switches for controlling CTL1–6 and 6 LEDs for GPO indicators. It also has built-in USB2ANY circuitry which utilizes an on-board MSP430 to enable the GUI to communicate with the device through a USB cable. Finally, it features an on-board TPS51285 device which provides 3.3- and 5-V rails from VSYS for use by BUCK3, BUCK4, BUCK5, V5ANA, and SWA1. Pads exist for the addition of Samtec HSEC8-110-01-S-DV-A vertical edge rate card sockets.

- For the CTL switches, S1, the “OFF” position is an open circuit and the CTL signal is pulled up to the corresponding rail. The “ON” position forces the CTL signal to GND.
- The LED order is D6, D1, D4, D5, D2, D3 with the resulting signal order from left to right being: USB, GPO1, GPO4, IRQB, GPO2, GPO3.

**Table 3. Other Connectors**

| Designator | Description |
|---|---|
| **S1** | In order from left to write, the switches are for: CTL1 - CTL6. Note: the “ON” (up) position shorts the CTL signals to GND. As a result, to enable an active high signal, the switch should be set to the “OFF” (down) position. |
| **D6** | Indicator light for successful USB connection. |
| **D1** | GPO1 |
| **D2** | GPO2 |
| **D3** | GPO3 |
| **D4** | GPO4 |
| **D5** | Inverted IRQB status indicator (since IRQB is active low) |

# 7 Setup

The general block diagram for the HVL116A EVM can be seen in Figure 2. Jumpers and shunt resistors can be used to reroute signals as needed.

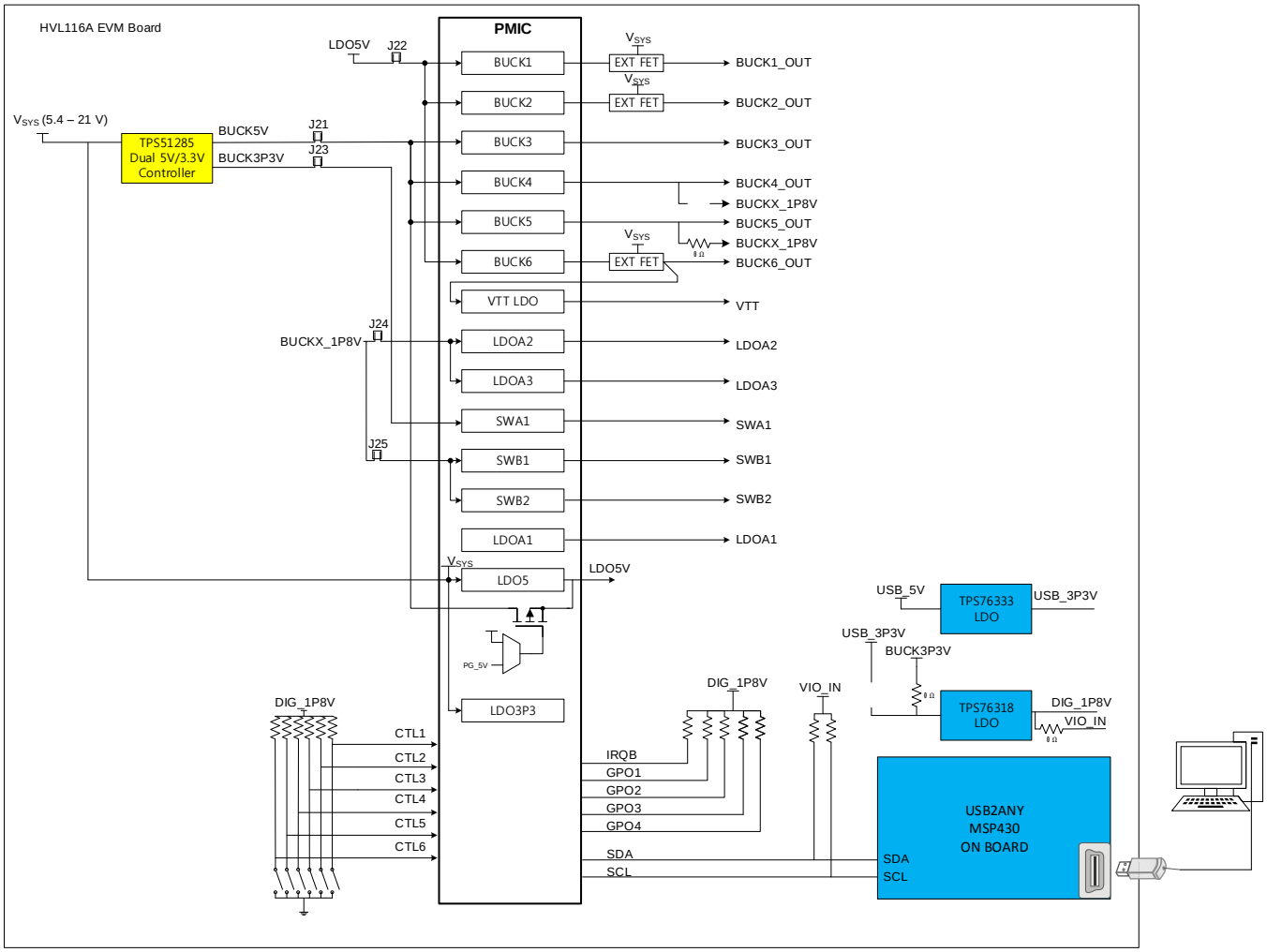


**Figure 2. HVL116A Block Diagram**

Figure 3 is an example setup for using the TPS65086x EVM:

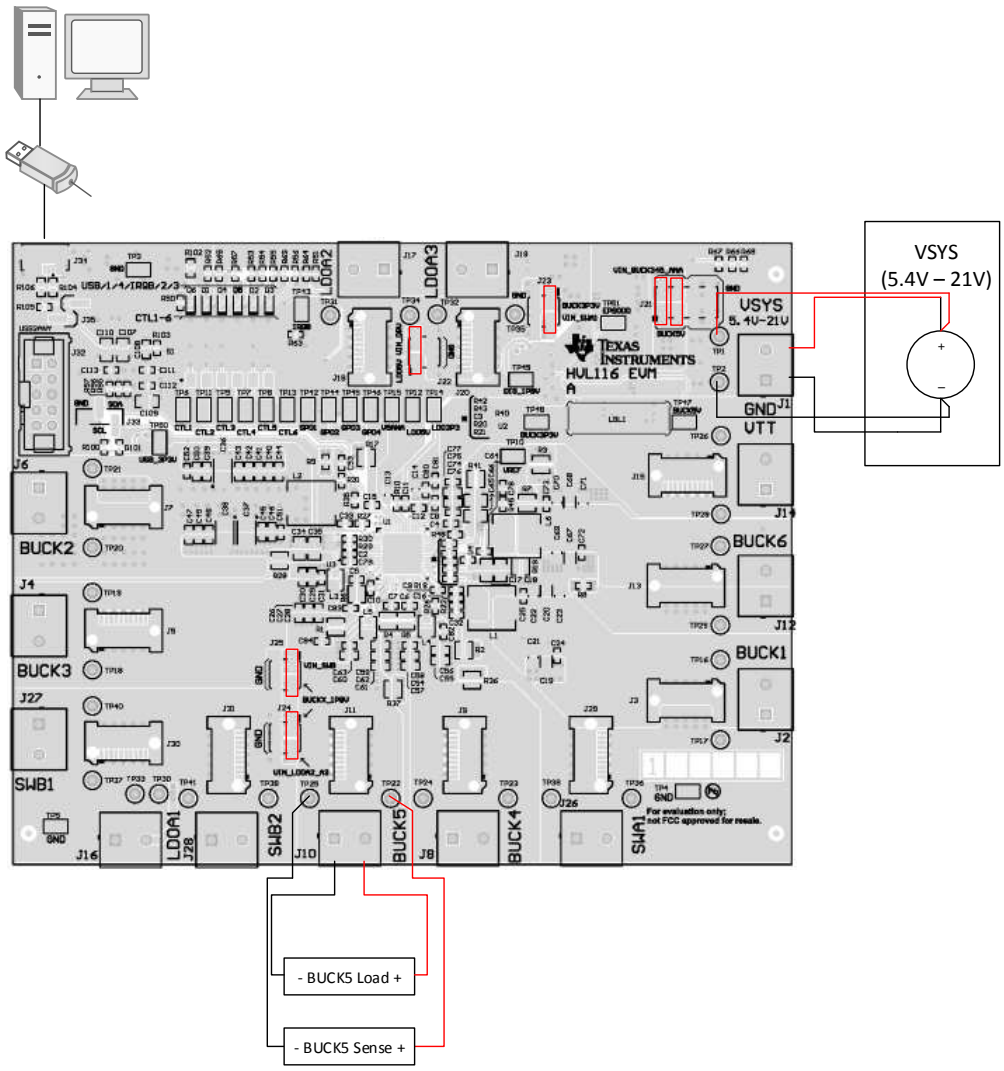


**Figure 3. TPS65086x EVM Setup**

For the default TPS650860 part, the GPO1 LED and LDOA1 should turn on as VSYS is applied, regardless of the state of the CTL pins. If all CTL pins are low, then no other output power rails will be enabled. As the CTL switches are set to the "OFF" position and the CTL pins are allowed to pullup to DIG_1P8V, the other rails are enabled based on the sequence in the datasheet.

# 8 Software

## 8.1 Software Installation Instruction

A GUI is supplied to provide a simple way to communicate to the device via $I^2C$. The GUI can be downloaded from:
http://www.ti.com/tool/IPG-UI

Information on the installation of the IPG-UI can be found in the *IPG-UI User's Guide* (SLVUAH9)

## 8.2 Using the TPS65086x GUI

Detailed information on the usage of the IPG-UI can also be found in the *IPG-UI User's Guide* (SLVUAH9). A brief overview is provided here for reference.

The proper device must first be selected from the "Select Devices" drop-down menu.

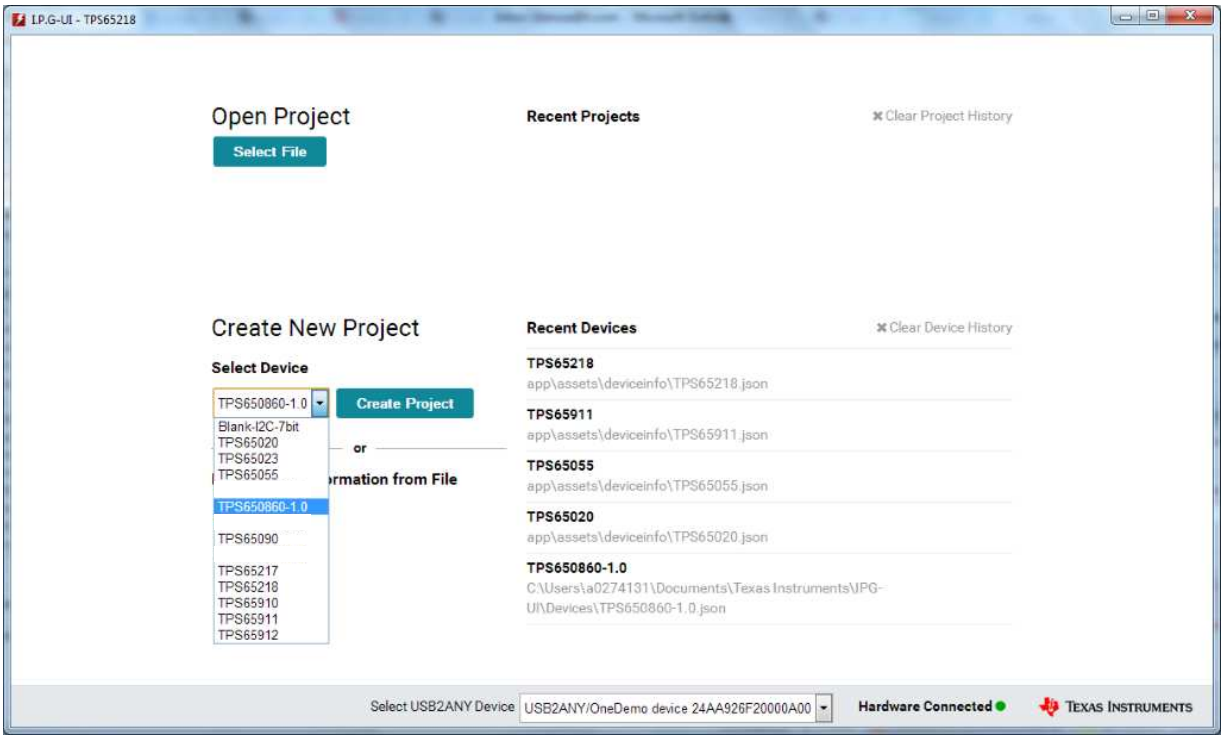


**Figure 4. GUI Front Page**

From there, the next screen is the device introduction page, which includes a brief overview as well as the functional block diagram for the device.

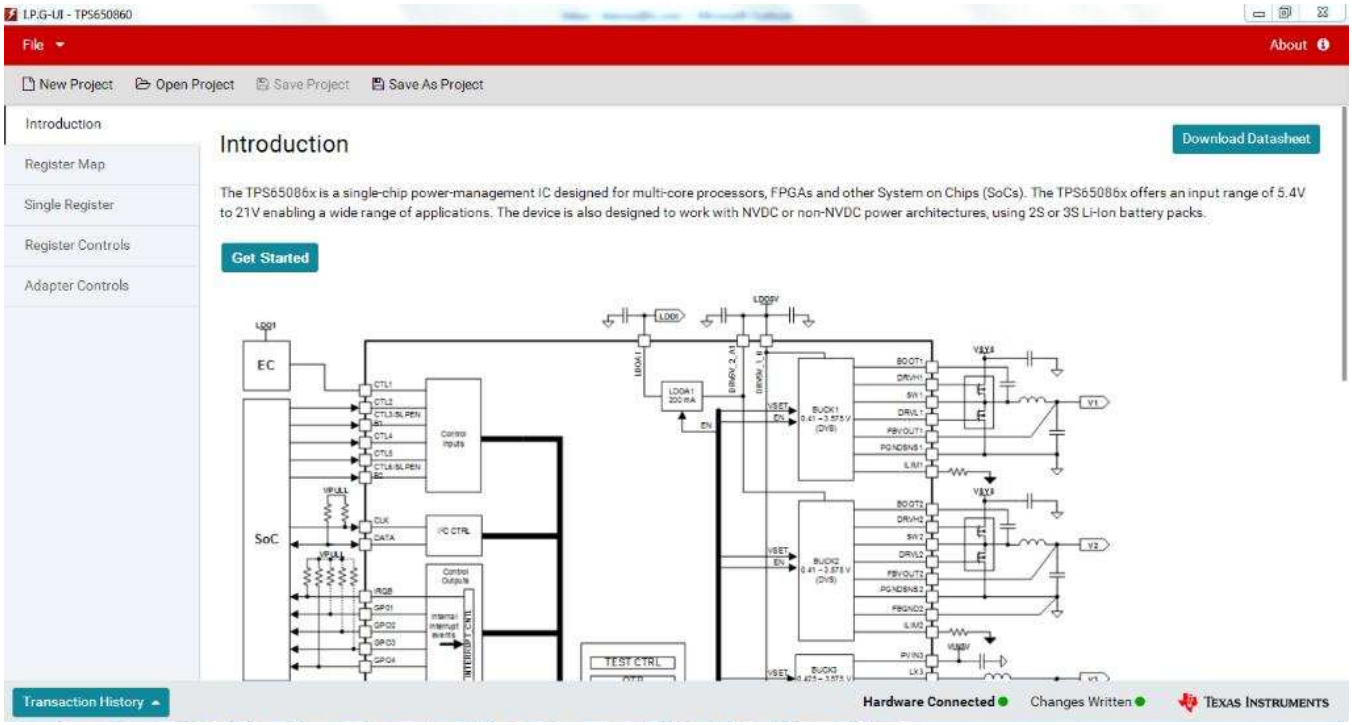


**Figure 5. GUI Device Introduction**

Finally, clicking on "Get Started" or on "Register Map" takes you to the I²C controls for the device sorted by register address.

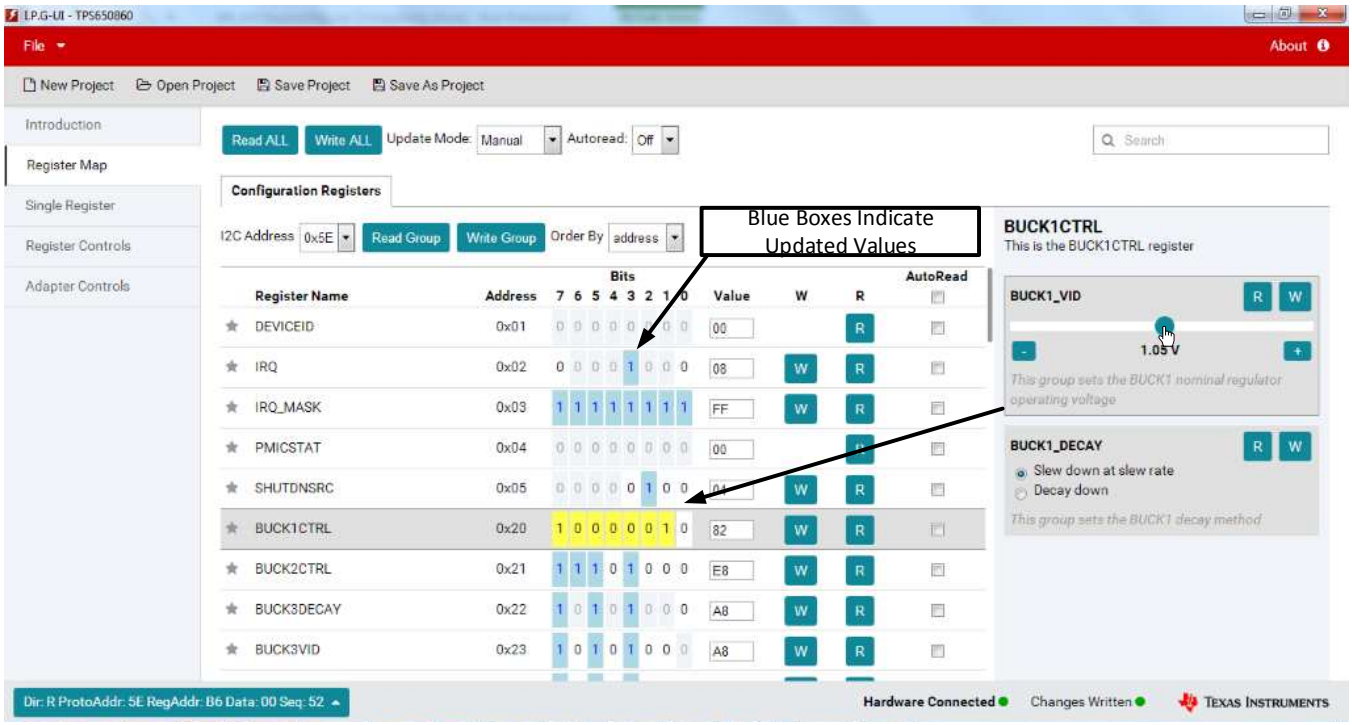


**Figure 6. GUI Register Map**

Alternatively, the part can be controlled using the "Register Controls" tab to sort by functionality rather than by I²C address location.

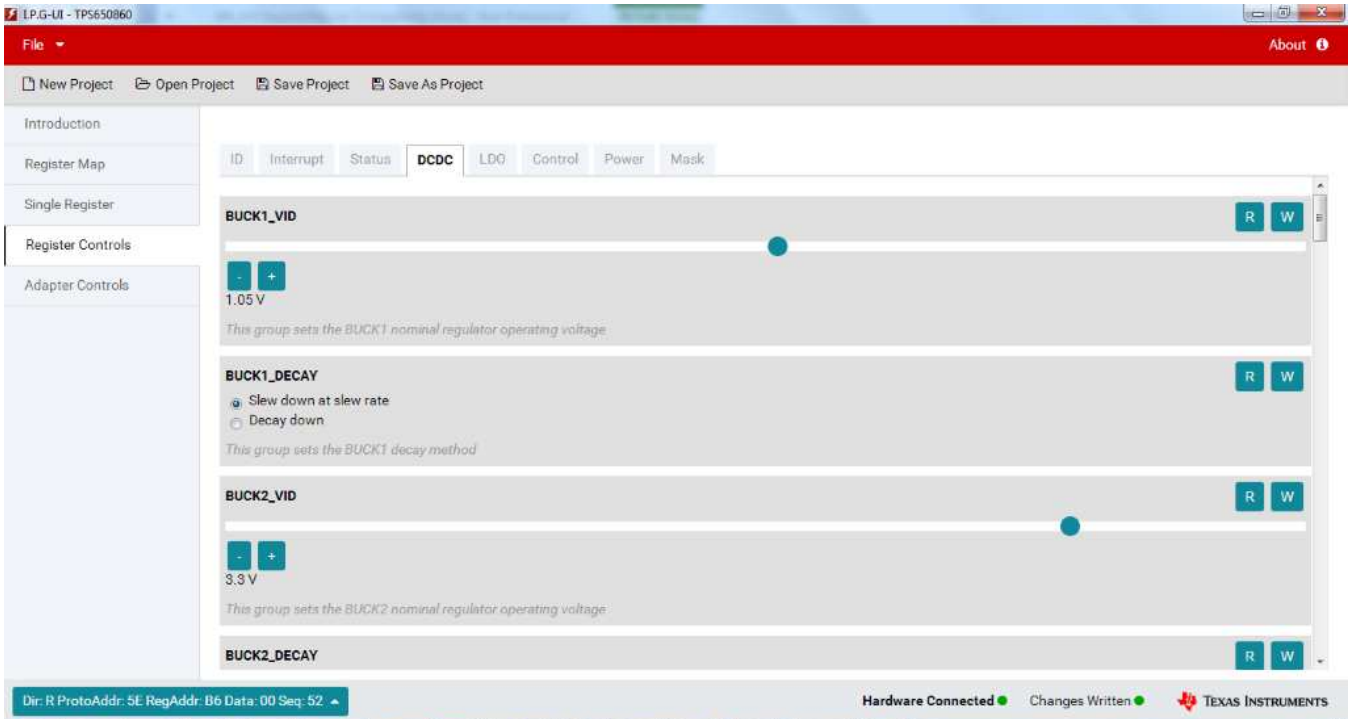


**Figure 7. GUI Register Controls**

With this information, it is possible to begin evaluating the TPS65086x device.

## 9 Sample Test Procedure

For reference, a sample procedure for measuring BUCK1 efficiency is described. A similar approach can be utilized for the other rails.

First, the relevant inputs need to be identified. For BUCK1, there are four device level inputs which each have a 0-Ω resistor which can be removed to isolate them:

1. Input to VSYS pin (R10): Powers up the TPS650860 and is used for internal LDOs to power the digital.
2. Input to V5ANA pin (R17): Powers the converters as well as a power path input to the LDO5P0 output pin.
3. Input to the DRV5V_1_6 and DRV5V_2_A1 pins (R8 and R9): Powers the controller drivers and LDOA1.
4. Input to the FET (R19 for BUCK1): Powers the output stage.

In order to measure accurate system level efficiency, all of the above resistors should be removed and external wires (using a 4-wire approach with voltage sense on the input capacitor) added to the board.

For quicker measurements where the accuracy is not as essential, there is a shorter alternative. First, the VSYS pin power draw (1 mA typical) is small and may be neglected if focusing on high load conditions. V5ANA can be powered from the VIN_BUCK345_ANA header and the DRV5V_x_x can be powered from the VIN_DRV header. Finally, the 2-mΩ sense resistor on the FET inputs can be used to sense the input current and a wire can be added to the input capacitor to measure the input voltage. Load should be applied through the screw terminals and output voltage should be sensed using the test points next to the screw terminals. Efficiency should be determined based on the measured output power and input power, not on the assumed values due to IR drops in the wires.

To enable only a single rail, all CTL pins should be low (S1 switches to "ON" - short to GND) and the BUCKx_EN bit located in the I2C_RAIL_ENx register (address 0xA0 and 0xA1) should be set to '1'. For BUCK1 - BUCK3, the voltage can be changed using the BUCKx_VID groups. For BUCK4 - BUCK 6, the voltage can be changed using the BUCKx_SLP_VID groups unless the BUCKx_SLP_EN is disabled first, in which case the BUCKx_VID groups are used as well.

# 10 Schematics, PCB Layouts, and Bill of Materials

## 10.1 Schematic

Figure 8 through Figure 13 illustrate the HVL116A schematics.

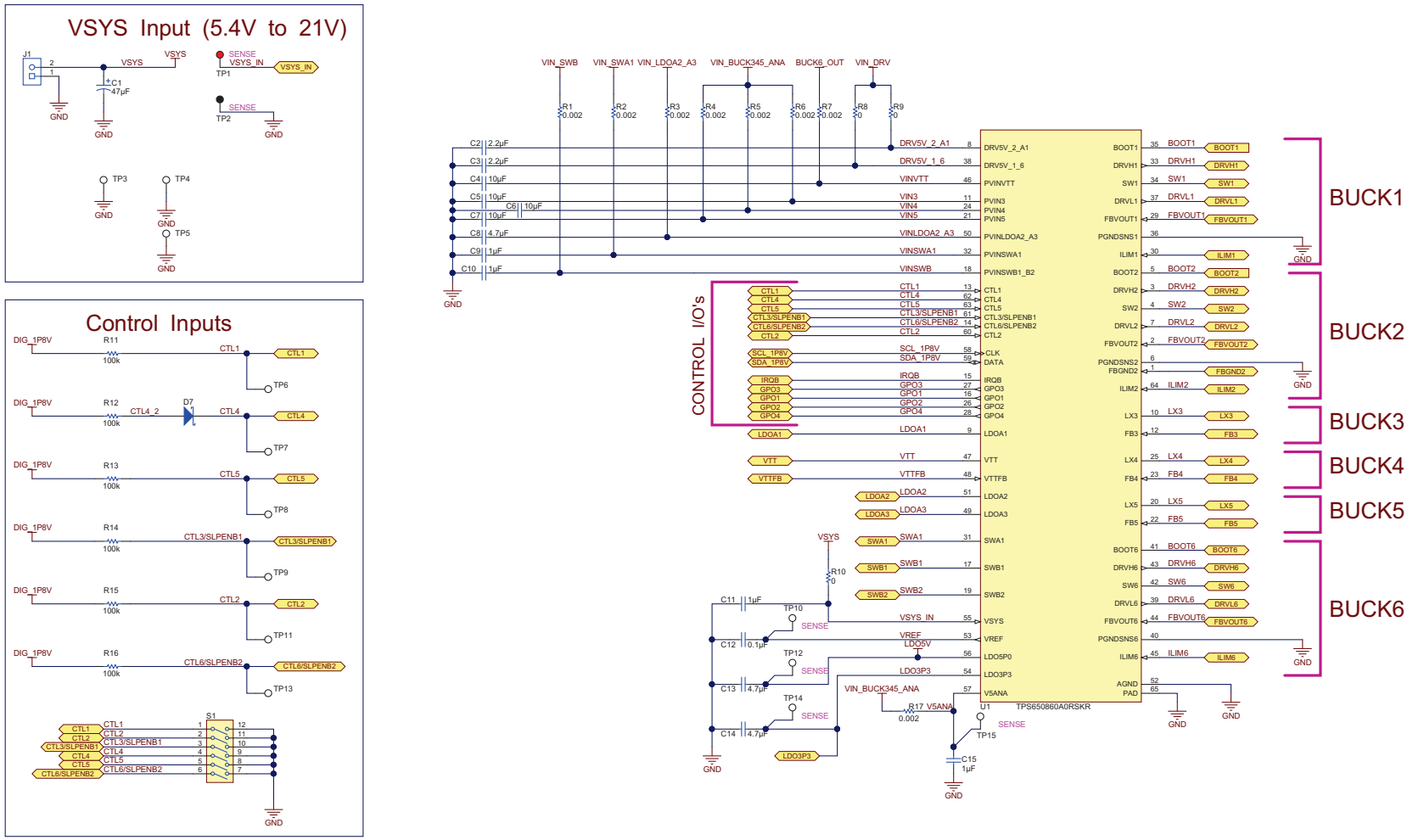


**Figure 8. HVL116A Schematic Page 1**

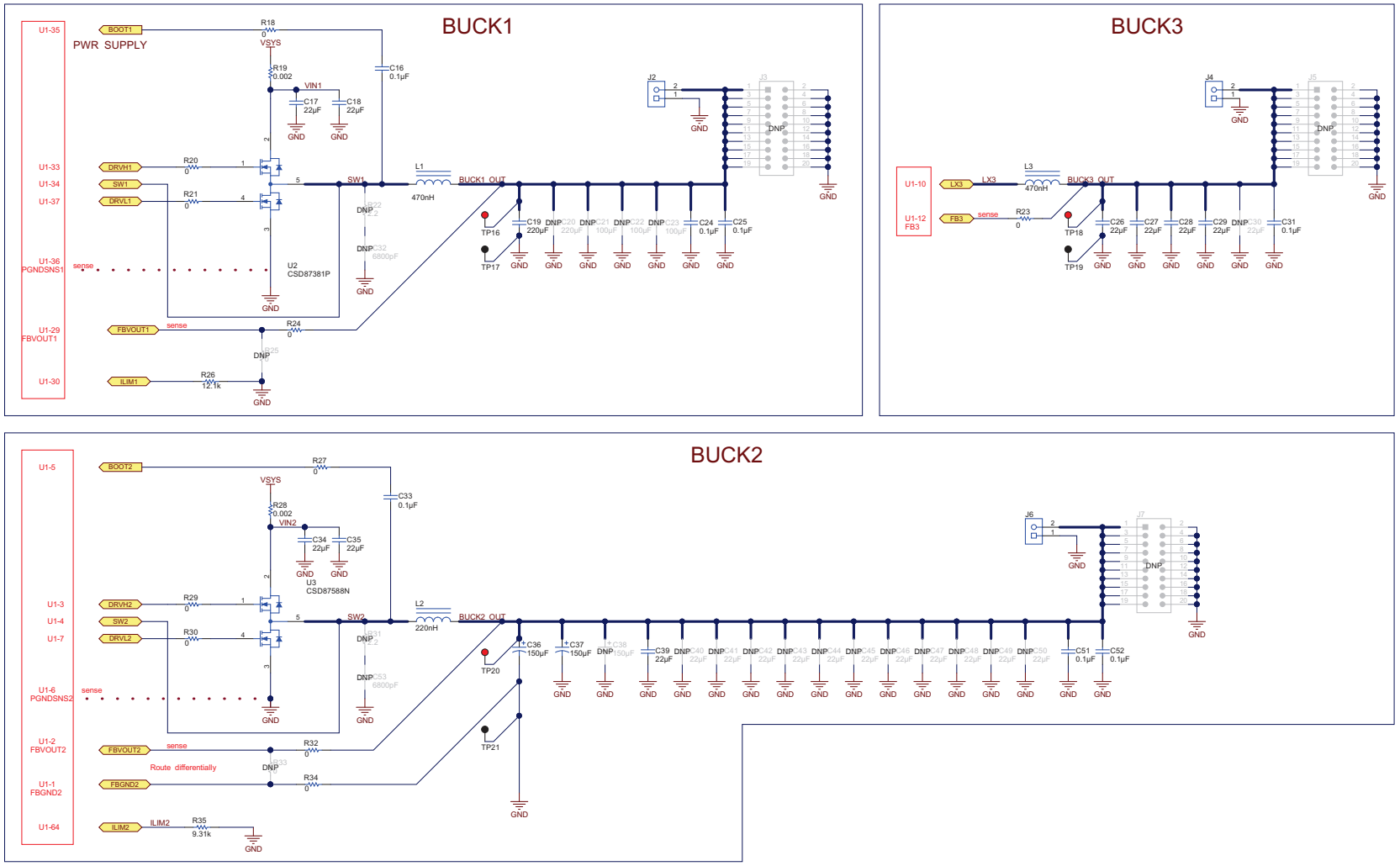


**Figure 9. HVL116A Schematic Page 2**

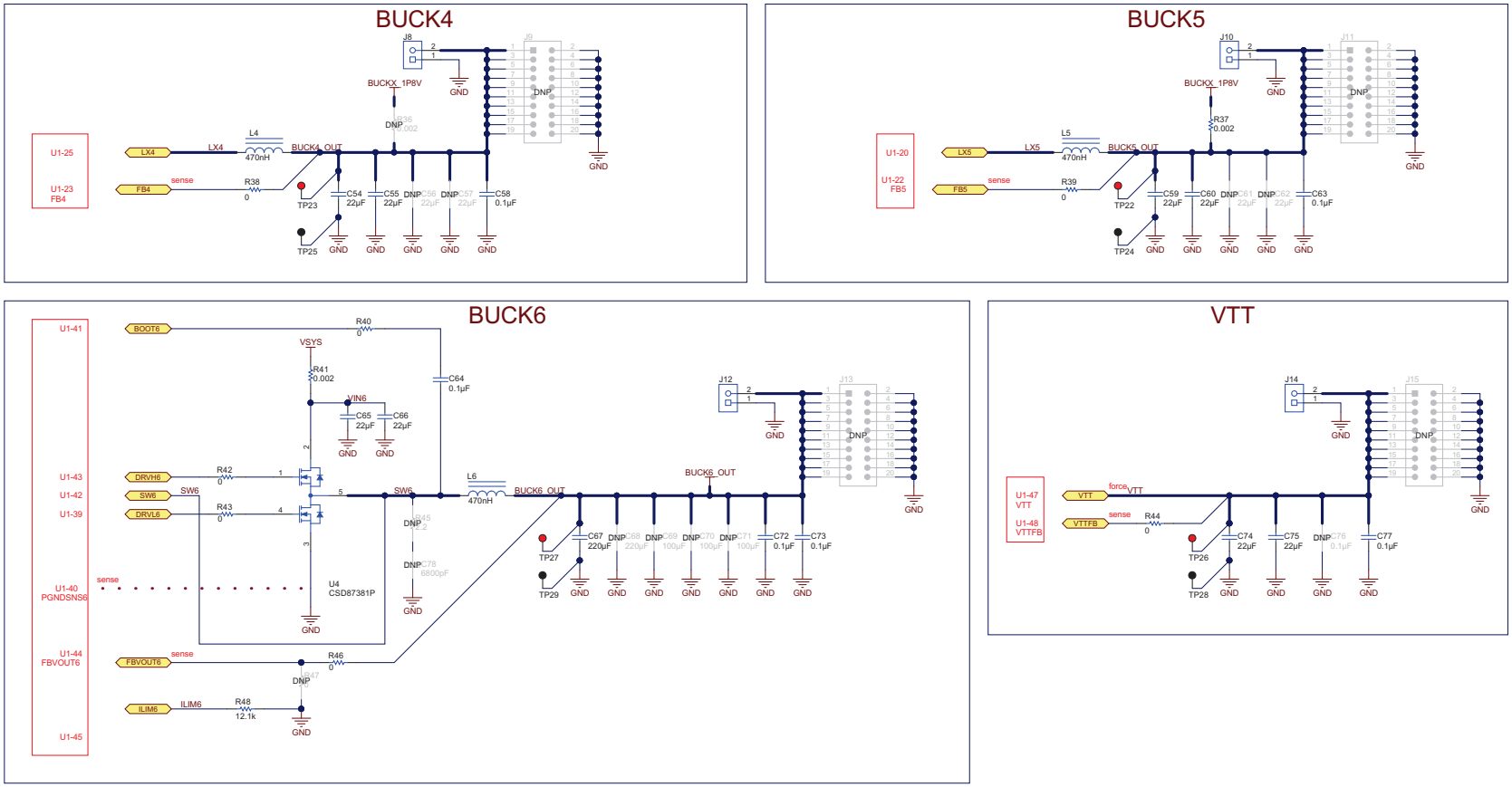


**Figure 10. HVL116A Schematic Page 3**

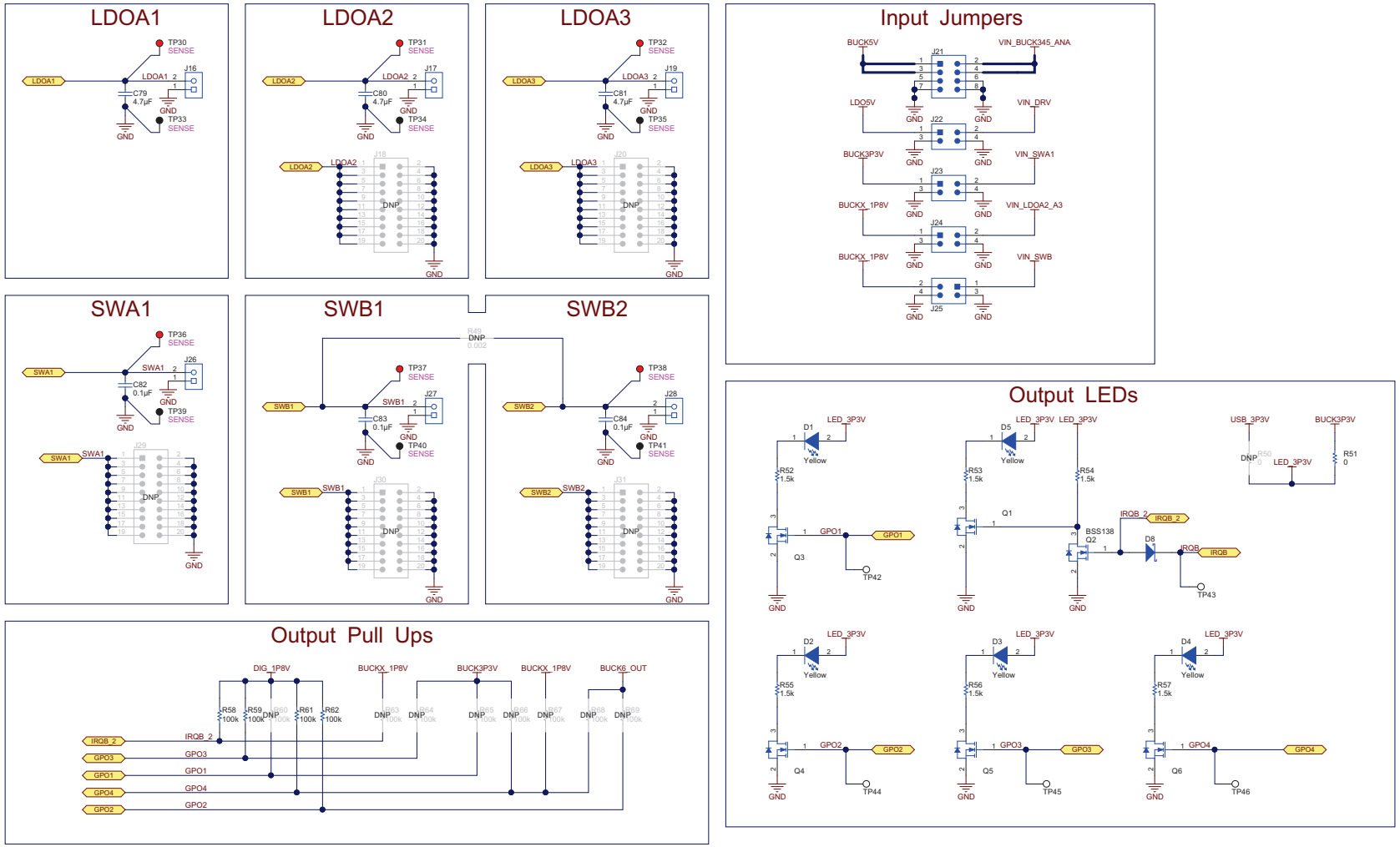


**Figure 11. HVL116A Schematic Page 4**

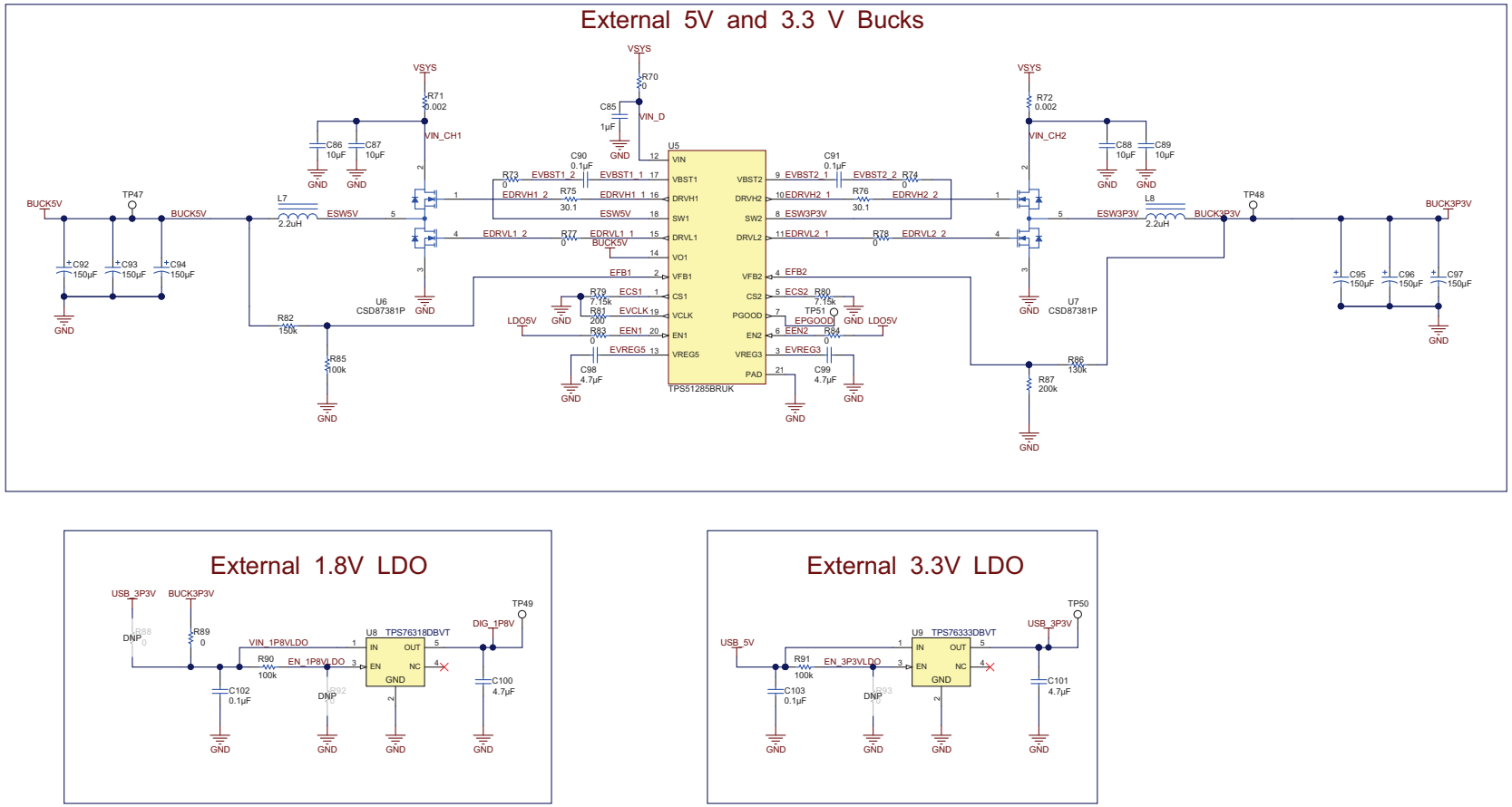


**Figure 12. HVL116A Schematic Page 5**

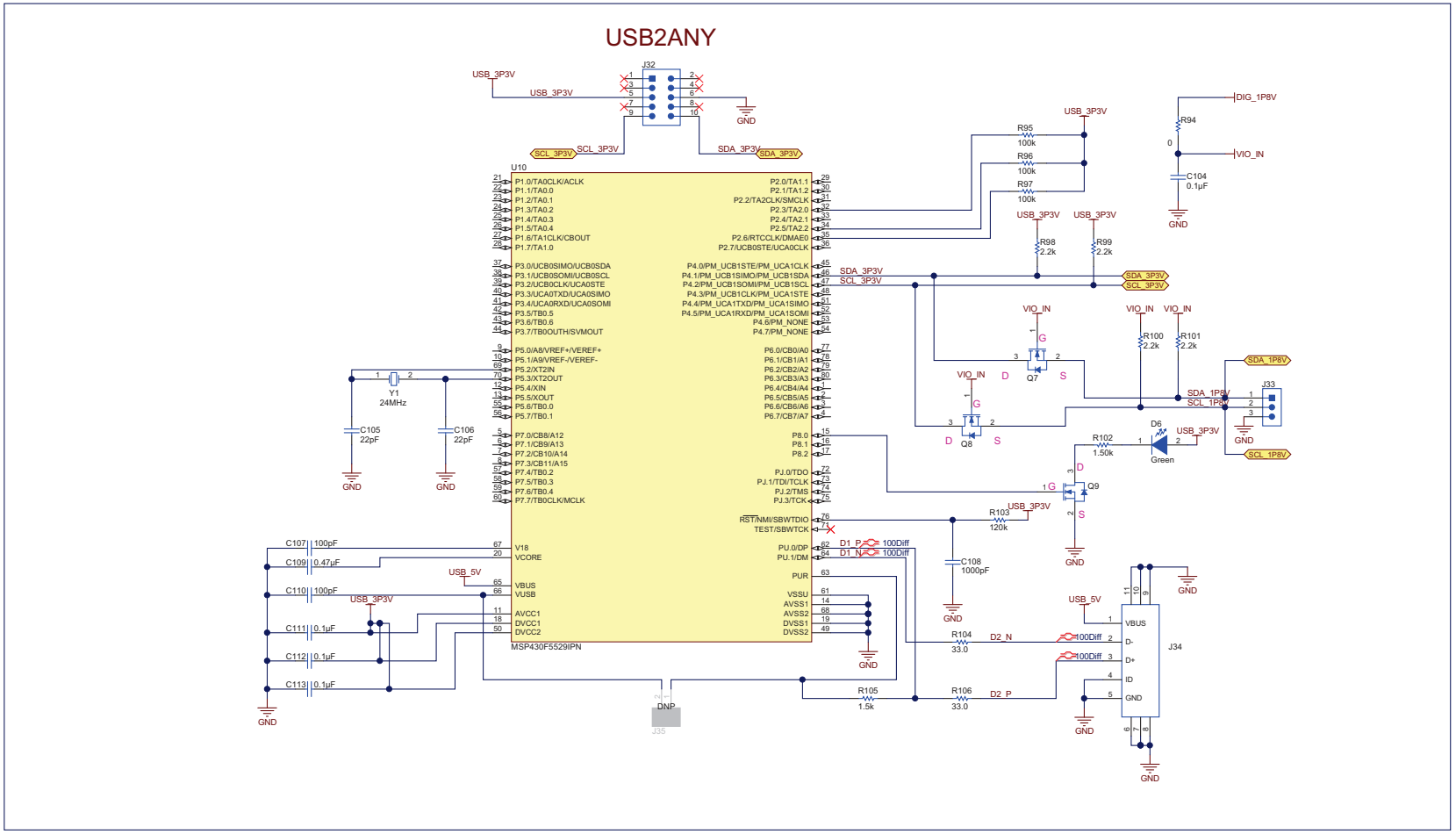


**Figure 13. HVL116A Schematic Page 6**

## 10.2 PCB Layouts

Figure 14 through Figure 25 illustrate the HVL116A PCB layouts.

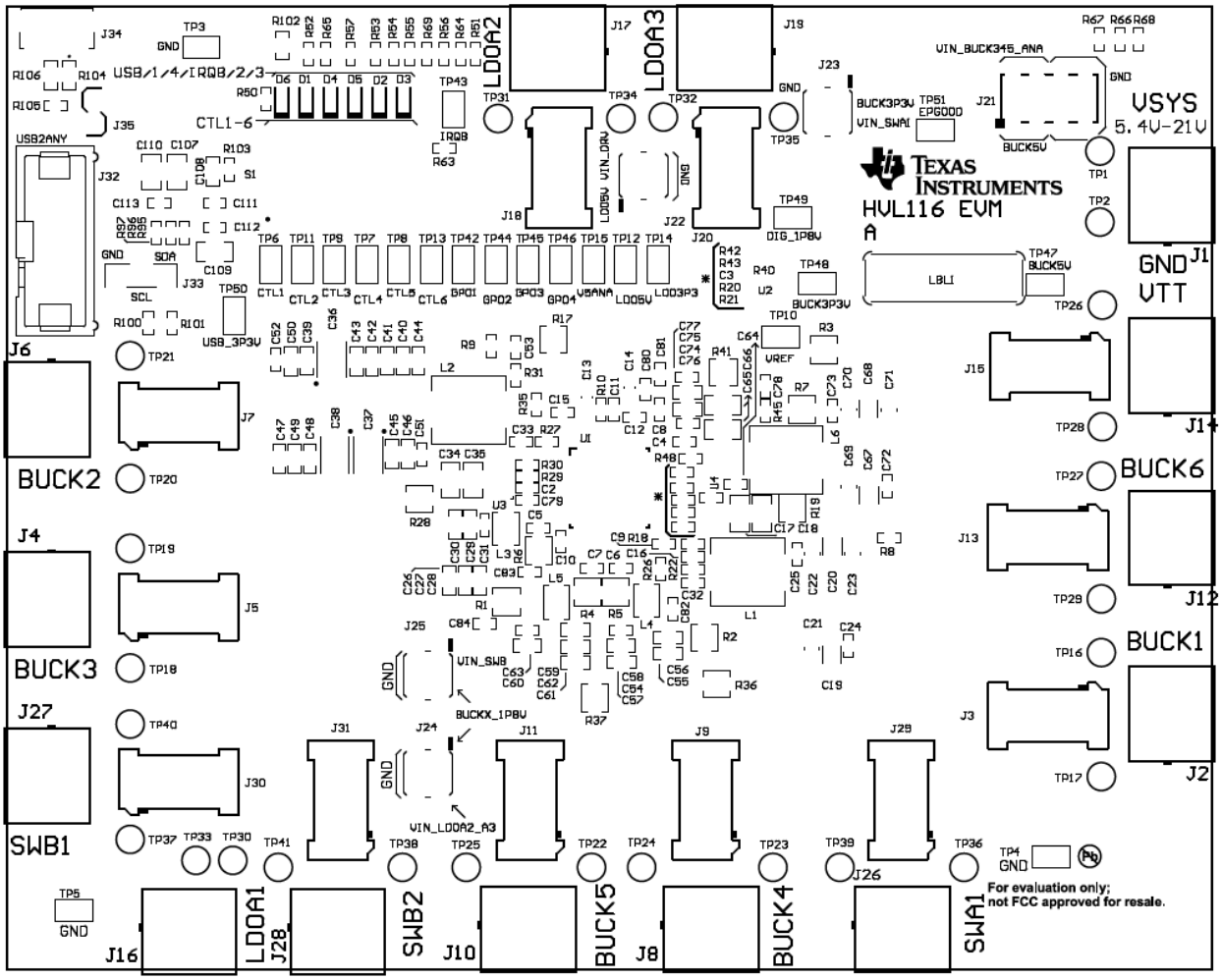


**Figure 14. Top Overlay**

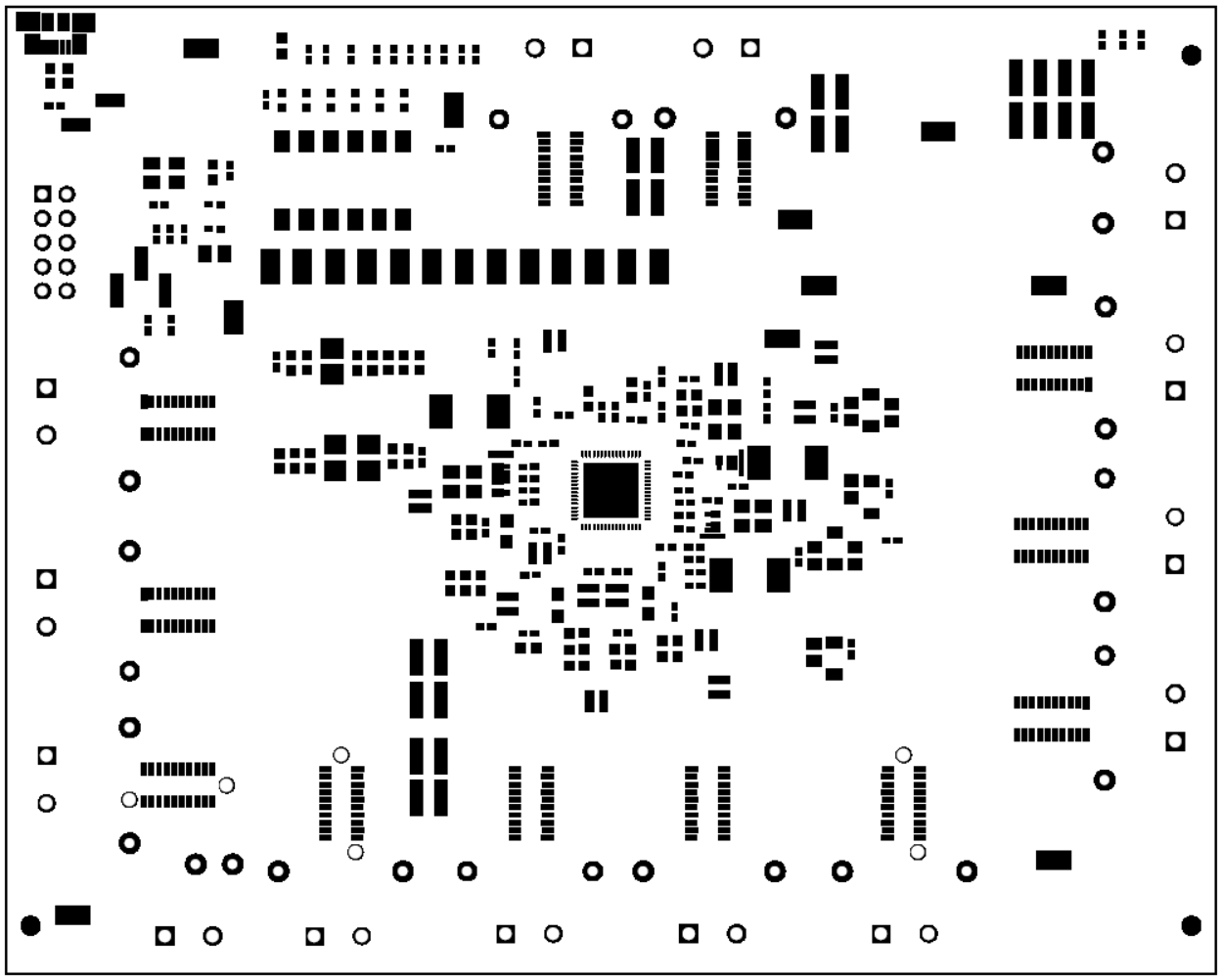

**Figure 15. Top Solder Mask**

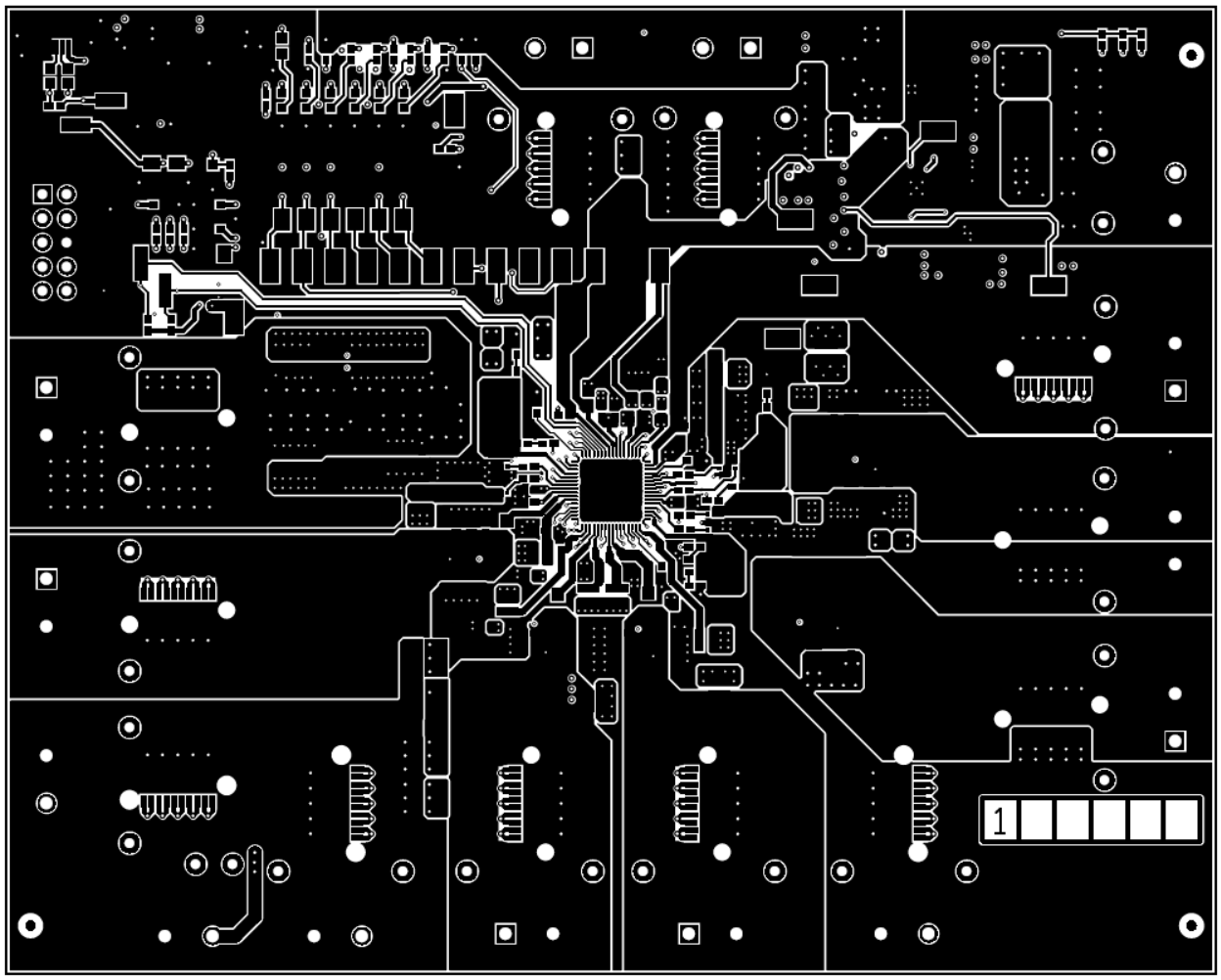


**Figure 16. Top Layer**

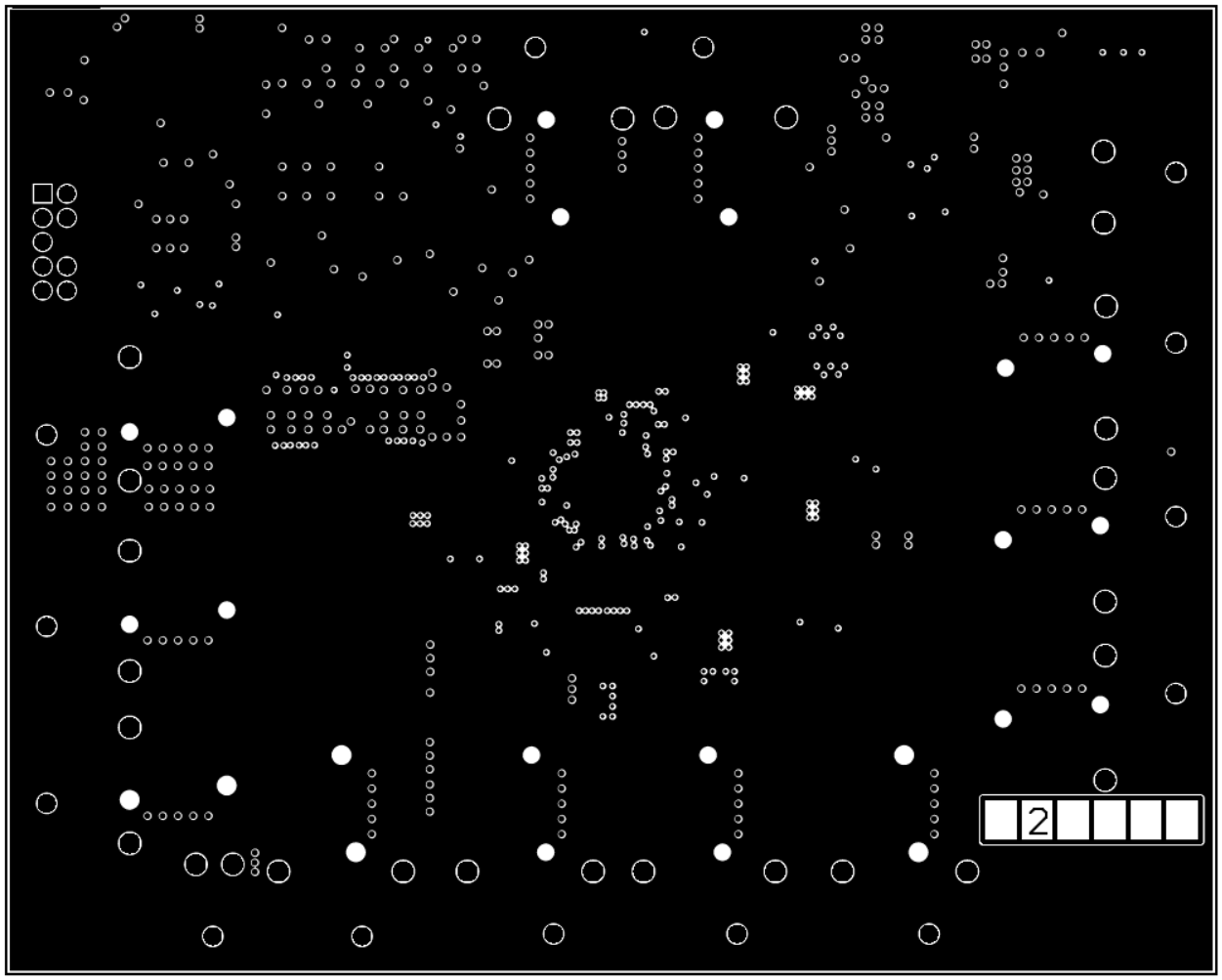


**Figure 17. GND Layer**

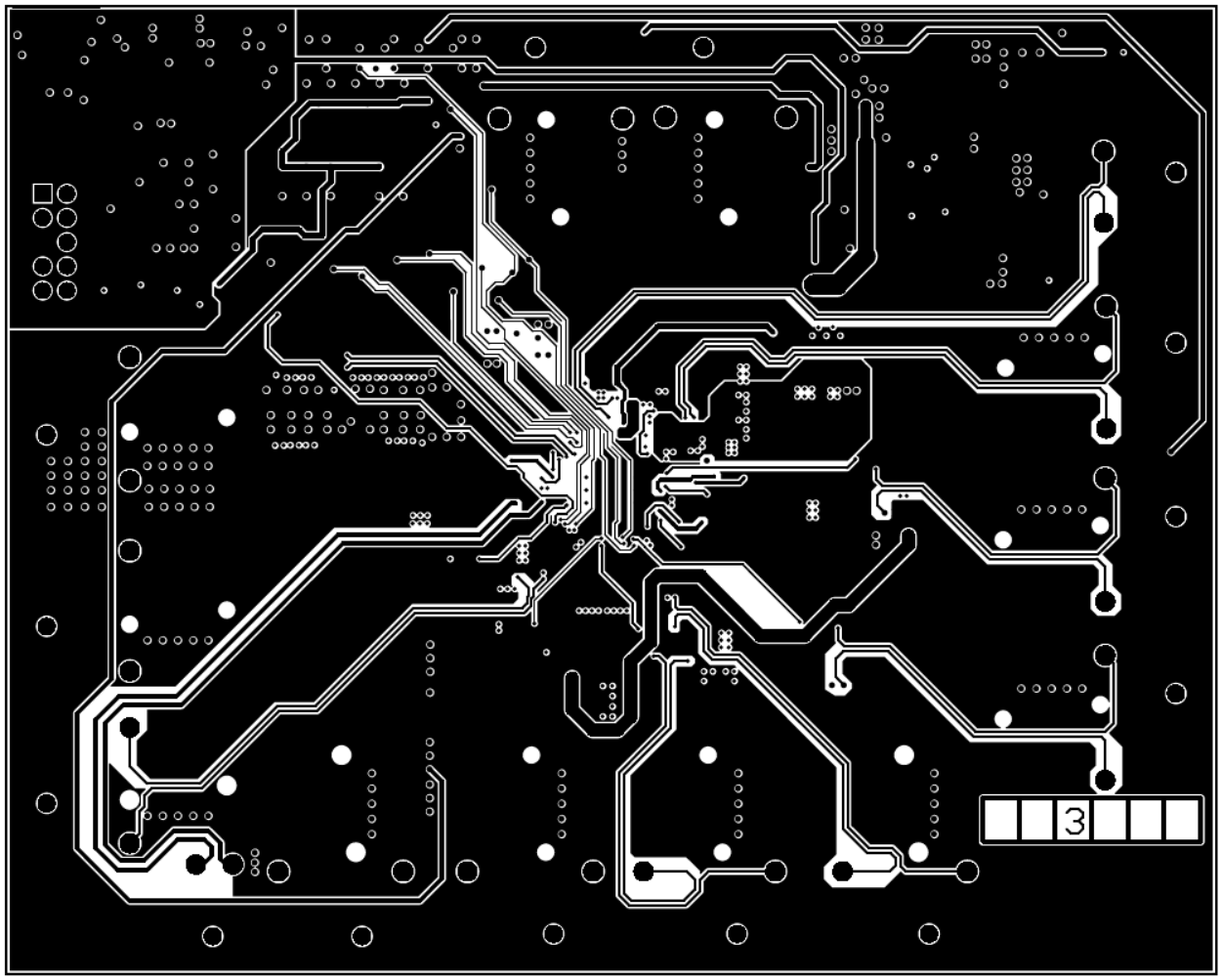


**Figure 18. Signal Layer 1**

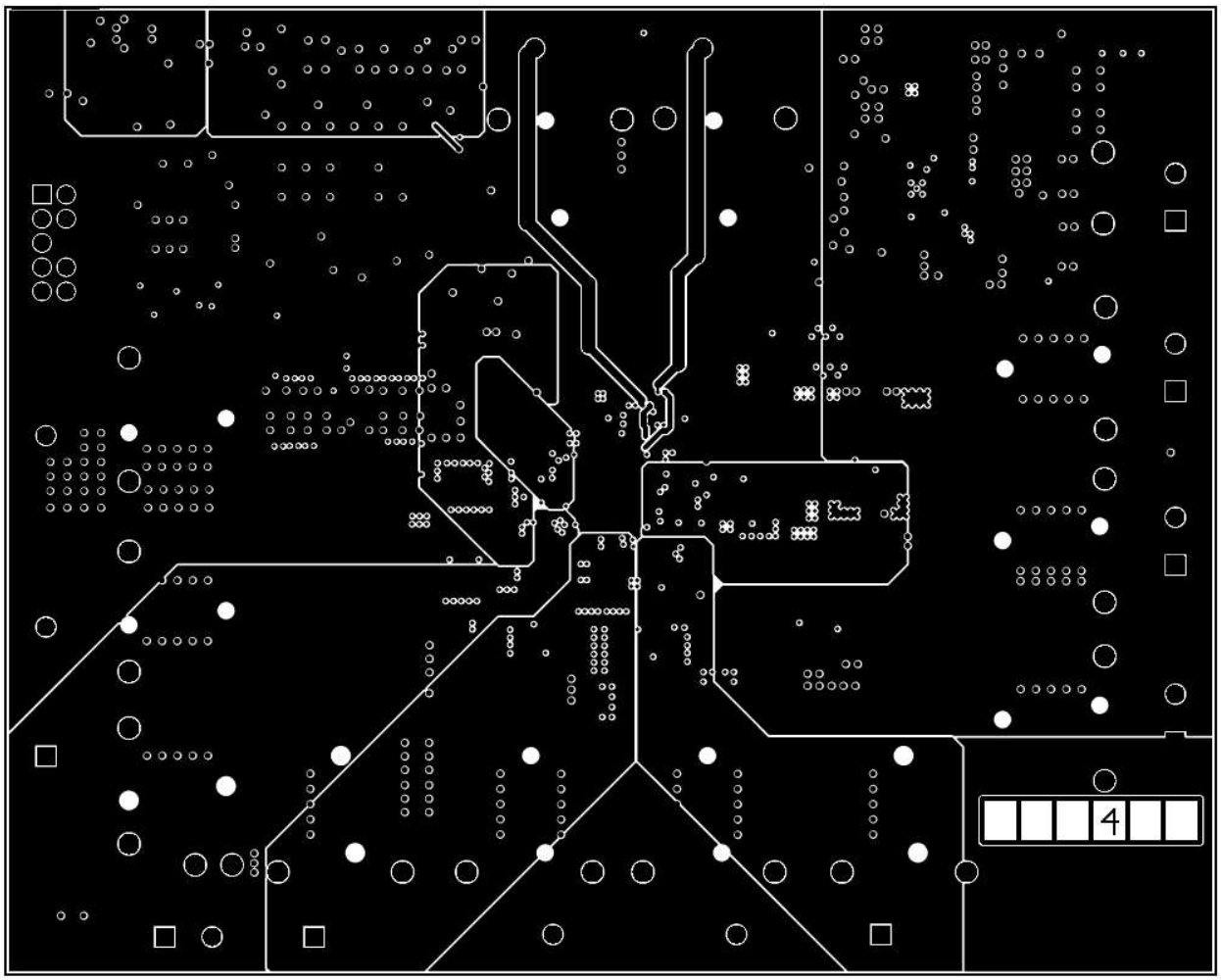


**Figure 19. Signal Layer 2**

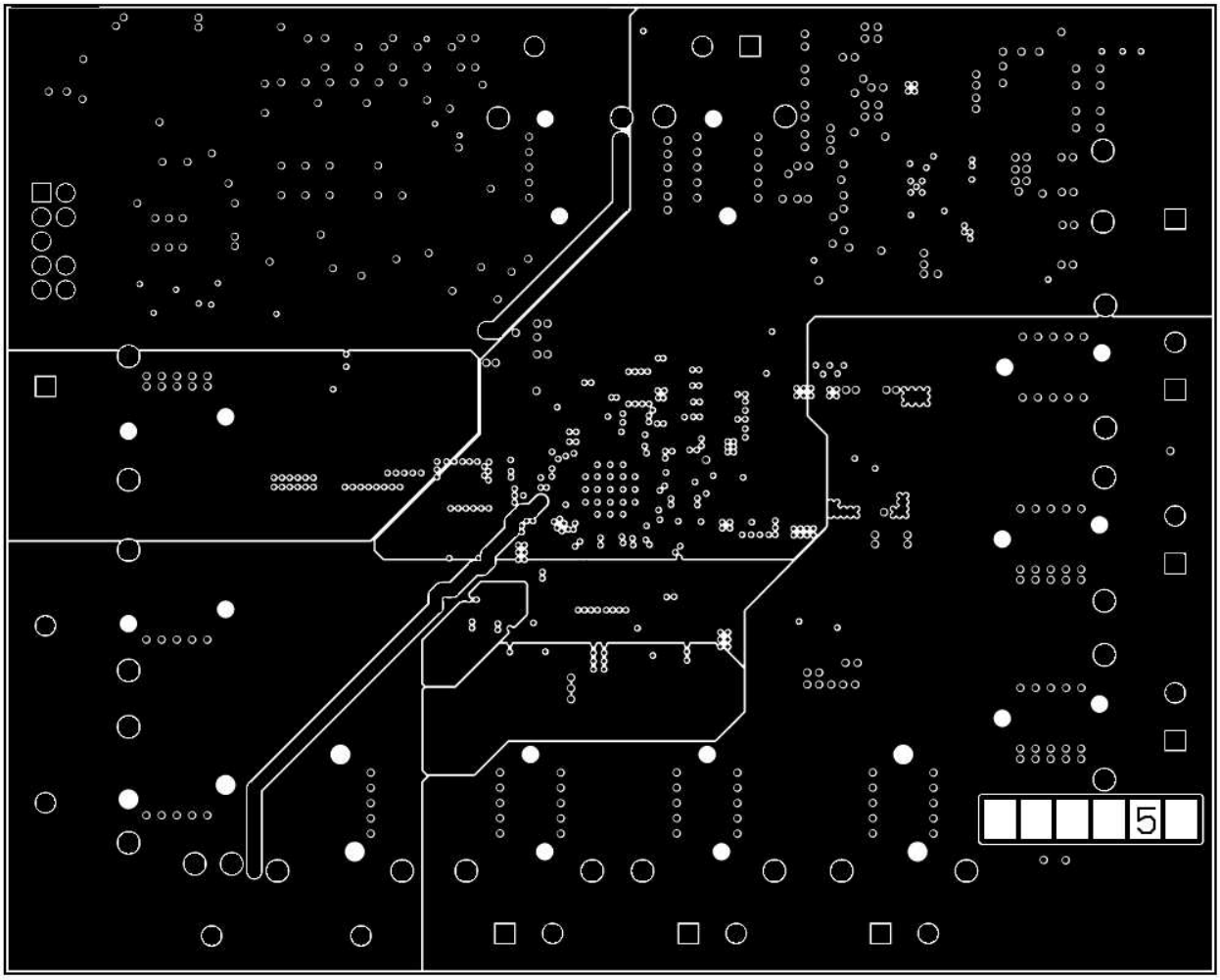


**Figure 20. Power Layer**

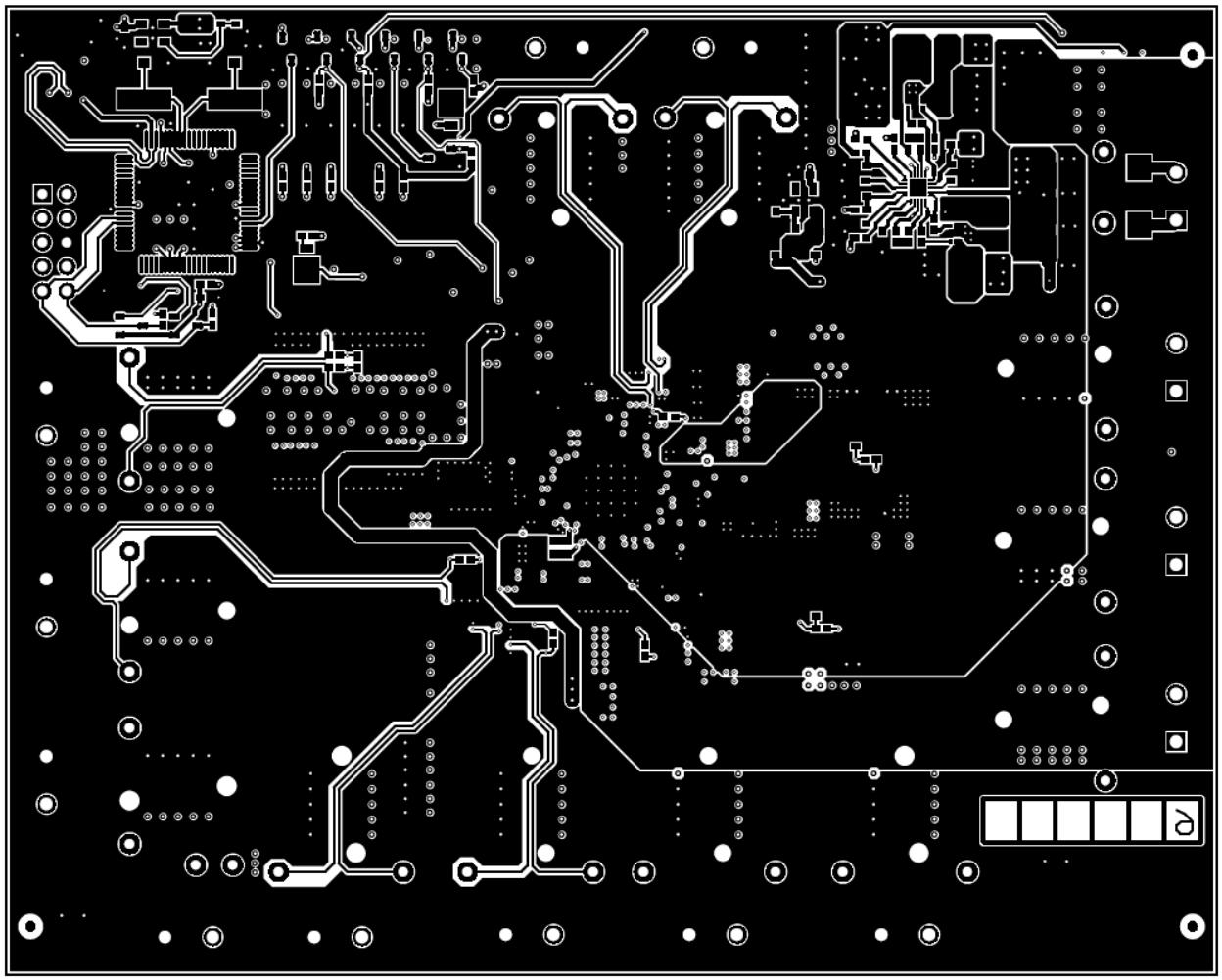

**Figure 21. Bottom Layer**

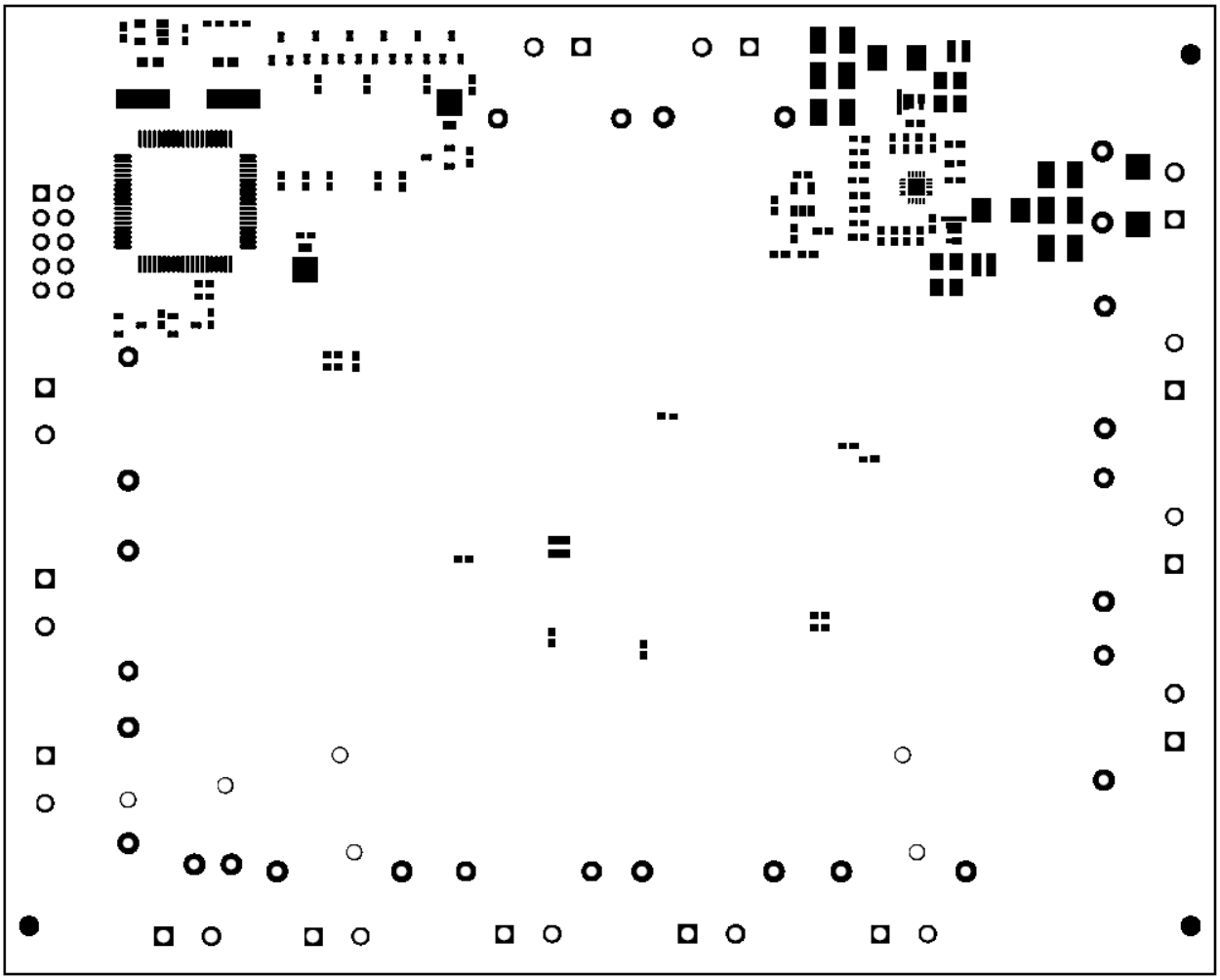

**Figure 22. Bottom Solder Mask**

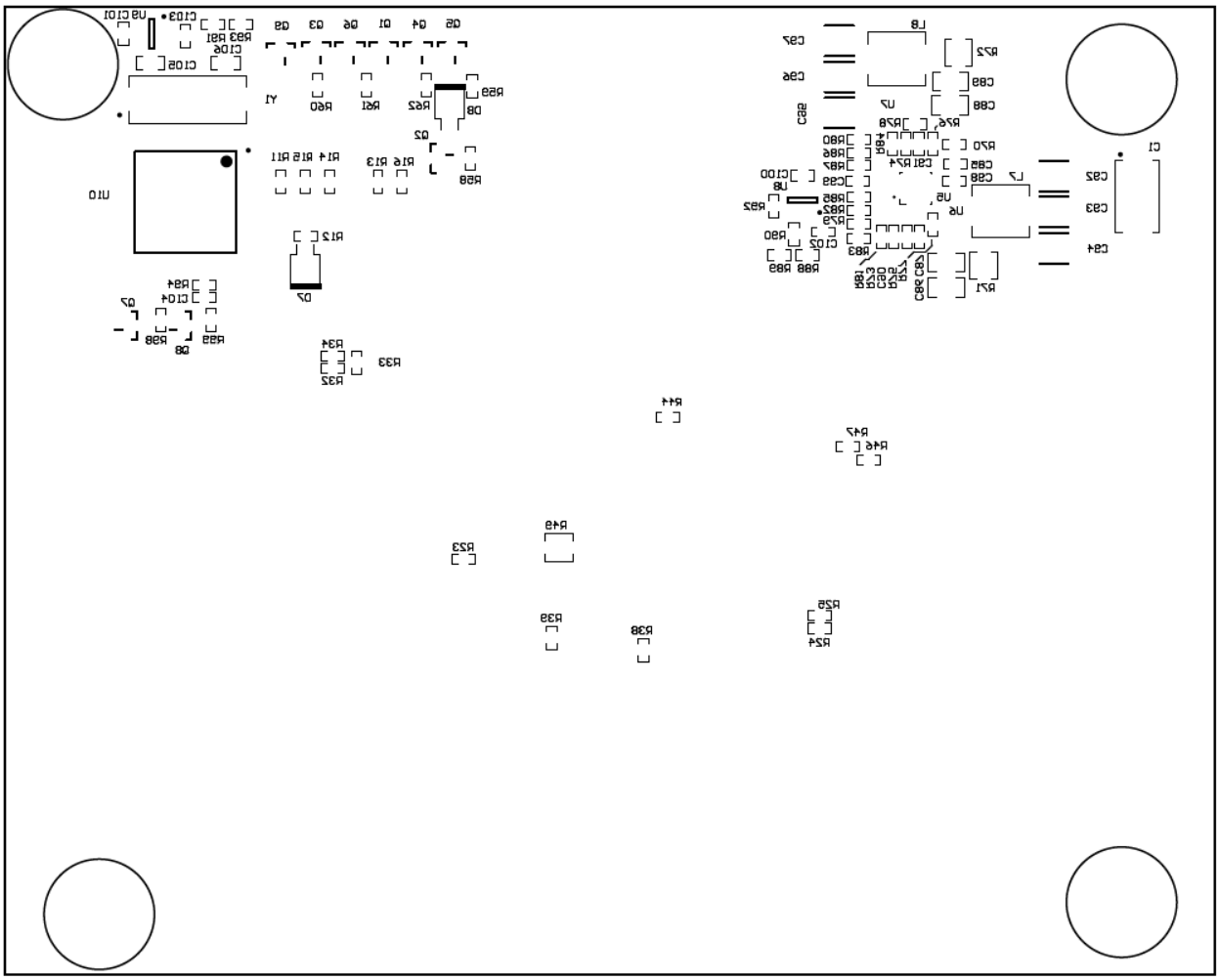

**Figure 23. Bottom Silk Overlay**

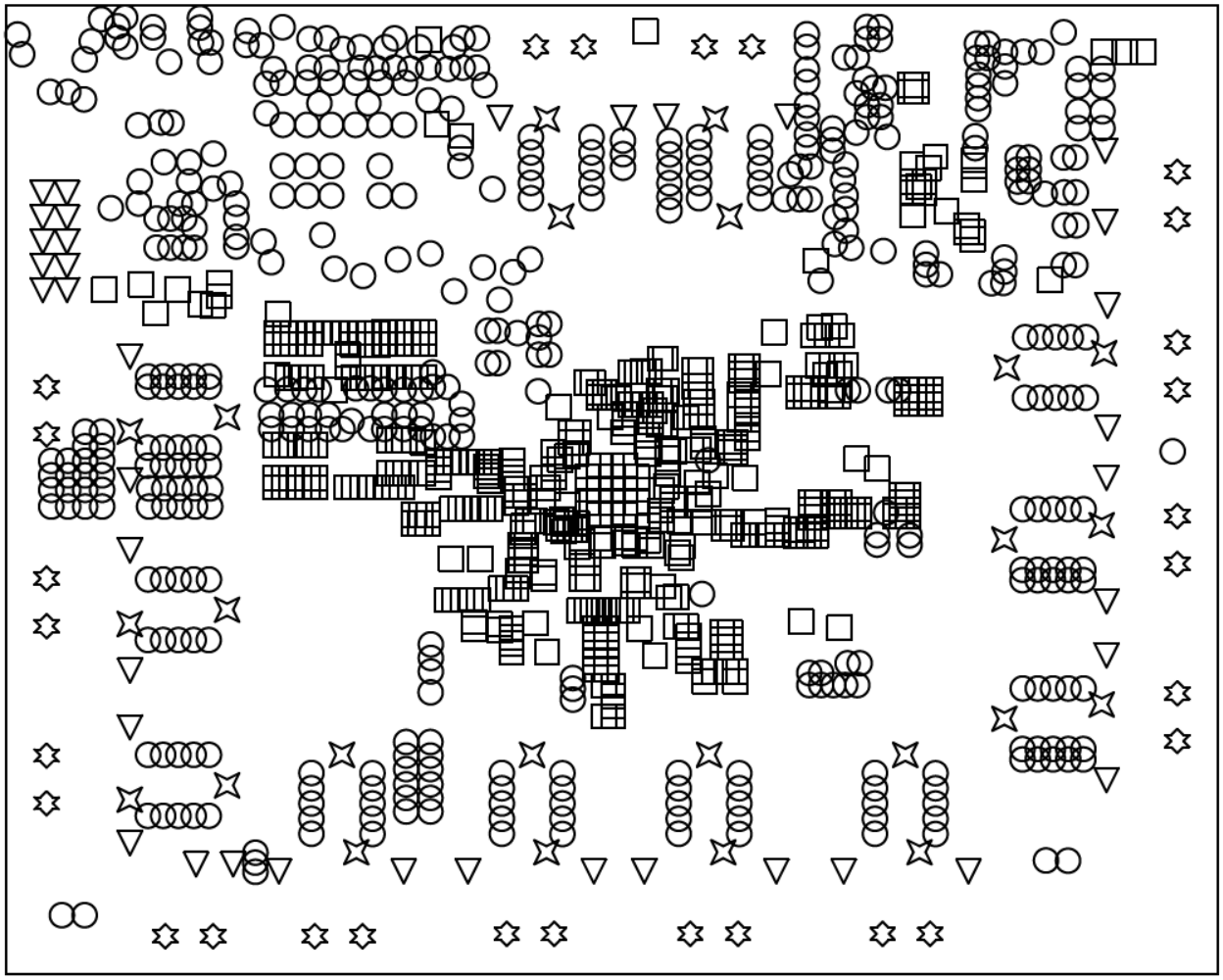

**Figure 24. Drill Drawing**

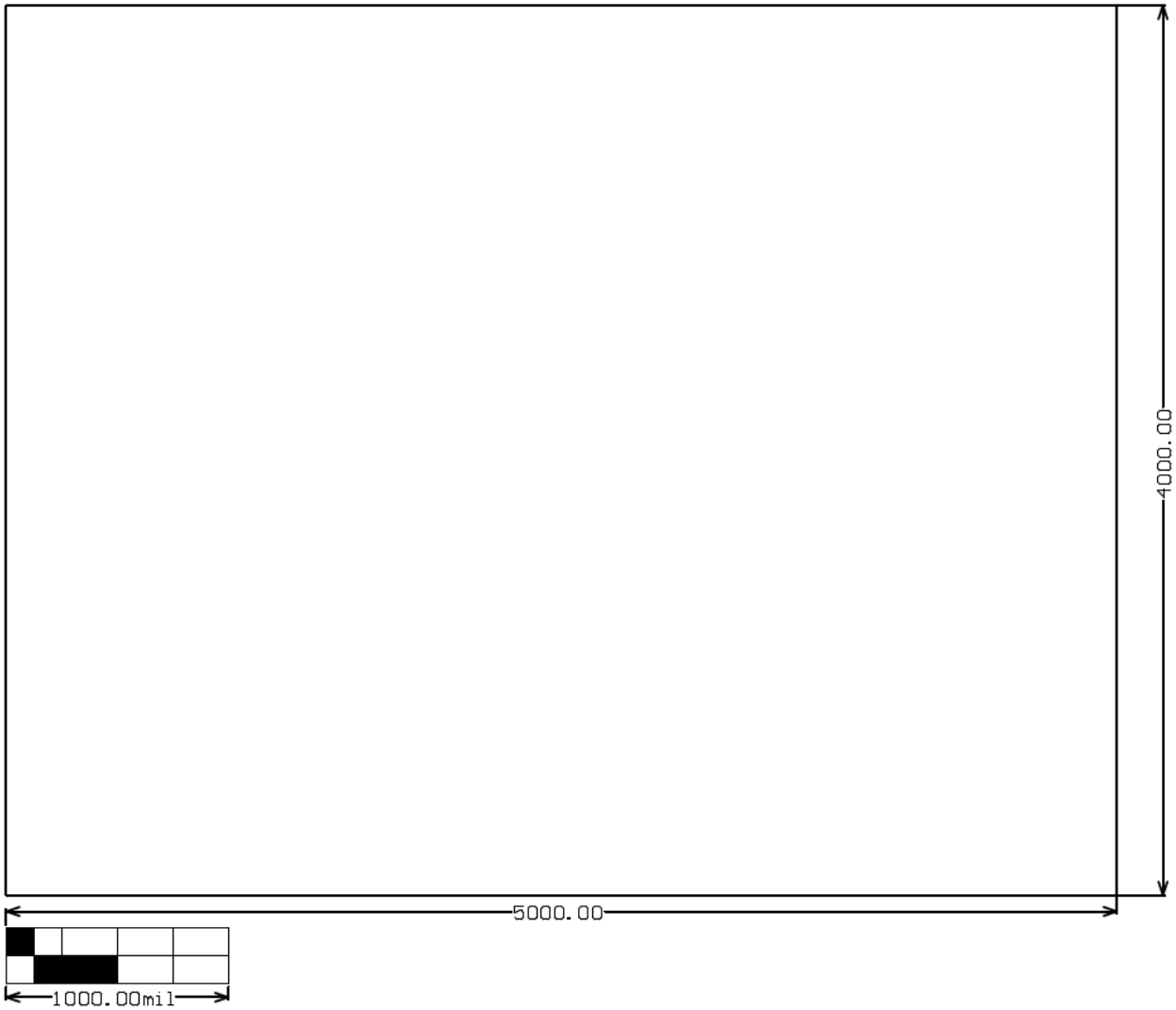


**Figure 25. Board Dimensions**

## 10.3 Bill of Materials

Table 4 lists the HVL116A bill of materials.

**Table 4. HVL116A Bill of Materials**

| Designator | Qty | Value | Description | Package Reference | Part Number | Manufacturer |
|---|---|---|---|---|---|---|
| !PCB1 | 1 | | Printed Circuit Board | | HVL116 EVM | Any |
| C1 | 1 | 47uF | CAP, TA, 47 µF, 35 V, +/- 10%, 0.3 ohm, SMD | 7343-43 | T495X476K035ATE300 | Kemet |
| C2, C3 | 2 | 2.2uF | CAP, CERM, 2.2 µF, 6.3 V, +/- 10%, X5R, 0402 | 0402 | CL05A225KQ5NNNC | Samsung |
| C4, C5, C6, C7 | 4 | 10uF | CAP, CERM, 10 µF, 10 V, +/- 20%, X5R, 0402 | 0402 | CL05A106MP5NUNC | Samsung Electro-Mechanics |
| C8, C79, C80, C81, C98, C99, C100, C101 | 8 | 4.7uF | CAP, CERM, 4.7 µF, 6.3 V, +/- 20%, X5R, 0402 | 0402 | GRM155R60J475ME47D | Murata |
| C9, C10, C15 | 3 | 1uF | CAP, CERM, 1 µF, 10 V, +/- 10%, X5R, 0402 | 0402 | GRM155R61A105KE15D | Murata |
| C11, C85 | 2 | 1uF | CAP, CERM, 1 µF, 35 V, +/- 10%, X5R, 0402 | 0402 | GRM155R6YA105KE11D | Murata |
| C12, C16, C24, C25, C31, C33, C51, C52, C58, C63, C64, C72, C73, C77, C82, C83, C84, C90, C91, C102, C103, C104, C111, C112, C113 | 25 | 0.1uF | CAP, CERM, 0.1 µF, 10 V, +/- 10%, X5R, 0402 | 0402 | GRM155R61A104KA01D | Murata |
| C13, C14 | 2 | 4.7uF | CAP, CERM, 4.7 µF, 10 V, +/- 20%, X5R, 0603_095 | 0603_095 | GRM188R61A475ME15 | Murata |
| C17, C18, C34, C35, C65, C66 | 6 | 22uF | CAP, CERM, 22 µF, 25 V, +/- 20%, X5R, 0805 | 0805 | GRM21BR61E226ME44 | Murata |
| C19, C67 | 2 | 220uF | CAP, CERM, 220 µF, 4 V, +/- 20%, X5R, 1206_190 | 1206_190 | GRM31CR60G227ME11L | Murata |
| C26, C27, C28, C29, C39, C74, C75 | 7 | 22uF | CAP, CERM, 22 µF, 6.3 V, +/- 20%, X5R, 0603 | 0603 | GRM188R60J226MEA0J | Murata |
| C36, C37 | 2 | 150uF | CAP, TA, 150 µF, 6.3 V, +/- 20%, 0.025 ohm, SMD | 3528-21 | T520B157M006ATE025 | Kemet |
| C54, C55, C59, C60 | 4 | 22uF | CAP, CERM, 22 µF, 6.3 V, +/- 20%, X5R, 0603 | 0603 | C1608X5R0J226M080AC | TDK |
| C86, C87, C88, C89 | 4 | 10uF | CAP, CERM, 10 µF, 35 V, +/- 10%, X5R, 0805 | 0805 | GRM21BR6YA106KE43L | Murata |
| C92, C93, C94, C95, C96, C97 | 6 | 150uF | CAP, Tantalum Polymer, 150 µF, 6.3 V, +/- 20%, 0.07 ohm, 3528-15 SMD | 3528-15 | 6TPG150M | Panasonic |
| C105, C106 | 2 | 22pF | CAP, CERM, 22 pF, 50 V, +/- 5%, C0G/NP0, 0603 | 0603 | 06035A220JAT2A | AVX |
| C107, C110 | 2 | 100pF | CAP, CERM, 100 pF, 50 V, +/- 10%, C0G/NP0, 0805 | 0805 | C0805C101K5GACTU | Kemet |
| C108 | 1 | 1000pF | CAP, CERM, 1000 pF, 50 V, +/- 10%, X7R, 0603 | 0603 | C0603C102K5RACTU | Kemet |
| C109 | 1 | 0.47uF | CAP, CERM, 0.47 µF, 16 V, +/- 5%, X7R, 0805 | 0805 | 0805YC474JAT2A | AVX |
| D1, D2, D3, D4, D5 | 5 | Yellow | LED, Yellow, SMD | LED_0603 | 150060YS75000 | Wurth Elektronik |
| D6 | 1 | Green | LED, Green, SMD | LED_0603 | 150060VS75000 | Wurth Elektronik |
| D7, D8 | 2 | 10V | Diode, Schottky, 10 V, 1 A, POWERMITE | POWERMITE | MBRM110LT1G | ON Semiconductor |
| FID1, FID2, FID3, FID4, FID5, FID6 | 6 | | Fiducial mark. There is nothing to buy or mount. | N/A | N/A | N/A |
| H1, H2, H3, H4 | 4 | | Bumpon, Hemisphere, 0.44 X 0.20, Clear | Transparent Bumpon | SJ-5303 (CLEAR) | 3M |
| H5 | 1 | | USB A MALE TO MICRO B MALE 6' | - | 3025013-06 | Qualtek |
| J1, J2, J4, J6, J8, J10, J12, J14, J16, J17, J19, J26, J27, J28 | 14 | | Terminal Block, 2x1, 5mm, Green, TH | Terminal Block, 2x1, 5mm, TH | 1935776 | Phoenix Contact |
| J21 | 1 | | Header, 100mil, 4x2, Gold, SMT | Header, 100mil, 4x2, SMT | 0015910080 | Molex |
| J22, J23, J24, J25 | 4 | | Header, 100mil, 2x2, Tin, SMT | 2x2 100mil Tin Header | 15-91-2040 | Molex |
| J32 | 1 | | Header (shrouded), 100mil, 5x2, High-Temperature, Gold, TH | 5x2 Shrouded header | N2510-6002-RB | 3M |
| J33 | 1 | | Header, 100mil, 3x1, Gold, SMT | Samtec_TSM-103-01-X-SV | TSM-103-01-L-SV | Samtec |

**Table 4. HVL116A Bill of Materials (continued)**

| Designator | Qty | Value | Description | Package Reference | Part Number | Manufacturer |
|---|---|---|---|---|---|---|
| J34 | 1 | | Connector, Receptacle, Micro-USB Type B, R/A, Bottom Mount SMT | 7.5x2.45x5mm | 0473460001 | Molex |
| L1, L6 | 2 | 470nH | Inductor, Drum Core, Powdered Iron, 470 nH, 11 A, 0.0073 ohm, SMD | 7.05 x 1.6 x 6.6mm | PIMB061H-R47MS | Cyntec |
| L2 | 1 | 220nH | Inductor, Ferrite, 220 nH, 21 A, 0.0032 ohm, SMD | 7x2.2x6.6mm | PIMB062D-R22MS | Cyntec |
| L3, L4, L5 | 3 | 470nH | Inductor, Drum Core, Powdered Iron, 470 nH, 4.5 A, 0.025 ohm, SMD | Inductor, 3.2x1.2x2.5mm | PIFE32251B-R47MS | Cyntec |
| L7, L8 | 2 | 2.2uH | Inductor, Drum Core, Powdered Iron, 2.2 µH, 5 A, 0.03 ohm, SMD | Inductor, 5.2x1.6x5.2mm | PIMB051H-2R2MS | Cyntec |
| LBL1 | 1 | | Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll | PCB Label 0.650"H x 0.200"W | THT-14-423-10 | Brady |
| Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9 | 9 | 50V | MOSFET, N-CH, 50 V, 0.22 A, SOT-23 | SOT-23 | BSS138 | Fairchild Semiconductor |
| R1, R2, R3, R4, R5, R6, R7, R17, R19, R28, R37, R41, R71, R72 | 14 | 0.002 | RES, 0.002, 2%, 1 W, 0508 | 0508 | KRL2012E-M-R002-G-T5 | Susumu Co Ltd |
| R8, R9, R10, R18, R20, R21, R23, R24, R27, R29, R30, R32, R34, R38, R39, R40, R42, R43, R44, R46, R51, R70, R73, R74, R77, R78, R83, R84, R89, R94 | 30 | 0 | RES, 0, 5%, 0.063 W, 0402 | 0402 | CRCW04020000Z0ED | Vishay-Dale |
| R11, R12, R13, R14, R15, R16, R90, R91, R95, R96, R97 | 11 | 100k | RES, 100 k, 5%, 0.063 W, 0402 | 0402 | CRCW0402100KJNED | Vishay-Dale |
| R26, R48 | 2 | 12.1k | RES, 12.1 k, 1%, 0.063 W, 0402 | 0402 | CRCW040212K1FKED | Vishay-Dale |
| R35 | 1 | 13.3k | RES, 13.3 k, 1%, 0.063 W, 0402 | 0402 | CRCW040213K3FKED | Vishay-Dale |
| R52, R53, R54, R55, R56, R57, R105 | 7 | 1.5k | RES, 1.5 k, 5%, 0.063 W, 0402 | 0402 | CRCW04021K50JNED | Vishay-Dale |
| R58, R59, R61, R62, R85 | 5 | 100k | RES, 100 k, 1%, 0.063 W, 0402 | 0402 | CRCW0402100KFKED | Vishay-Dale |
| R75, R76 | 2 | 30.1 | RES, 30.1, 1%, 0.063 W, 0402 | 0402 | CRCW040230R1FKED | Vishay-Dale |
| R79, R80 | 2 | 7.15k | RES, 7.15 k, 1%, 0.063 W, 0402 | 0402 | CRCW04027K15FKED | Vishay-Dale |
| R81 | 1 | 200 | RES, 200, 5%, 0.063 W, 0402 | 0402 | CRCW0402200RJNED | Vishay-Dale |
| R82 | 1 | 150k | RES, 150 k, 1%, 0.063 W, 0402 | 0402 | CRCW0402150KFKED | Vishay-Dale |
| R86 | 1 | 130k | RES, 130 k, 1%, 0.063 W, 0402 | 0402 | CRCW0402130KFKED | Vishay-Dale |
| R87 | 1 | 200k | RES, 200 k, 1%, 0.063 W, 0402 | 0402 | CRCW0402200KFKED | Vishay-Dale |
| R98, R99, R100, R101 | 4 | 2.2k | RES, 2.2 k, 5%, 0.063 W, 0402 | 0402 | CRCW04022K20JNED | Vishay-Dale |
| R102 | 1 | 1.50k | RES, 1.50 k, 1%, 0.1 W, 0603 | 0603 | CRCW06031K50FKEA | Vishay-Dale |
| R103 | 1 | 120k | RES, 120 k, 1%, 0.063 W, 0402 | 0402 | CRCW0402120KFKED | Vishay-Dale |
| R104, R106 | 2 | 33.0 | RES, 33.0, 1%, 0.1 W, 0603 | 0603 | CRCW060333R0FKEA | Vishay-Dale |
| S1 | 1 | | Switch, SPST 6Pos, SMT | 10.4x3.9x9.3mm | SDA06H1SBD | C&K Components |
| SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6 | 6 | | Shunt, 100mil, Gold plated, Black | Shunt 2 pos. 100 mil | 881545-2 | TE Connectivity |
| TP1, TP16, TP18, TP20, TP22, TP23, TP26, TP27, TP30, TP31, TP32, TP36, TP37, TP38 | 14 | Red | Test Point, Miniature, Red, TH | Red Miniature Testpoint | 5000 | Keystone |
| TP2, TP17, TP19, TP21, TP24, TP25, TP28, TP29, TP33, TP34, TP35, TP39, TP40, TP41 | 14 | Black | Test Point, Miniature, Black, TH | Black Miniature Testpoint | 5001 | Keystone |

**Table 4. HVL116A Bill of Materials (continued)**

| Designator | Qty | Value | Description | Package Reference | Part Number | Manufacturer |
|---|---|---|---|---|---|---|
| TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP42, TP43, TP44, TP45, TP46, TP47, TP48, TP49, TP50, TP51 | 23 | SMT | Test Point, Miniature, SMT | Testpoint_Keystone_Miniature | 5015 | Keystone |
| U1 | 1 | | Configurable Multi-Rail PMU for Multi-Core Processor, RSK0064C | RSK0064C | TPS650860A0RSKR | Texas Instruments |
| U2, U4, U6, U7 | 4 | | Synchronous Buck NexFET Power Block II, MPC0005A | MPC0005A | CSD87381P | Texas Instruments |
| U3 | 1 | | Synchronous Buck NexFET Power Block II, MPA0005A | MPA0005A | CSD87588N | Texas Instruments |
| U5 | 1 | | Ultra-Low Quiescent (ULQ(TM)) Dual Synchronous Step-Down Controller with 5V and 3.3V LDOs, RUK0020B | RUK0020B | TPS51285BRUK | Texas Instruments |
| U8 | 1 | | Single Output LDO, 150 mA, Fixed 1.8 V Output, 2.7 to 10 V Input, with Low IQ, 5-pin SOT-23 (DBV), -40 to 125 degC, Green (RoHS & no Sb/Br) | DBV0005A | TPS76318DBVT | Texas Instruments |
| U9 | 1 | | Single Output LDO, 150 mA, Fixed 3.3 V Output, 2.7 to 10 V Input, with Low IQ, 5-pin SOT-23 (DBV), -40 to 125 degC, Green (RoHS & no Sb/Br) | DBV0005A | TPS76333DBVT | Texas Instruments |
| U10 | 1 | | Mixed Signal MicroController, PN0080A | PN0080A | MSP430F5529IPN | Texas Instruments |
| Y1 | 1 | | Crystal, 24.000MHz, 20pF, SMD | Crystal, 11.4x4.3x3.8mm | ECS-240-20-5PX-TR | ECS Inc. |
| C20, C68 | 0 | 220uF | CAP, CERM, 220 µF, 4 V, +/- 20%, X5R, 1206_190 | 1206_190 | GRM31CR60G227ME11L | Murata |
| C21, C22, C23, C69, C70, C71 | 0 | 100uF | CAP, CERM, 100 µF, 6.3 V, +/- 20%, X5R, 0805 | 0805 | GRM21BR60J107M | Murata |
| C30, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50 | 0 | 22uF | CAP, CERM, 22 µF, 6.3 V, +/- 20%, X5R, 0603 | 0603 | GRM188R60J226MEA0J | Murata |
| C32, C53, C78 | 0 | 6800pF | CAP, CERM, 6800 pF, 25 V, +/- 10%, X7R, 0402 | 0402 | GRM155R71E682KA01D | Murata |
| C38 | 0 | 330uF | CAP, Tantalum Polymer, 330 µF, 2 V, +/- 20%, 0.015 ohm, 3528-21 SMD | 3528-21 | 2TPE330MAFB | Panasonic |
| C56, C57, C61, C62 | 0 | 22uF | CAP, CERM, 22 µF, 6.3 V, +/- 20%, X5R, 0603 | 0603 | C1608X5R0J226M080AC | TDK |
| C76 | 0 | 0.1uF | CAP, CERM, 0.1 µF, 10 V, +/- 10%, X5R, 0402 | 0402 | GRM155R61A104KA01D | Murata |
| J3, J5, J7, J9, J11, J13, J15, J18, J20, J29, J30, J31 | 0 | | Card Edge Socket, 0.8mm, 10x2, SMT | Card Edge Socket, 0.8mm, 10x2, SMT | HSEC8-110-01-S-DV-A | Samtec |
| J35 | 0 | | Header, 2.54 mm, 2x1, Gold, R/A, SMT | Header, 2.54 mm, 2x1, R/A, SMT | 87898-0204 | Molex |
| R22, R31, R45 | 0 | 2.2 | RES, 2.2, 5%, 0.063 W, 0402 | 0402 | CRCW04022R20JNED | Vishay-Dale |
| R25, R33, R47, R50, R88, R92, R93 | 0 | 0 | RES, 0, 5%, 0.063 W, 0402 | 0402 | CRCW04020000Z0ED | Vishay-Dale |
| R36, R49 | 0 | 0.002 | RES, 0.002, 2%, 1 W, 0508 | 0508 | KRL2012E-M-R002-G-T5 | Susumu Co Ltd |
| R60, R63, R64, R65, R66, R67, R68, R69 | 0 | 100k | RES, 100 k, 1%, 0.063 W, 0402 | 0402 | CRCW0402100KFKED | Vishay-Dale |

# STANDARD TERMS AND CONDITIONS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, or documentation (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms and conditions set forth herein. Acceptance of the EVM is expressly subject to the following terms and conditions.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms and conditions that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms and conditions do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for any defects that are caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI. Moreover, TI shall not be liable for any defects that result from User's design, specifications or instructions for such EVMs. Testing and other quality control techniques are used to the extent TI deems necessary or as mandated by government requirements. TI does not test all parameters of each EVM.

   2.3 If any EVM fails to conform to the warranty set forth above, TI's sole liability shall be at its option to repair or replace such EVM, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      **CAUTION**

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      **FCC Interference Statement for Class A EVM devices**

      *NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.*

**FCC Interference Statement for Class B EVM devices**

*NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:*

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210*

**Concerning EVMs Including Radio Transmitters:**

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

**Concernant les EVMs avec appareils radio:**

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

**Concerning EVMs Including Detachable Antennas:**

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

**Concernant les EVMs avec antennes détachables**

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

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