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REVISION HISTORY

1/2020—Revision 0: Initial Version

Table 4. P1 to P4 and IN1 to IN4 Link Settings for Parallel Interface

Controlled RF Switch	RF Switch Status	Link Name	Link Position
RF1 to RFC	On	P1	D_IN1
		IN1	On
	Off	P1	D_IN1 (default)
		IN1	Off (default)
RF2 to RFC	On	P2	D_IN2
		IN2	On
	Off	P2	D_IN2 (default)
		IN2	Off (default)
RF3 to RFC	On	P3	D_IN3
		IN3	On
	Off	P3	D_IN3 (default)
		IN3	Off (default)
RF4 to RFC	On	P4	D_IN4
		IN4	On
	Off	P4	D_IN4 (default)
		IN4	Off (default)

MEMORY MAP

All registers are fully accessible from the **ADGM1304 Memory Map** tab, and can be edited at a bit level (see Figure 6). The bits in dark gray are read-only bits and cannot be accessed from the ACE software. All other bits are toggled. The **Apply Changes** button transfers data to the device. All changes made in this tab correspond to the block diagram.

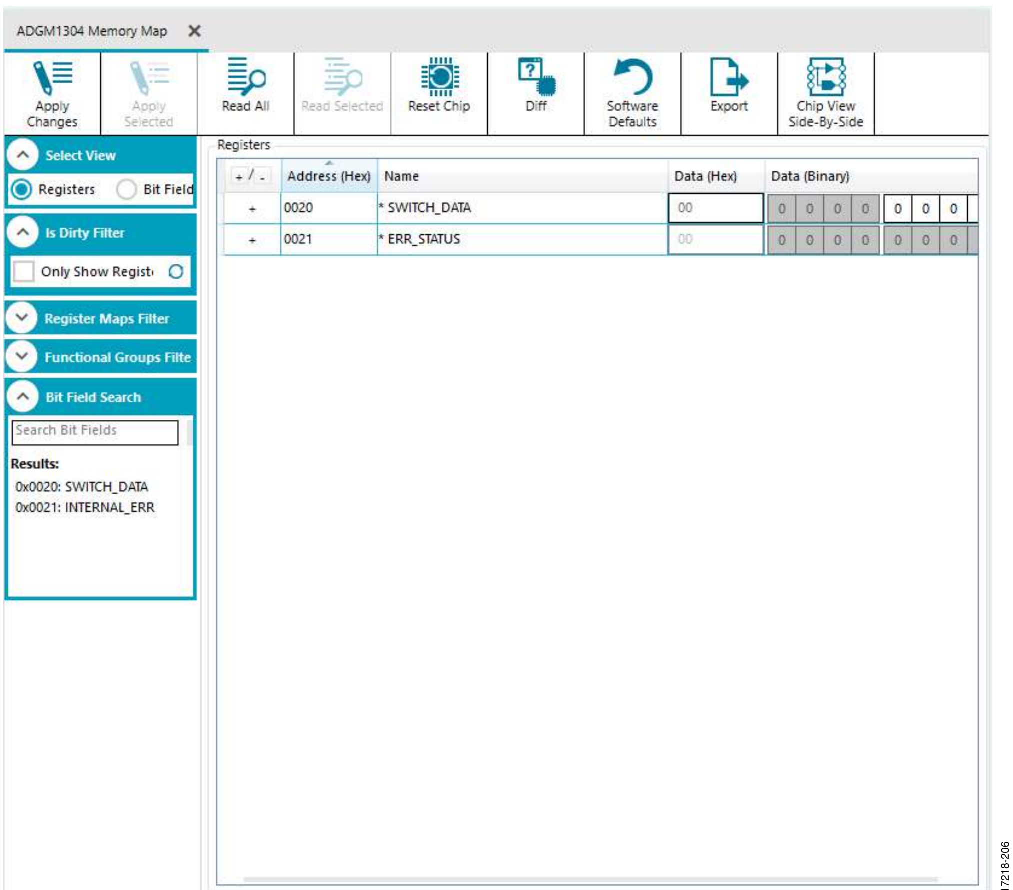

Figure 6. ADGM1304 Memory Map

Figure 9 shows the ADGM1304 switch insertion loss (network analyzer two port S(2,1) measurement) measurement results that were de-embedded with respect to the PCB transmission line losses. The blue trace is the RF2 to RFC switch channel and the red trace is the RF1 to RFC switch channel. The dashed traces are the respective return loss traces. The performance of the RF2 switch is identical to the RF3 switch, and the performance of the RF1 switch is identical to the RF4 switch.

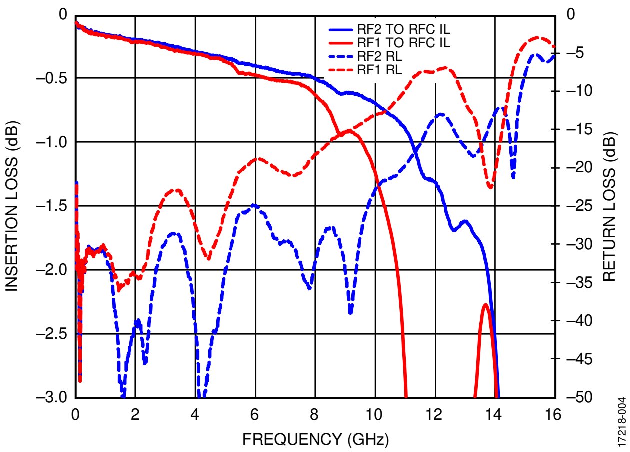

Figure 9. ADGM1304 Insertion Loss Performance, PCB De-Embedded

Figure 10 shows the ADGM1304 switch off isolation performance measurement results for two channels. The blue trace is the RF2 to RFC switch channel, and the red trace is the RF1 to RFC switch channel. The performance of the RF2 switch is identical to the RF3 switch, and the performance of the RF1 switch is identical to the RF4 switch.

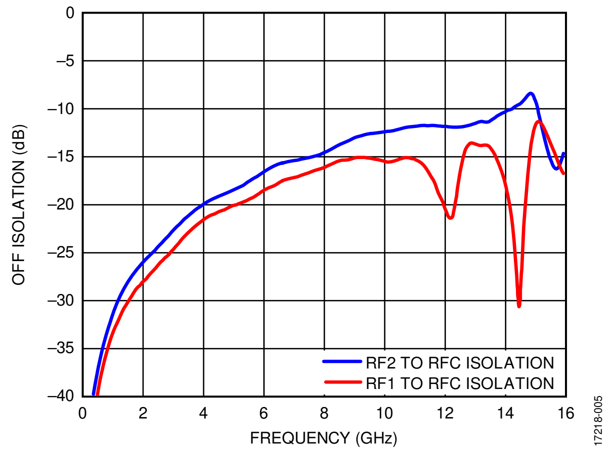

Figure 10. ADGM1304 Off-Isolation Performance

NETWORK ANALYZER CALIBRATION PROCEDURE

Use the following procedure in conjunction with the EVAL-ADGM1304SDZ evaluation board for two port measurements. Two port measurements require the user to have a set of manual calibration standards or an electric calibration type unit to perform a short, load, open, through (SLOT) calibration of the network analyzer. The maximum value of the network analyzer frequency sweep for the EVAL-ADGM1304SDZ PCB can be up to 16 GHz.

1. Perform a full, two-port standard SLOT calibration of the network analyzer.
2. Connect the CALIBRATION THRU calibration line (Connector RF5 and Connector RF6) to the analyzer and measure its insertion loss S(2, 1).
3. Save the measured data to the network analyzer memory for later use.
4. Configure the EVAL-ADGM1304SDZ links and power up the EVAL-ADGM1304SDZ with a 3.3 V dc power supply.
5. Connect the network analyzer to the desired MEMS switch RF connectors and apply the external control signals, if needed.
6. Measure the complete insertion loss of the EVAL-ADGM1304SDZ. Include the insertion loss of the MEMS switch and test fixture (PCB transmission lines and RF connectors).
7. De-embed the PCB losses from the complete evaluation board measurement using the data saved at Step 3 and the measured data at Step 6. The extraction method is dependent on the network analyzer, so the user must consult the documentation of the network analyzer in use before performing the extraction. Typically, the divide function is used to divide the complete S(2, 1) measurement data by the CALIBRATION THRU line S(2, 1) data stored in memory.
8. Use the network analyzer port extension function to de-embed the phase offset introduced by the PCB transmission lines. The port extension method uses time delay offset values to correct for phase. Enter the time delay values into the port extension menu on the network analyzer for each RF edged connector to switch the pin path equal to the electrical length of the calibration line divided by two.

HANDLING GUIDELINES

Adhere to the following handling guidelines when using the EVAL-ADGM1304SDZ:

- Always treat the ADGM1304 as a static sensitive device and observe normal handling precautions, including working only on static dissipative surfaces, wearing wrist straps, and using other electrostatic discharge (ESD) control devices.
- Take care when connecting signals. Hold the EVAL-ADGM1304SDZ from the edges to avoid any damage to the device under test (DUT).
- Avoid connecting live signal sources to the EVAL-ADGM1304SDZ. Ensure that outputs are switched off (preferably grounded) before connecting to the DUT. Ensure that all instrumentation shares a common chassis ground.
- Avoid running measurement instruments such as digital multimeters (DMMs) in autorange modes. Some instruments generate large transient compliance voltages when switching ranges.
- Use the highest practical range (lowest resolution) setting for resistance measurements to minimize compliance voltages.
- Physically handle the EVAL-ADGM1304SDZ with care.

EVALUATION BOARD SCHEMATIC AND ARTWORK

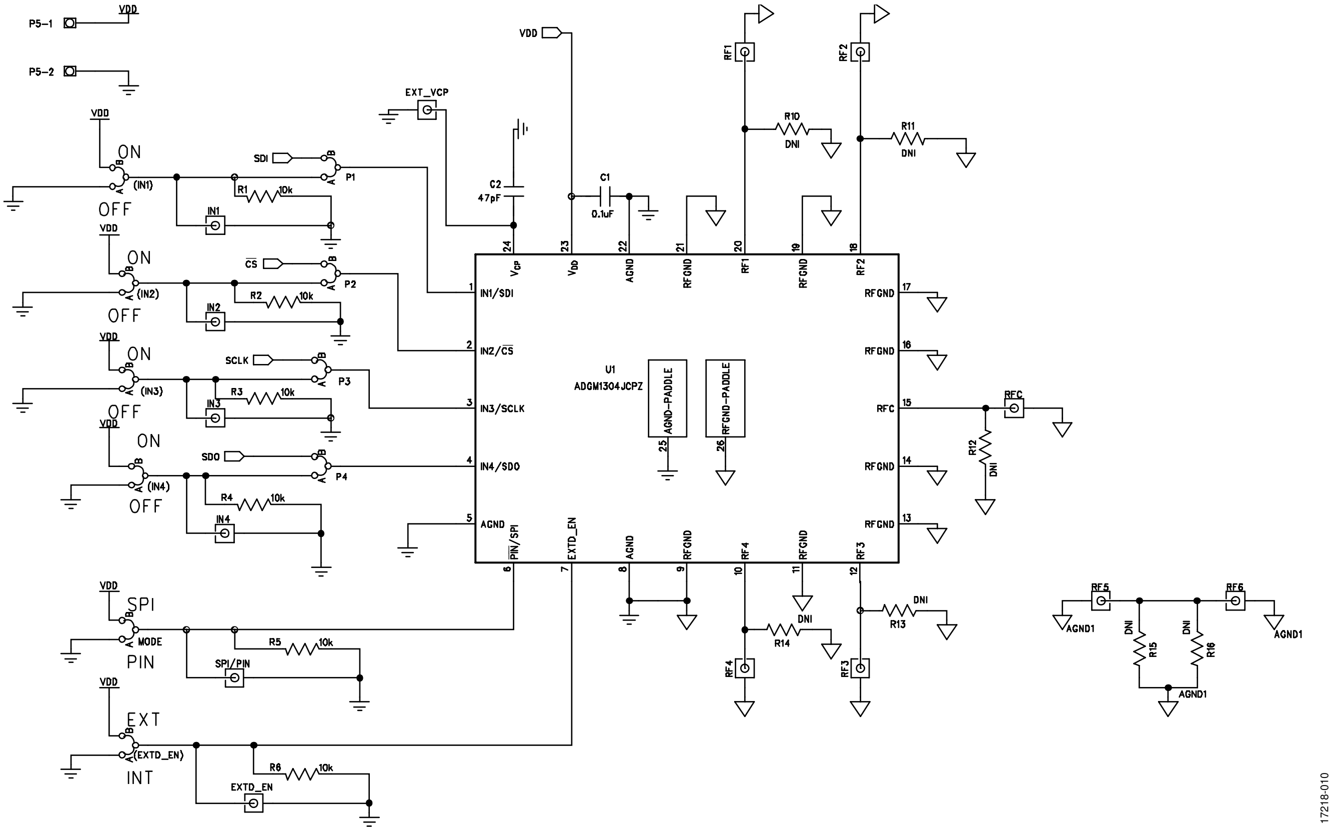

Figure 11. Schematic of the EVAL-ADGM1304SDZ

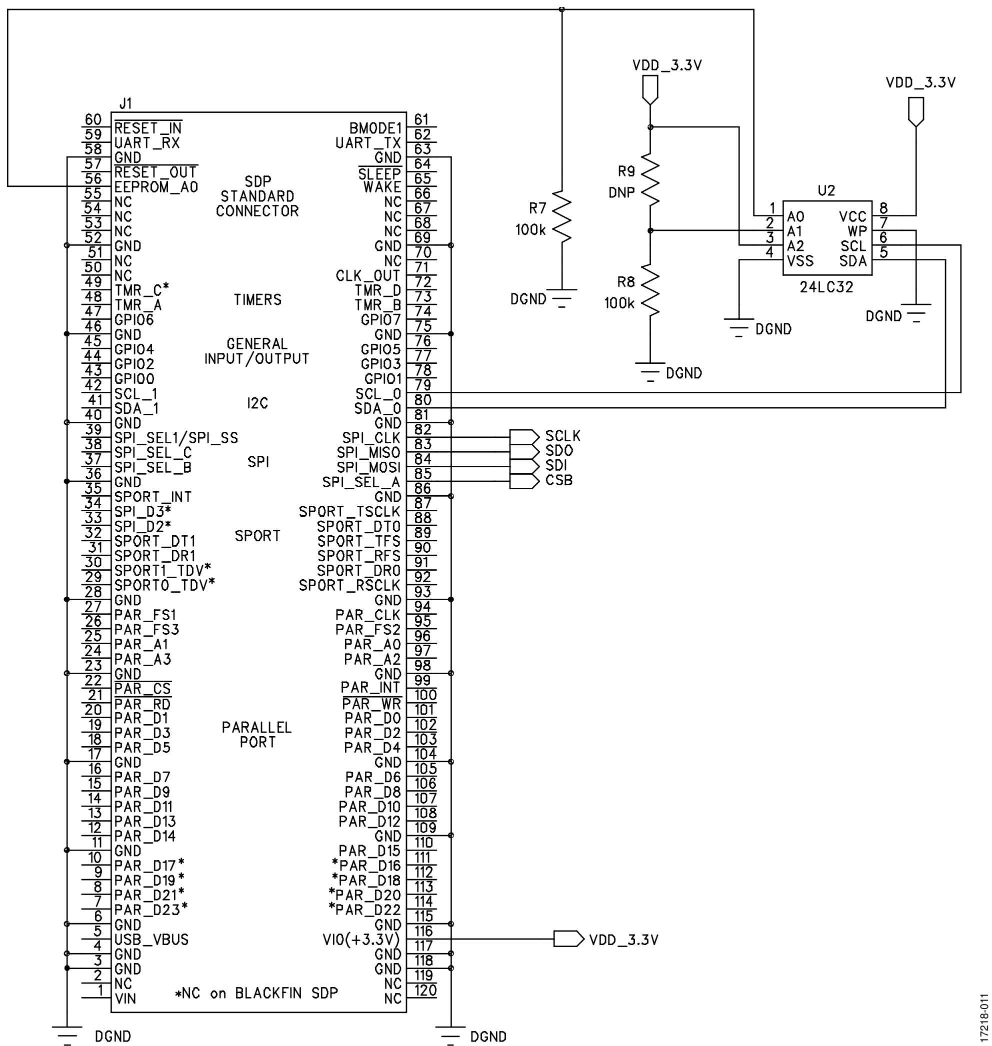

Figure 12. Schematic of the EVAL-ADGM1304SDZ Showing SDP Connector

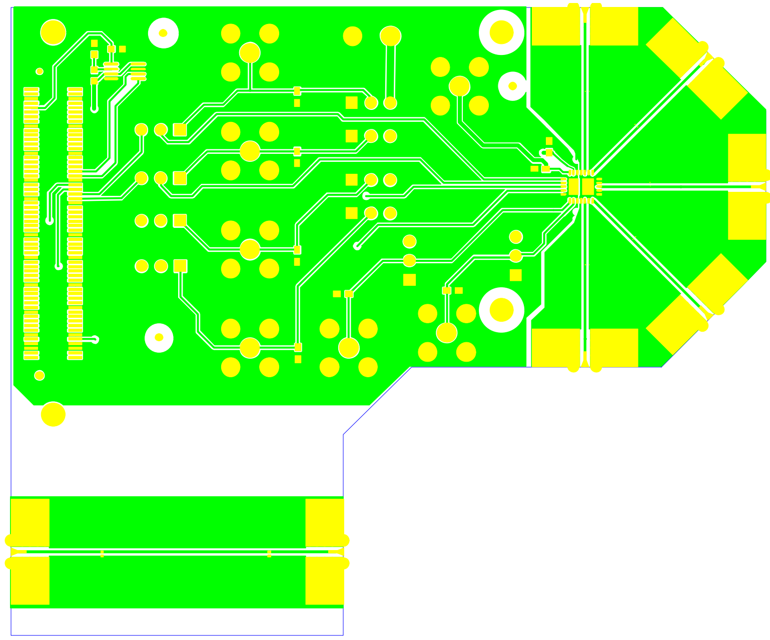

Figure 13. EVAL-ADGM1304SDZ Component Side PCB Drawing (Layer 1)

Figure 14. EVAL-ADGM1304SDZ Component Side Ground Plane PCB Drawing (Layer 2)

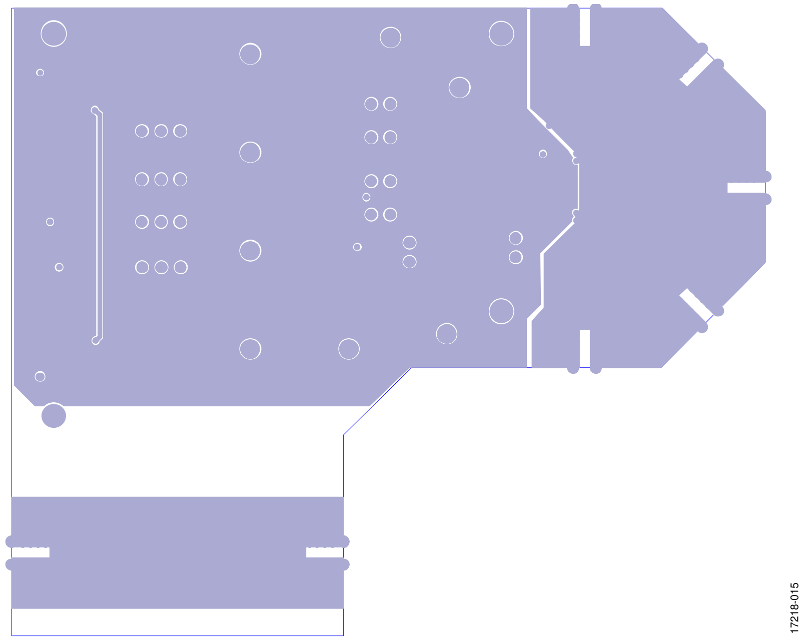

Figure 15. EVAL-ADGM1304SDZ Component Side Ground Plane PCB Drawing (Layer 3)

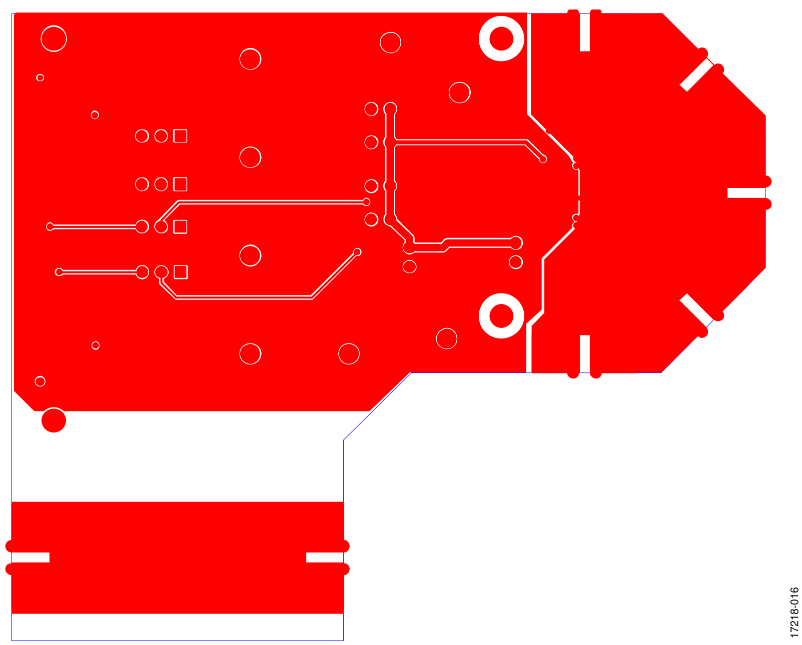

Figure 16. EVAL-ADGM1304SDZ Component Side, Bottom Side PCB Drawing (Layer 4)

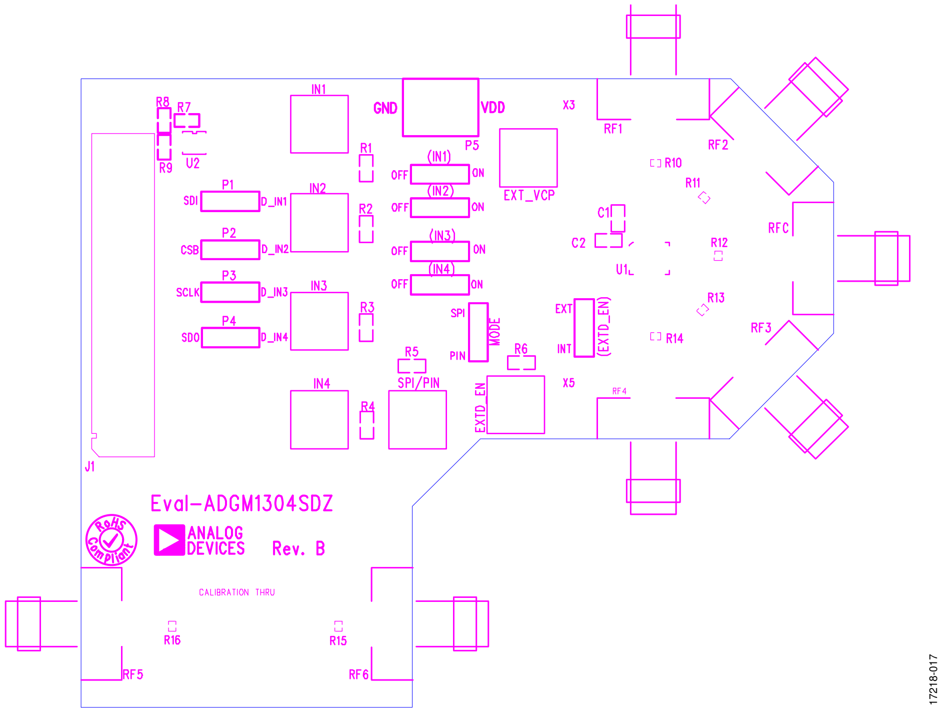

Figure 17. EVAL-ADGM1304SDZ Component Side Silkscreen PCB Drawing (Top)

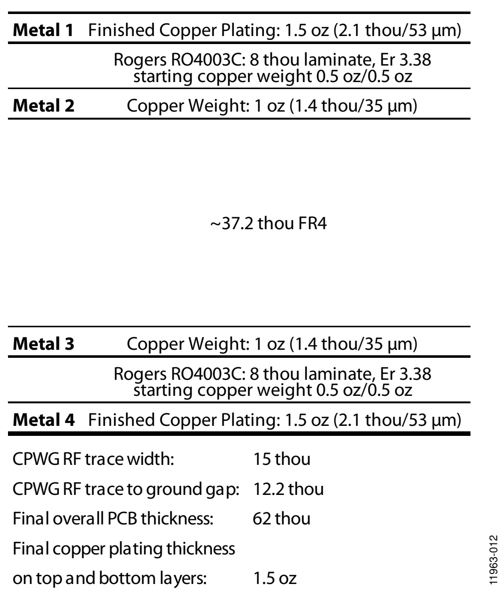

Figure 18. EVAL-ADGM1304SDZ PCB Stack Up with Coplanar Waveguide with Ground (CPWG) Dimensions

ORDERING INFORMATION

BILL OF MATERIALS

Table 7.

Quantity	Reference Designator	Description	Part Number	Manufacturer
1	C1	0.1 µF, 0603 package, 16 V, X7R, surface mount device (SMD) ceramic capacitor	MCB0603R104KCT	Multicomp Pro
1	C2	47 pF, 0603 package, 100 V, C0G/NP0 capacitor	06031A470JAT2A	AVX Corporation
7	IN1 to IN4, EXT_EN, EXT_VCP, SPI/PIN	50 Ω SMB connector through holes	SMB1251B1-3GT30G-50	Amphenol
6	(IN1) to (IN4), (EXTD_EN), MODE, P1 to P4	3-pin silicone headers and shorting links	M20-9990345 and M7566-05	Harwin
1	P5	2-pin terminal block (5 mm pitch)	KRM 02	Lumberg
1	J4	FX8-120S-SV(21), 120-way connector, 0.6 mm pitch	FX8-120S-SV(21)	Hirose(HRS)
6	R1 to R6	10 kΩ (0603 package) SMD resistors	MC0063W0603110K	Multicomp
2	R7 to R8	100 kΩ (0603 package) SMD resistors	MC0063W06031100K	Multicomp Pro
1	R9	Not populated	Not applicable	Not applicable
7	R10 to R16	10 MΩ (0201 package) SMD resistors, not populated	Not applicable	Not applicable
9	RF1 to RF6, RFC	50 Ω side launch SMA connectors	32K243-40ML5	Rosenberger
1	U1	0 Hz/dc to 14 GHz, single-pole, four-throw MEMS switch with integrated driver	ADGM1304	Analog Devices
1	U2	24LC32A-I/MS, 32 kΩ, I^{2}C serial electronically erasable programmable read-only memory (EEPROM)	24LC32A-I/MS	Microchip
3	Not applicable[1]	Wideband 50 Ω termination SMA loads	PE6081	Pasternack

[1] Screwed on at measurement time (see Figure 1).

I^{2}C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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