

## Automotive MOSFET

## OptiMOS™ 6 Power-Transistor



## Features

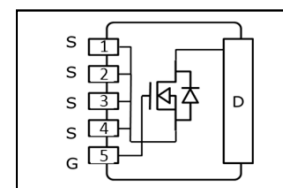
- OptiMOS™ power MOSFET for automotive applications
- N-channel – Enhancement mode – Normal Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL3 up to 260°C peak reflow
- 175°C operating temperature
- Green product (RoHS compliant)
- 100% Avalanche tested

## Potential applications

General automotive applications.

## Product validation

Qualified for automotive applications. Product validation according to AEC-Q101.



## Product Summary

$V_{DS}$	40	V
$R_{DS(on),max}$	0.7	mΩ
$I_D$ (chip limited)	380	A

Type	Package	Marking
IAUA250N04S6N007E	PG-HSOF-5-1	6N04R7E



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## Maximum ratings

at  $T_j=25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$V_{GS} = 10\text{ V}$ , Chip limitation <sup>1,2)</sup>	380	A
		$V_{GS} = 10\text{ V}$ , DC current <sup>3)</sup>	250	
		$T_a = 85\text{ °C}$ , $V_{GS} = 10\text{ V}$ , $R_{thJA}$ on 2s2p <sup>2,4)</sup>	55	
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	$T_C = 25\text{ °C}$ , $t_p = 100\text{ }\mu\text{s}$	1300	
Avalanche energy, single pulse <sup>2)</sup>	$E_{AS}$	$I_D = 55\text{ A}$ , $R_{G,min} = 25\text{ }\Omega$	560	mJ
Avalanche current, single pulse	$I_{AS}$	$R_{G,min} = 25\text{ }\Omega$	110	A
Gate source voltage	$V_{GS}$	-	$\pm 20$	V
Power dissipation	$P_{tot}$	$T_C = 25\text{ °C}$	192	W
Operating and storage temperature	$T_j, T_{stg}$	-	-55 ... +175	°C

**Thermal characteristics<sup>2)</sup>**

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal resistance, junction - case	$R_{thJC}$	–	–	–	0.78	K/W
Thermal resistance, junction - ambient <sup>4)</sup>	$R_{thJA}$	–	–	22.9	–	

**Electrical characteristics**

 at  $T_j=25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Static characteristics**

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	40	–	–	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 110\text{ }\mu\text{A}$	2.2	2.6	3.0	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 40\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_j = 25\text{ °C}$	–	–	1	$\mu\text{A}$
		$V_{DS} = 40\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_j = 125\text{ °C}^{2)}$	–	–	31	
Gate-source leakage current	$I_{GSS}$	$V_{GS} = 20\text{ V}$ , $V_{DS} = 0\text{ V}$	–	–	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 7\text{ V}$ , $I_D = 100\text{ A}$	–	0.65	0.83	m $\Omega$
		$V_{GS} = 10\text{ V}$ , $I_D = 100\text{ A}$	–	0.55	0.70	
Gate resistance <sup>2)</sup>	$R_G$	–	–	1	–	$\Omega$

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics<sup>2)</sup>**

Input capacitance	$C_{iss}$	$V_{GS} = 0 \text{ V}, V_{DS} = 25 \text{ V},$ $f = 1 \text{ MHz}$	-	6444	8377	pF
Output capacitance	$C_{oss}$		-	1944	2528	
Reverse transfer capacitance	$C_{rss}$		-	94	124	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 32 \text{ V}, V_{GS} = 10 \text{ V},$ $I_D = 250 \text{ A}, R_G = 3.5 \Omega$	-	13	-	ns
Rise time	$t_r$		-	14	-	
Turn-off delay time	$t_{d(off)}$		-	27	-	
Fall time	$t_f$		-	19	-	

**Gate Charge Characteristics<sup>2)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD} = 32 \text{ V}, I_D = 250 \text{ A},$ $V_{GS} = 0 \text{ to } 10 \text{ V}$	-	28	36	nC
Gate to drain charge	$Q_{gd}$		-	19	29	
Gate charge total	$Q_g$		-	94	128	
Gate plateau voltage	$V_{plateau}$		-	4.2	-	V

**Reverse Diode**

Diode continuous forward current <sup>2)</sup>	$I_S$	$T_C = 25 \text{ °C}$	-	-	250	A
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$	$T_C = 25 \text{ °C}, t_p = 100 \mu\text{s}$	-	-	1300	
Diode forward voltage	$V_{SD}$	$V_{GS} = 0 \text{ V}, I_F = 125 \text{ A},$ $T_j = 25 \text{ °C}$	-	0.8	1.1	V
Reverse recovery time <sup>2)</sup>	$t_{rr}$	$V_R = 20 \text{ V}, I_F = 50 \text{ A},$ $di_F/dt = 100 \text{ A}/\mu\text{s}$	-	60	-	ns
Reverse recovery charge <sup>2)</sup>	$Q_{rr}$		-	73	-	nC

<sup>1)</sup> Current is limited by the overall system design and the customer-specific PCB.

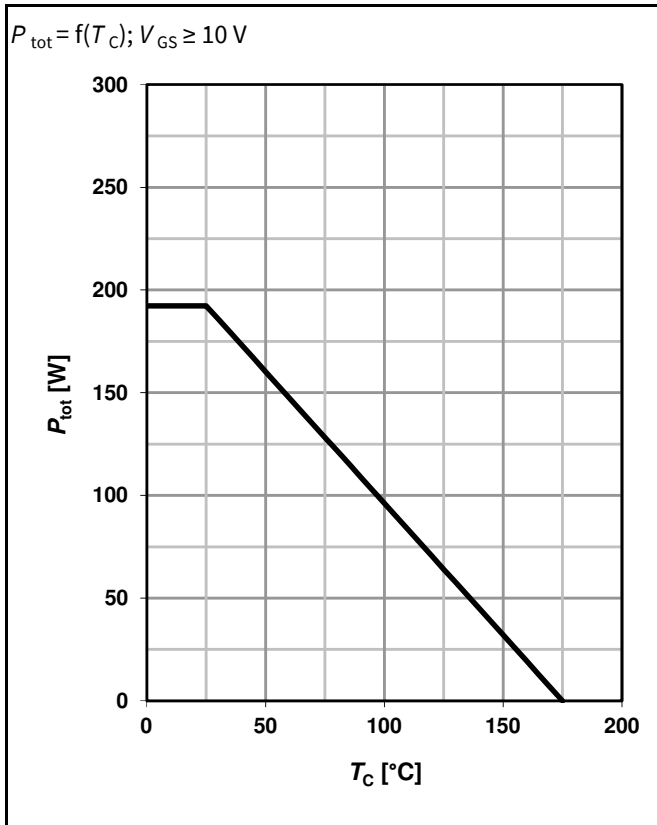
<sup>2)</sup> The parameter is not subject to production testing – specified by design.

<sup>3)</sup> Current is limited by the package.

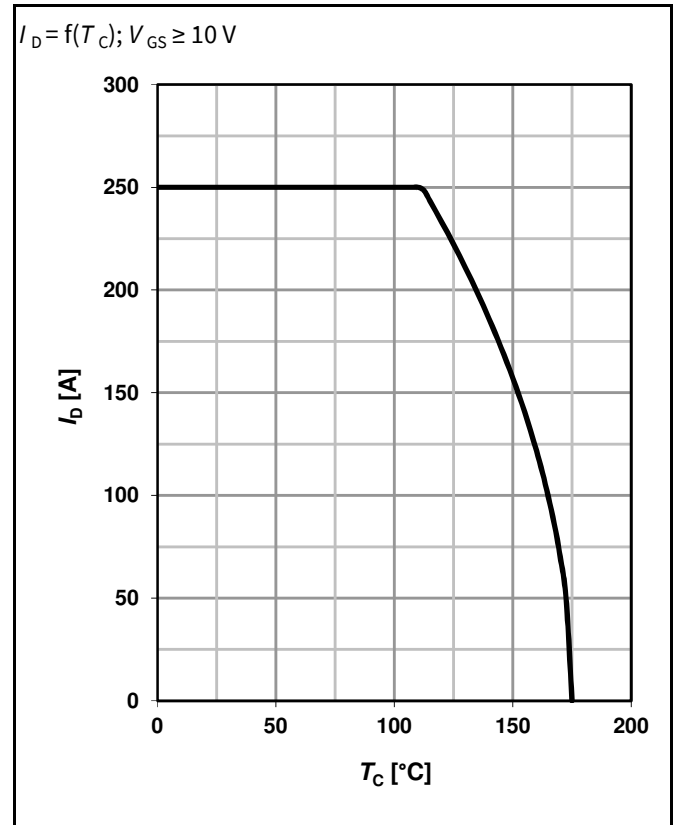
<sup>4)</sup> Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

### Electrical characteristics diagrams

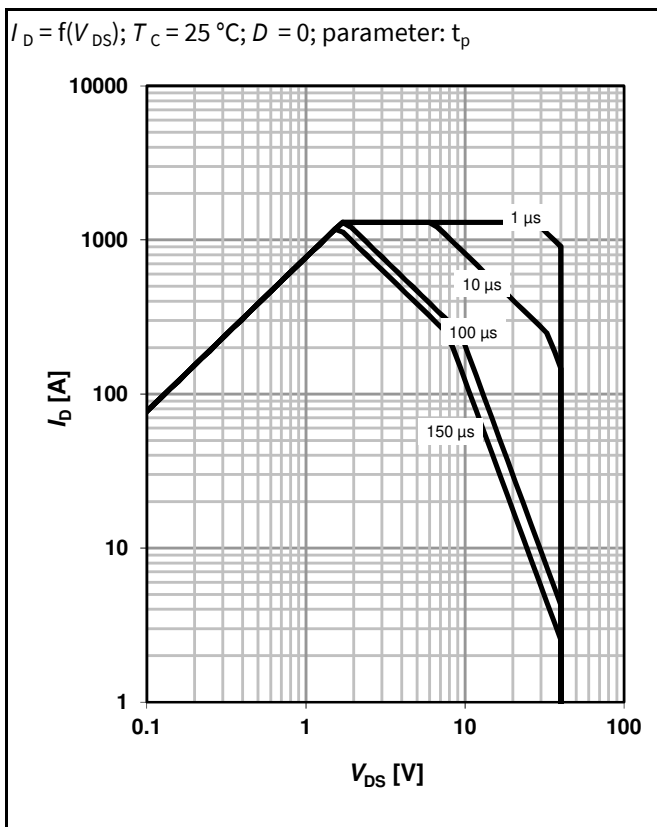
1 Power dissipation



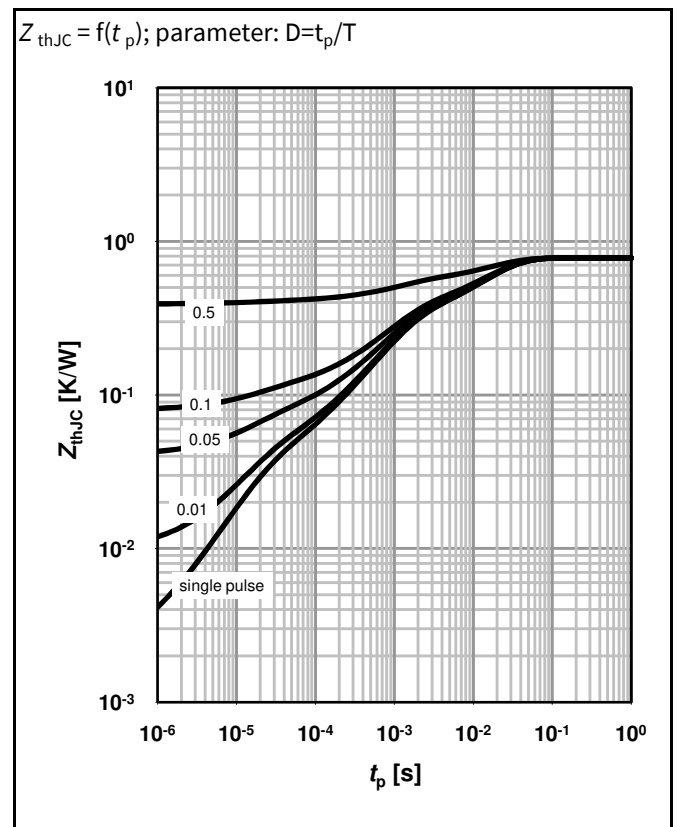
2 Drain current



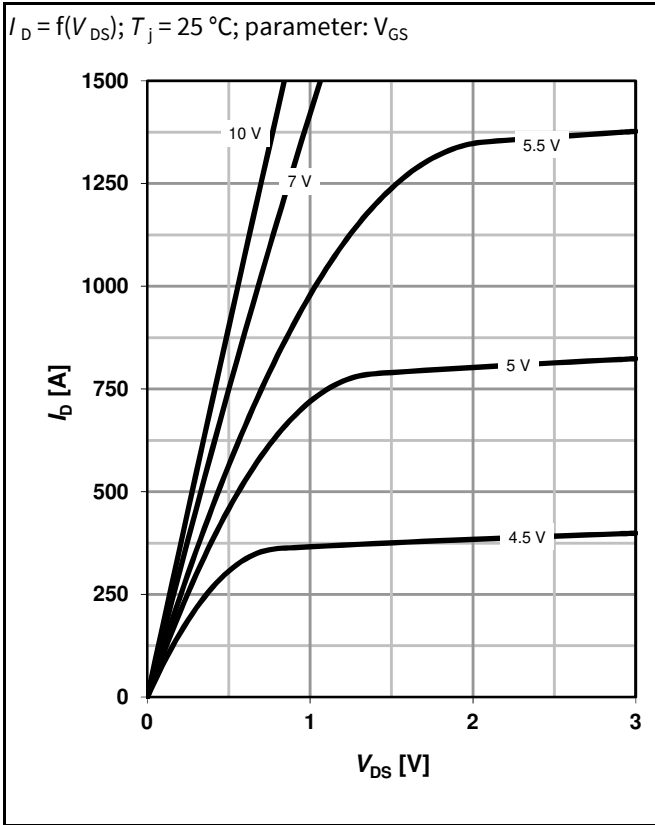
3 Safe operating area



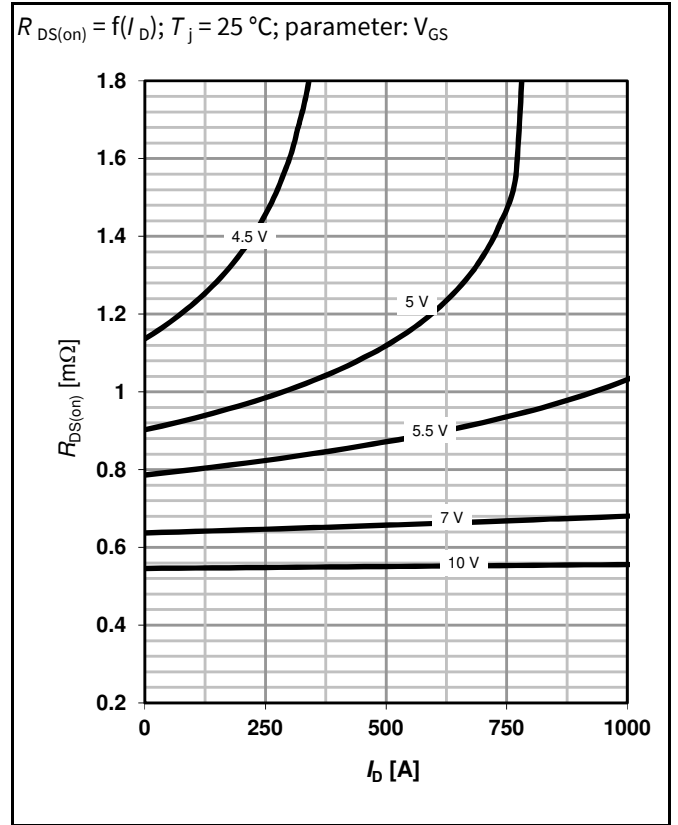
4 Max. transient thermal impedance



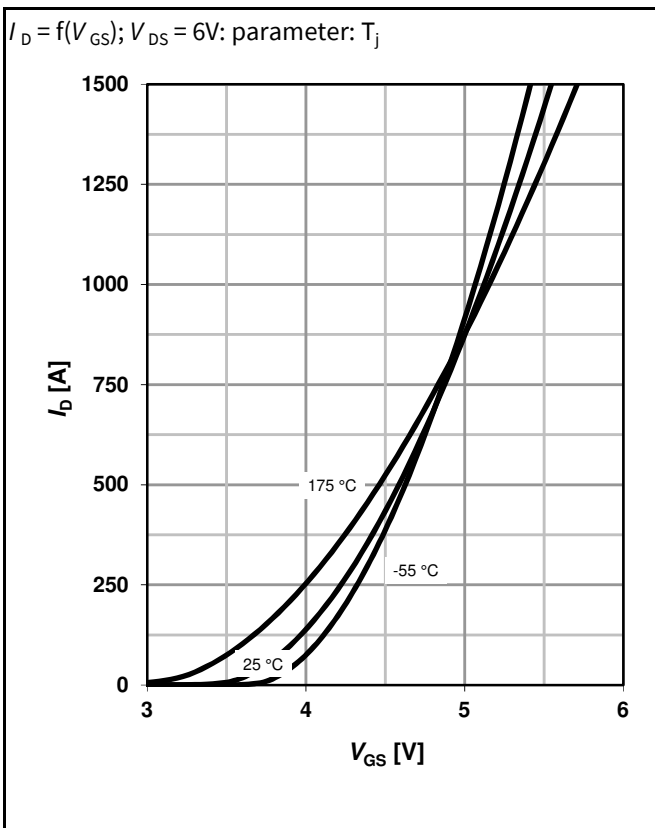
5 Typ. output characteristics



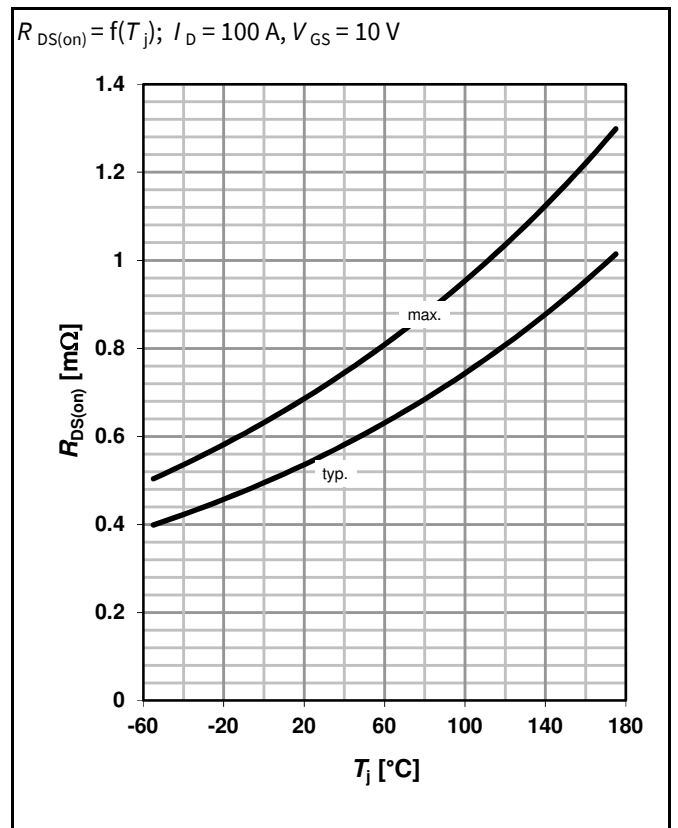
6 Typ. drain-source on-state resistance



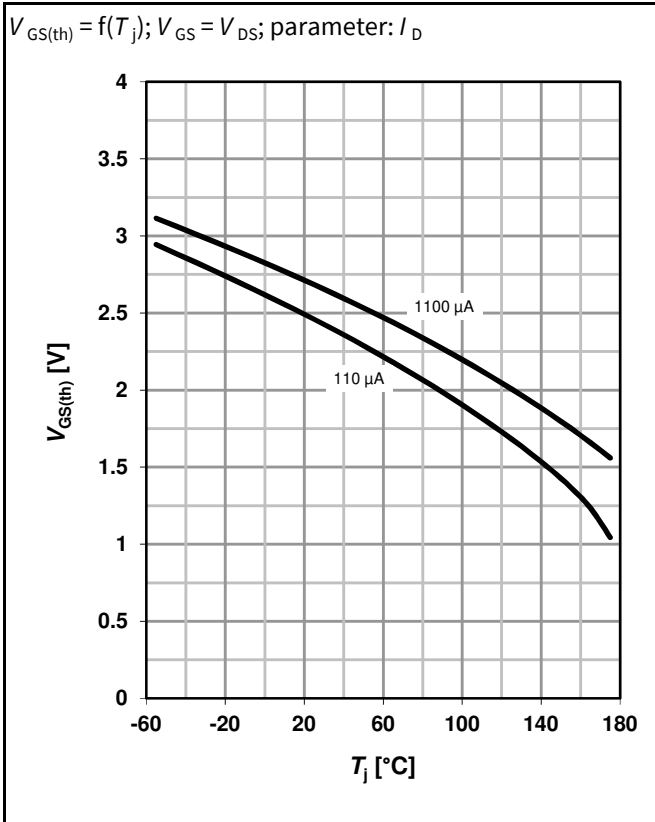
7 Typ. transfer characteristics



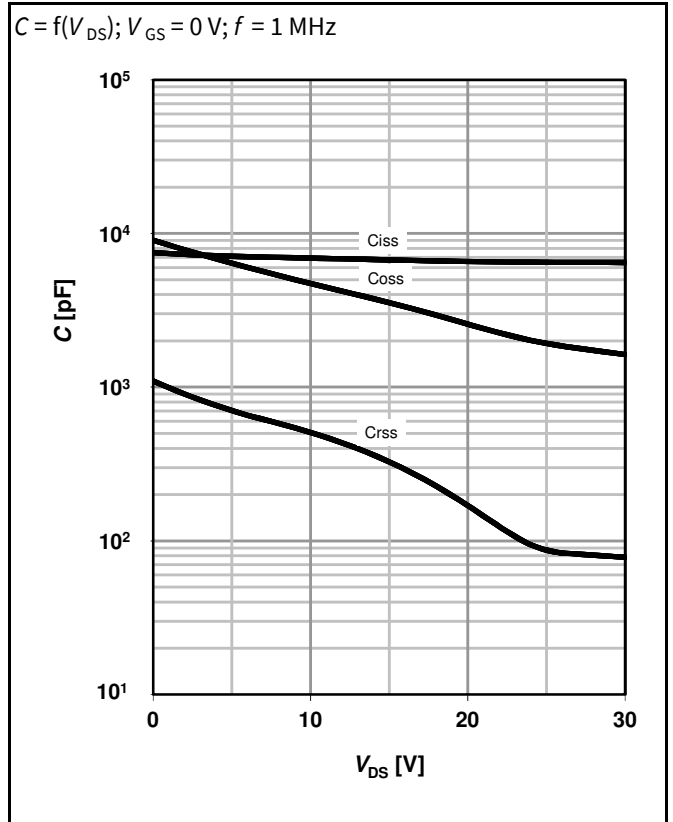
8 Typ. drain-source on-state resistance



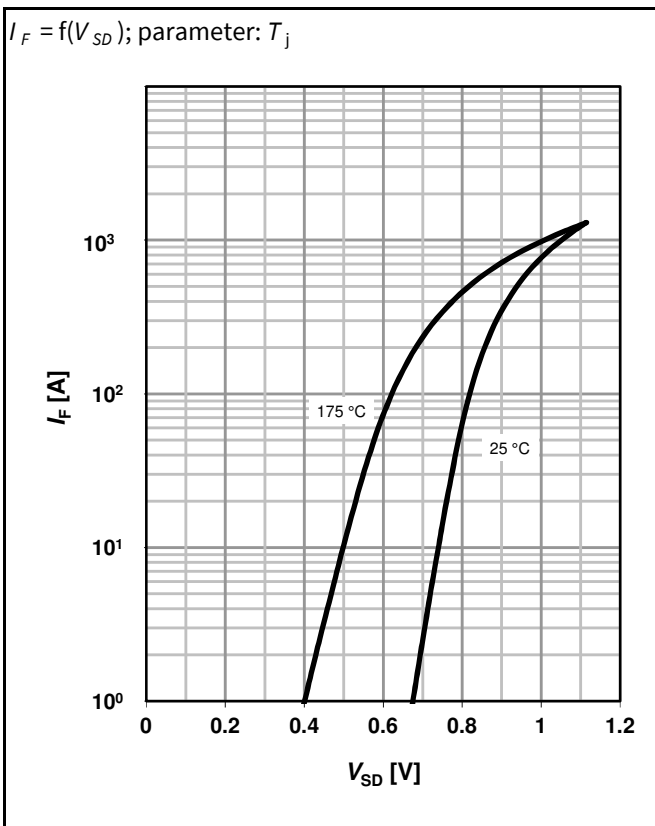
9 Typ. gate threshold voltage



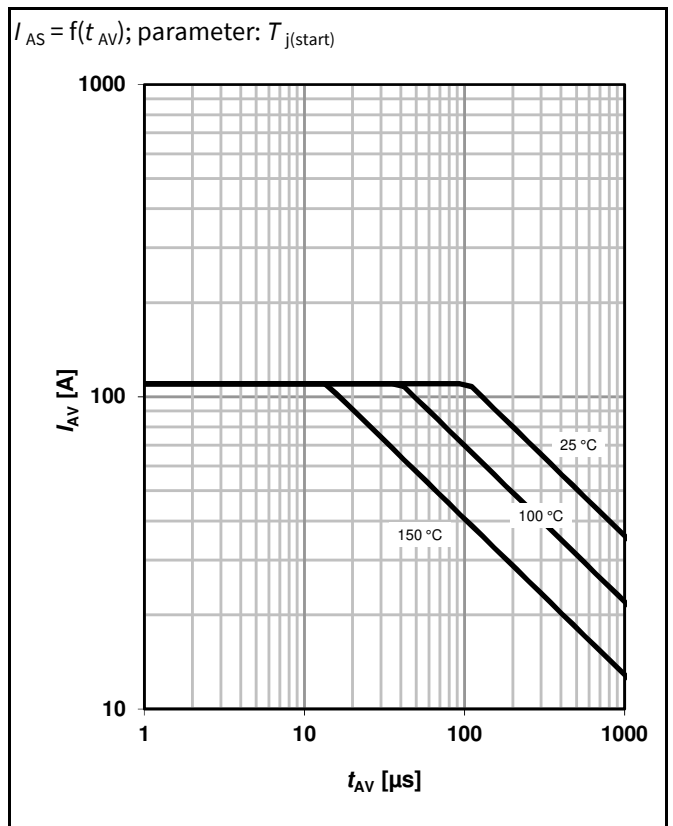
10 Typ. capacitances



11 Typical forward diode characteristics

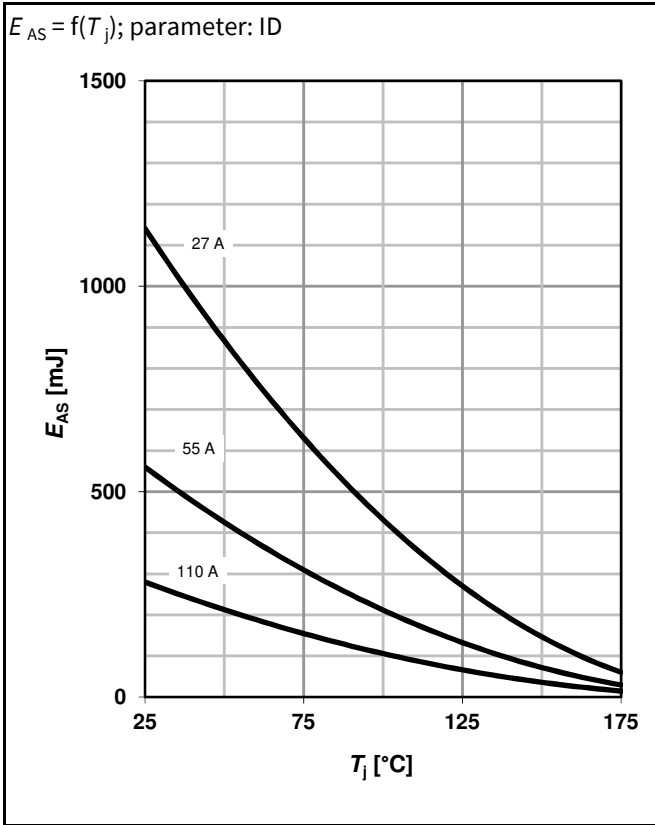


12 Typ. avalanche characteristics

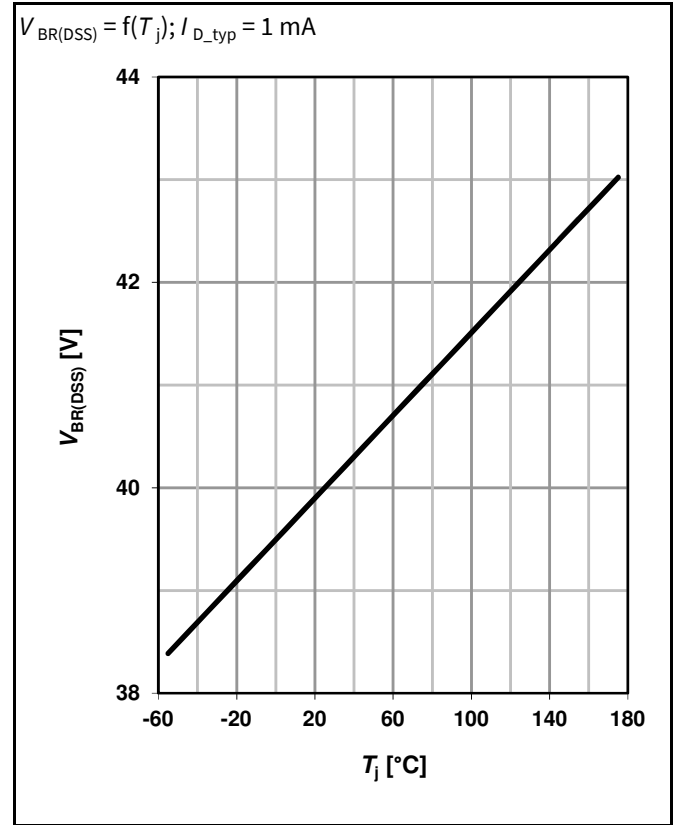




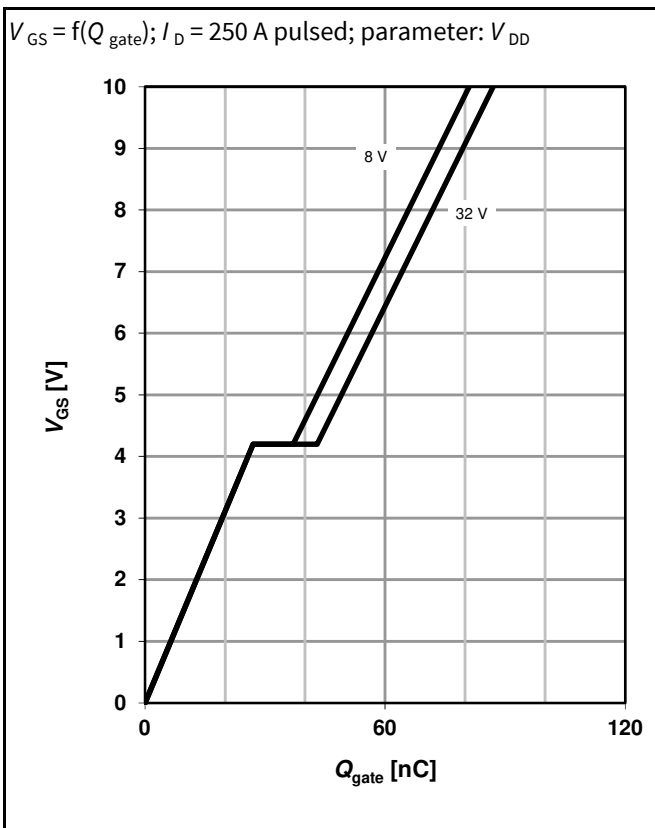
13 Typical avalanche energy



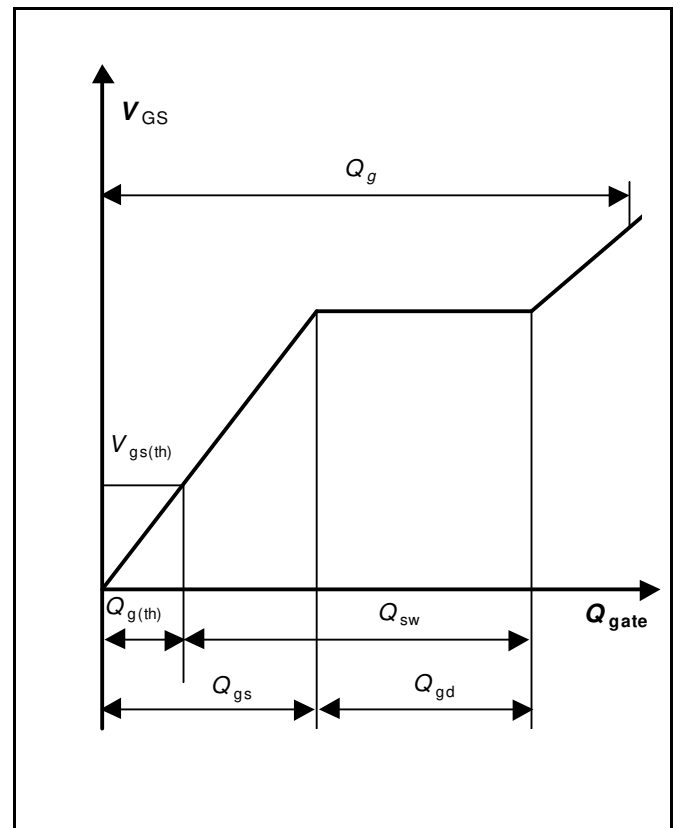
14 Drain-source breakdown voltage



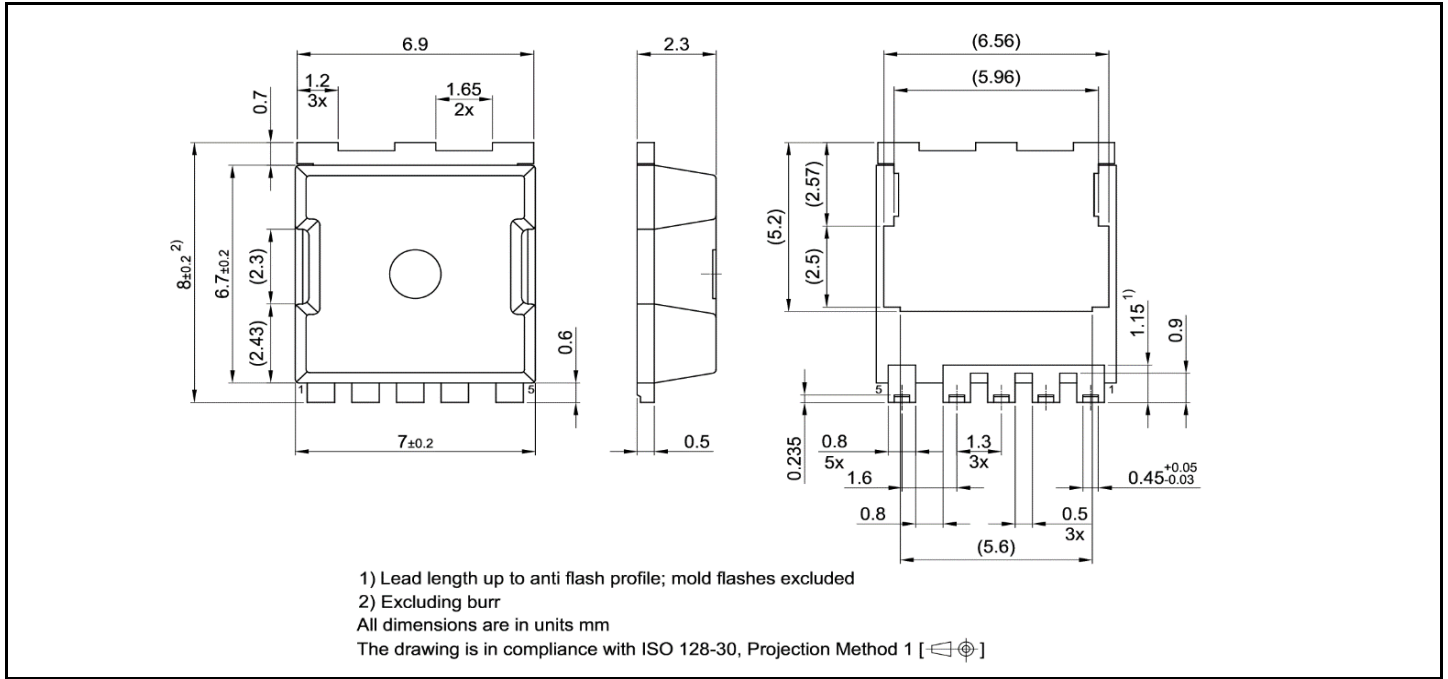
15 Typ. gate charge



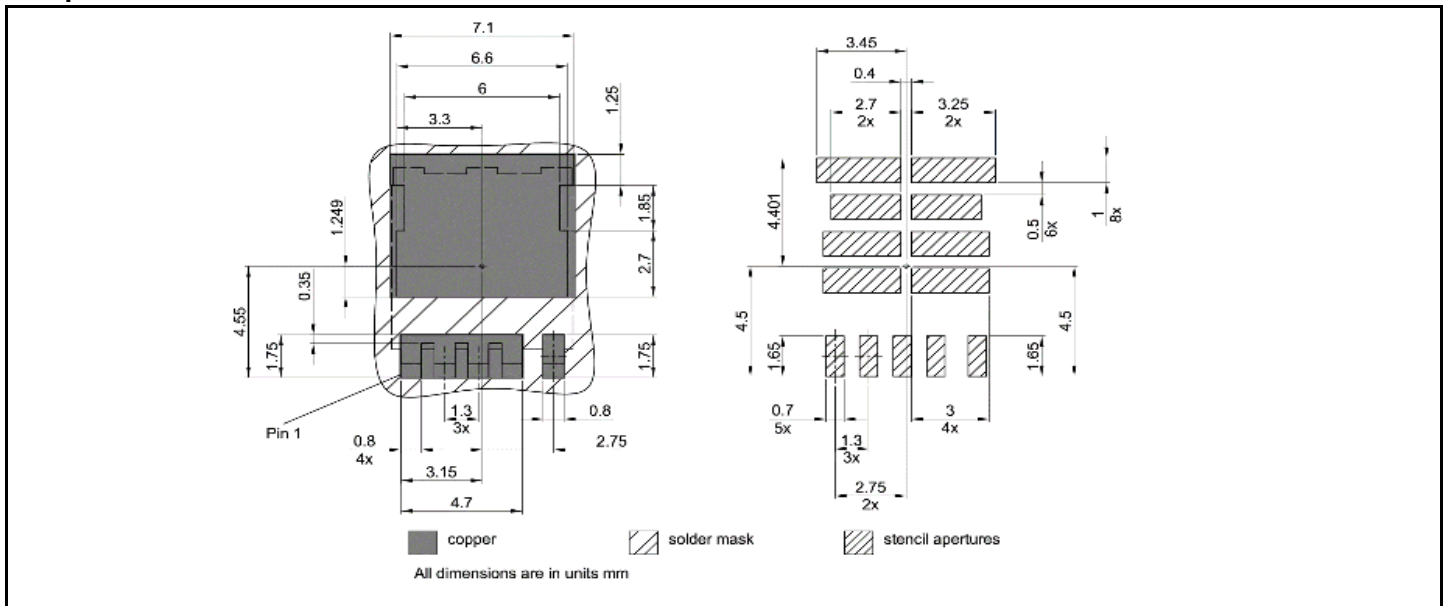
16 Gate charge waveforms



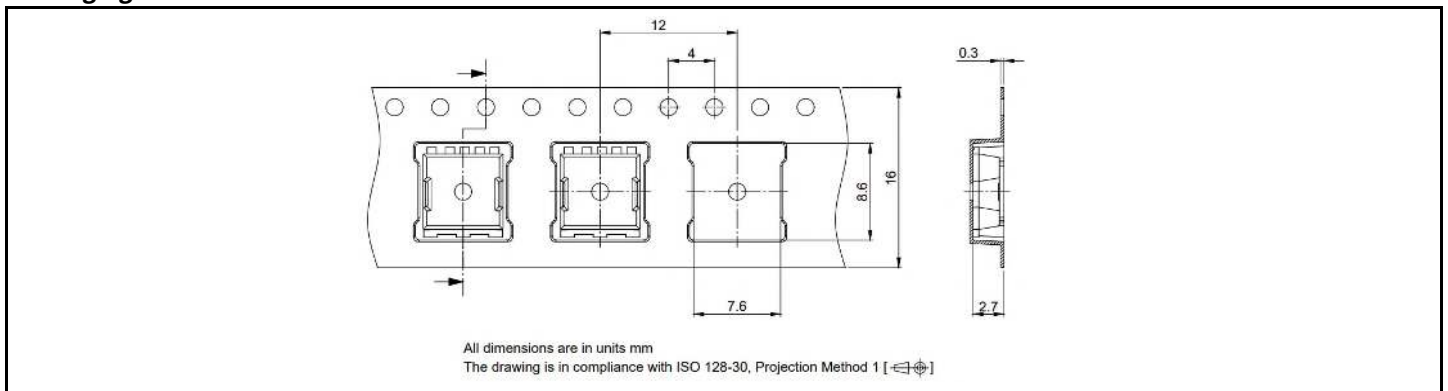
## Package Outline



## Footprint



## Packaging





## Revision History

Revision	Date	Changes
Revision 1.0	24.01.2022	Final Data Sheet

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