MP2131

High Efficiency, 4 A, 5.5 V, 1.2 MHz Synchronous Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP2131 is a monolithic step-down, switch-mode converter with built-in internal power MOSFETs. It achieves a 4 A continuous output current from a 2.7 V to 5.5 V input voltage with excellent load and line regulation. The MP2131 is ideal for powering portable equipment that run from a single cell lithium-ion (Li+) battery. The output voltage is regulated as low as 0.6 V.

The constant-on-time (COT) control scheme provides fast transient response, high light-load efficiency, and eases loop stabilization.

Fault condition protection includes cycle-by-cycle current limit and thermal shutdown.

The MP2131 requires a minimum number of readily available, standard, external components and is available in an ultra-small QFN-12 (2mm x 2mm) package.

The MP2131 is ideal for a wide range of applications including portable instruments, small handheld and battery–powered devices, PDAs, and DVD drives.

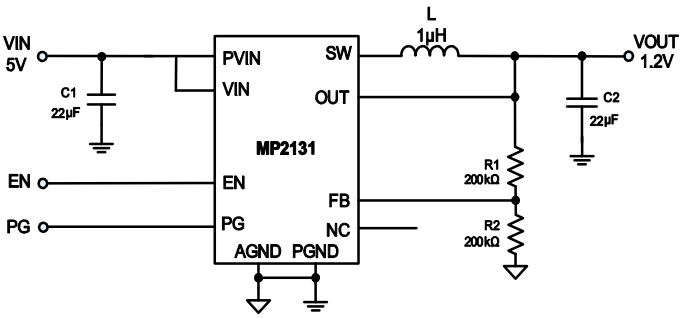
FEATURES

- Wide 2.7 V to 5.5 V Operating Input Range
- Output Voltage as Low as 0.6 V
- 4 A Output Current
- 35 mΩ and 18 mΩ Internal Power MOSFET
- Above 96% Peak Efficiency
- Above 80% Light Load Efficiency
- Low IQ: 19 μA
- 1.2 MHz Frequency
- 100% Duty Cycle in Dropout
- 0.5 ms Internal Soft-Start Time
- EN and Power Good for Power Sequencing
- Auto Discharge at EN Off
- Short-Circuit Protection with Hiccup Mode
- Available in a QFN-12 (2mm x 2mm) Package

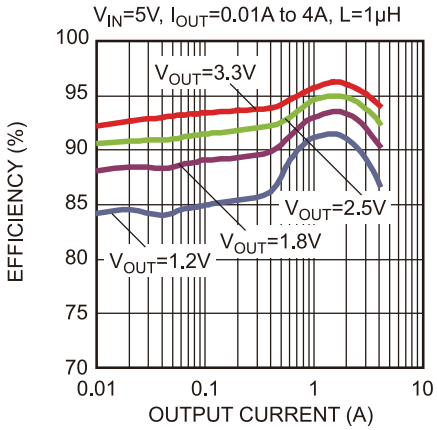
APPLICATIONS

- Storage Drives
- Portable/Handheld Devices
- Wireless/Networking Cards
- Low Voltage I/O System Power

TYPICAL APPLICATION



Efficiency vs. Output Current



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2131GG	QFN-12 (2mm x 2mm)	*See Below*

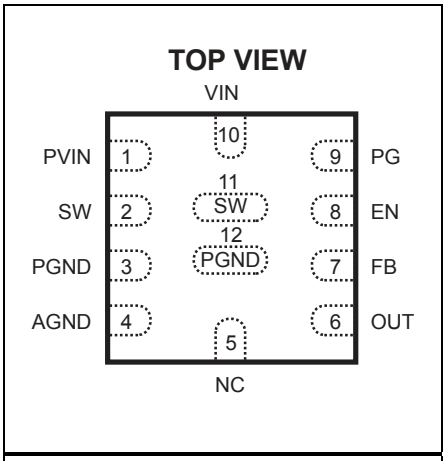
* For Tape & Reel, add suffix –Z (e.g. MP2131GG–Z)

TOP MARKING

CAY
LLL

CA: Product code of MP2131GG
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



QFN-12 (2mm x 2mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) ..... 6.5 V
V_{SW} .....
-0.3 V (-3 V for <10 ns) to 6.5 V (8 V for <10 ns)
All other pins ..... -0.3 V to 6.5 V
Junction temperature ..... 150°C
Lead temperature..... 260°C
Continuous power dissipation (T_A = +25°C) **(2)**
……..... 1.6 W
Storage temperature .....-65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 2.7V to 5.5V
Operating junction temp. (T_J)....-40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-12 (2mm x 2mm)……	80 …	16 °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will produce an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6 V, T_J = -40°C to +125°C, typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Feedback voltage	V_{FB}	2.7 V ≤ V_{IN} ≤ 5.5 V, T_J = 25°C	594	600	606	mV
Feedback voltage	V_{FB}	2.7 V ≤ V_{IN} ≤ 5.5 V	588	600	612	mV
Feedback current	I_{FB}	V_{FB} = 0.63 V		10	50	nA
PFET switch on resistance	R_{DSON_P}	V_{IN} = 5 V		35		mΩ
NFET switch on resistance	R_{DSON_N}	V_{IN} = 5 V		18		mΩ
Switch leakage		V_{EN} = 0 V, V_{IN} = 5.5 V V_{SW} =0 V and 5.5 V, T_J=25°C		0	5	μA
PFET peak current limit(5)		T_J=25°C	5.5	7.5		A
NFET valley current limit(5)				3.5		A
On time	T_{ON}	V_{IN} = 5 V, V_{OUT} = 1.2 V		200		ns
		V_{IN} = 3.6 V, V_{OUT} = 1.2 V		280		
Switching frequency	F_s	V_{OUT} =1.2 V		1200		kHz
Minimum off time	$T_{MIN-OFF}$			100		ns
Minimum on time(6)	T_{MIN-On}			80		ns
Soft-start time	T_{SS-ON}	From 10% V_{OUT} to 90% V_{OUT}		0.5		ms
Soft-stop time	T_{SS-OFF}	From 90% V_{OUT} to 10% V_{OUT}		0.8		ms
Power good upper trip threshold		FB with respect to the regulation		+10		%
Power good lower trip threshold				-10		%
Power good delay		Rising		90		μs
Power good sink current capability	V_{PG_LO}	Sink 1 mA			0.4	V
Power good logic-high voltage	V_{PG_HI}	V_{IN} = 5 V,V_{FB} = 0.63 V	4.9			V
Power good internal pull-up resistor	R_{PG}			400		kΩ
Under-voltage lockout threshold—rising		-40°C ≤ T_J ≤ 85°C		2.48	2.68	V
Under-voltage lockout threshold—hysteresis				450		mV

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6 V, T_J = -40°C to +125°C, typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
EN input logic-low voltage					0.4	V
EN input logic-high voltage			1.2			V
EN input current		V_{EN} = 2 V		2		µA
		V_{EN} = 0 V		0		µA
Supply current (shutdown)		V_{EN} = 0 V, T_J = 25°C		0	1	µA
Supply current (quiescent)		V_{EN} = 2 V, V_{FB} = 0.63 V, V_{IN} = 3.6 V, T_J = 25°C		19	25	µA
Thermal shutdown(6)				155		°C
Thermal hysteresis(6)				25		°C

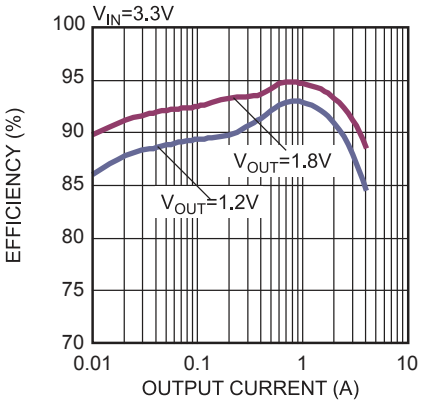
NOTES:

5) Guaranteed by engineering sample characterization.
6) Guaranteed by design.

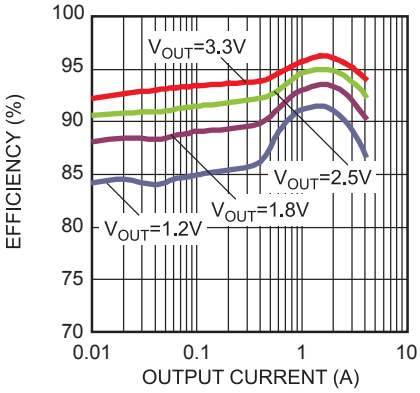
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the design example section.
V_{IN} = 5 V, V_{OUT} = 1.2 V, L = 1 µH, T_A = +25ºC, unless otherwise noted.

Efficiency vs. Output Current

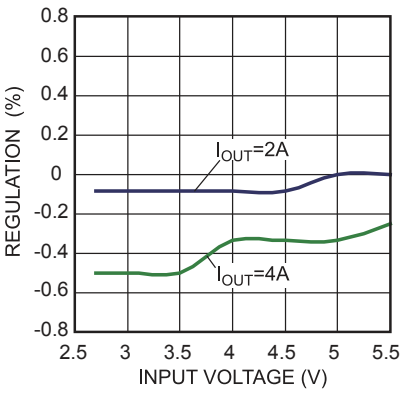


Efficiency vs. Output Current



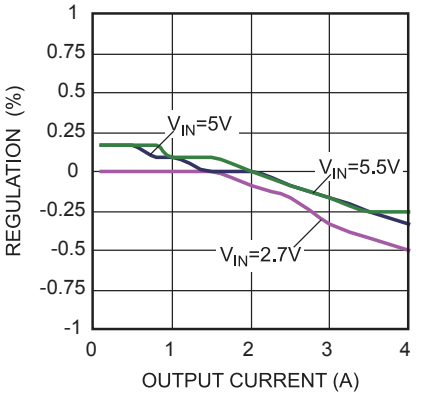
Line Regulation

V_{IN}=2.7V-5.5V



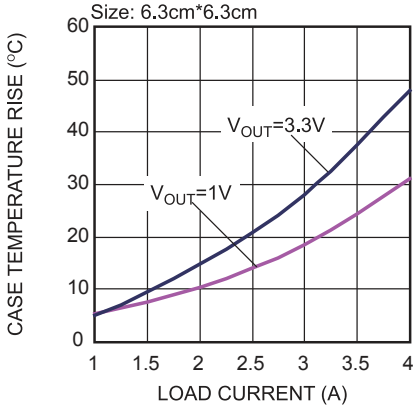
Load Regulation

V_{IN}=2.7V/5V/5.5V, I_{OUT}=0.1A-4A

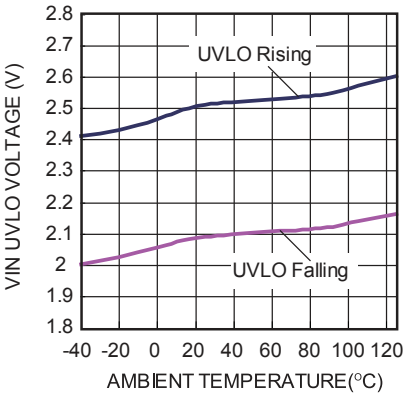


Case Temperature Rise vs. Output Current

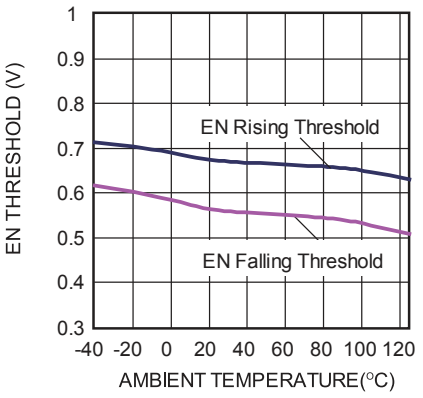
I_{OUT}=0A-4A, 4 layers PCB,
Size: 6.3cm*6.3cm



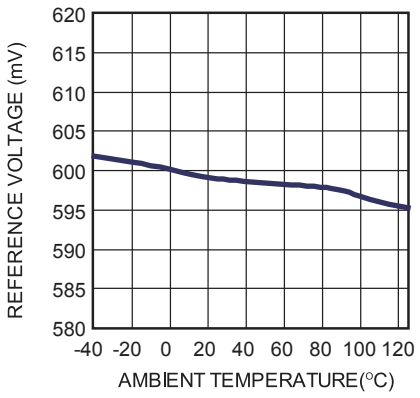
V_{IN} UVLO vs. Temperature



EN Threshold vs. Temperature



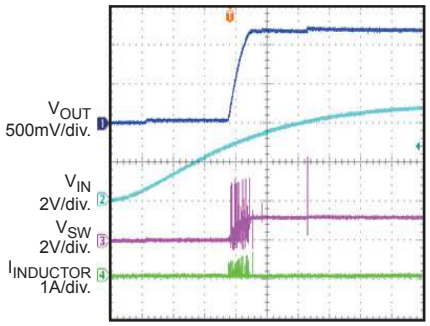
Reference Voltage vs. Temperature



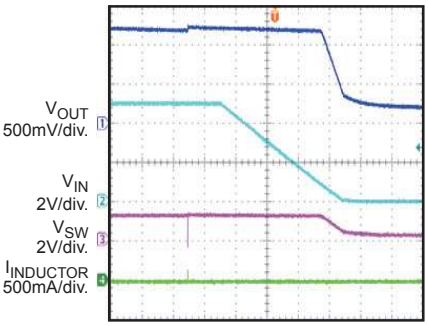
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the design example section.
V_{IN} = 5 V, V_{OUT} = 1.2 V, L = 1 µH, T_A = +25ºC, unless otherwise noted.

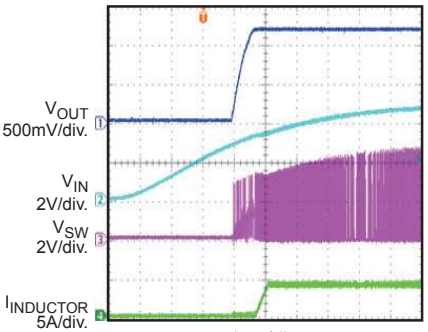
Start-Up through Input Voltage
I_{OUT}= 0A



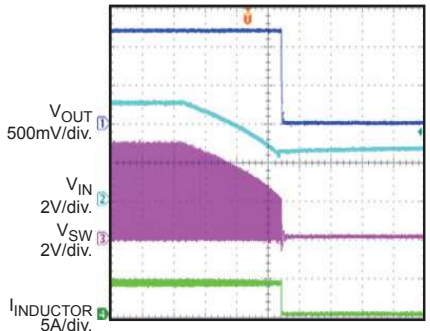
Shutdown through Input Voltage
I_{OUT}= 0A



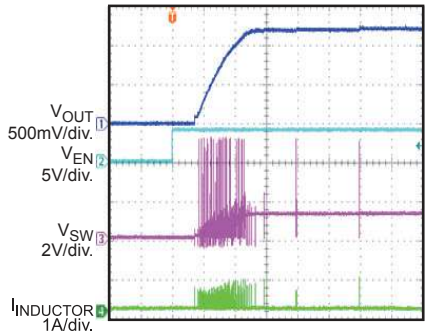
Start-Up through Input Voltage
I_{OUT}= 4A



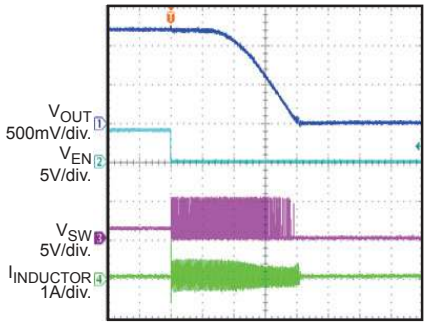
Shutdown through Input Voltage
I_{OUT}= 4A



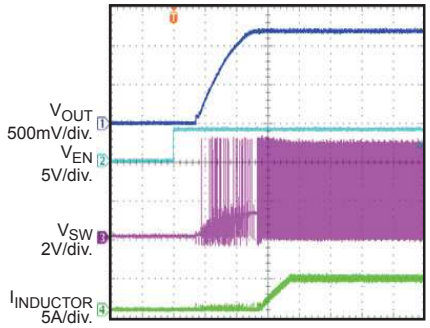
Start-Up through Enable
I_{OUT}= 0A



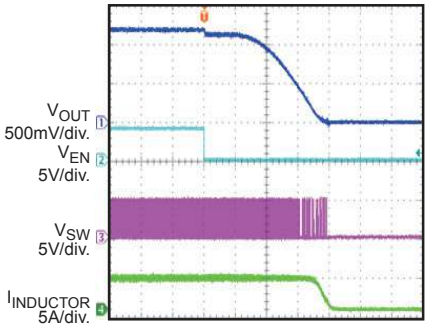
Shutdown through Enable
I_{OUT}= 0A



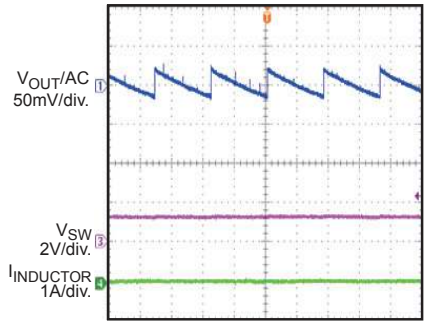
Start-Up through Enable
I_{OUT}= 4A



Shutdown through Enable
I_{OUT}= 4A



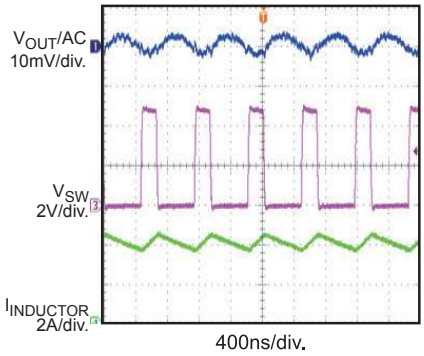
Output Ripple
I_{OUT}= 0A



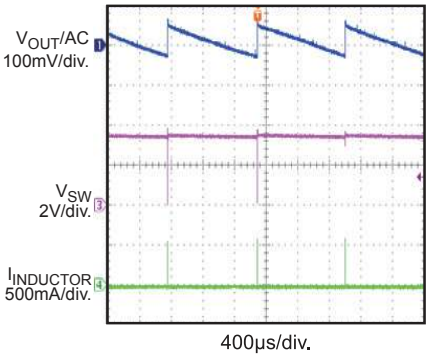
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the design example section.
V_{IN} = 5 V, V_{OUT} = 1.2 V, L = 1 µH, T_A = +25ºC, unless otherwise noted.

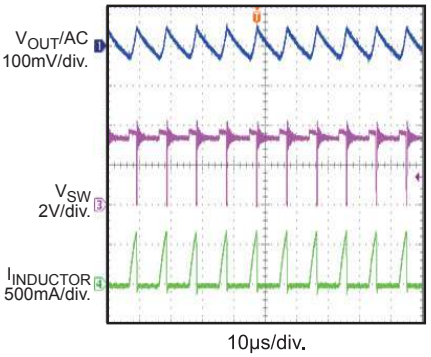
Output Ripple
I_{OUT}= 4A



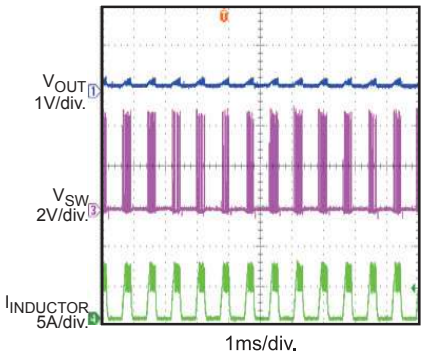
Output Ripple
V_{IN}=3.6V, V_{OUT}=3.3V, I_{OUT}= 0A



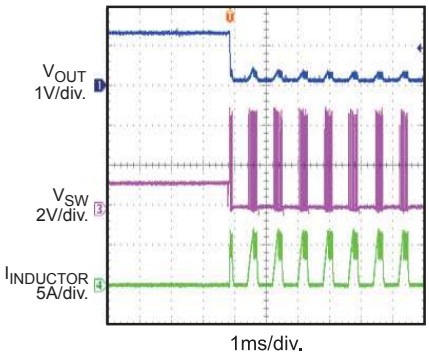
Output Ripple
V_{IN}=3.6V, V_{OUT}=3.3V, I_{OUT}= 0.1A



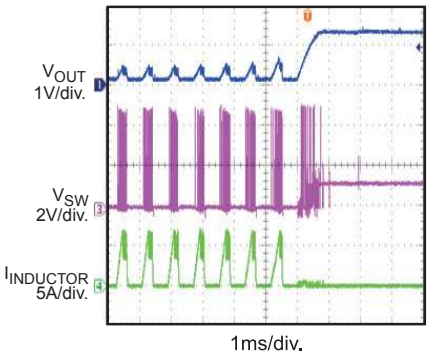
Short-Circuit Steady State



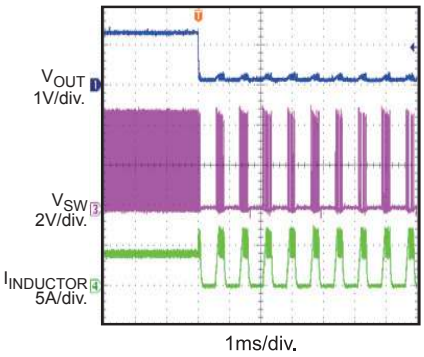
Short-Circuit Entry
I_{OUT}= 0A



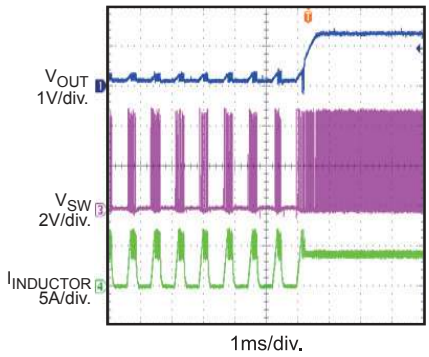
Short-Circuit Recovery
I_{OUT}= 0A



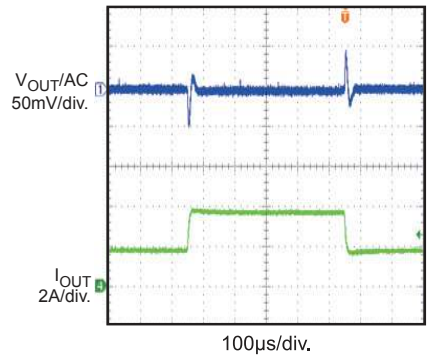
Short-Circuit Entry
I_{OUT}= 4A



Short-Circuit Recovery
I_{OUT}= 4A



Transient Response
I_{OUT}=2A to 4A, 2.5A/µs



PIN FUNCTIONS

Pin #	Name	Description
1	PVIN	**Supply voltage to power FETs.** PVIN is connected to VIN internally.
2, 11	SW	**Switch output.** Pin 2 and pin 11 can be connected together.
3, 12	PGND	**Power ground.** Pin 3 and pin 12 can be connected together.
4	AGND	**Quiet ground for controller circuits.**
5	NC	**No connection.** Leave NC open.
6	OUT	**Input sense pin for output voltage.**
7	FB	**Feedback.** An external resistor divider from the output to GND (tapped to FB) sets the output voltage.
8	EN	**On/off control.**
9	PG	**Power good indicator.** The output of PG is an open drain with an internal pull-up resistor to VIN. PG is pulled up to VIN when the FB voltage is within 10% of the regulation level; otherwise it is low.
10	VIN	**Supply voltage to internal control circuitry.** VIN is connected to PVIN internally.

FUNCTIONAL BLOCK DIAGRAM

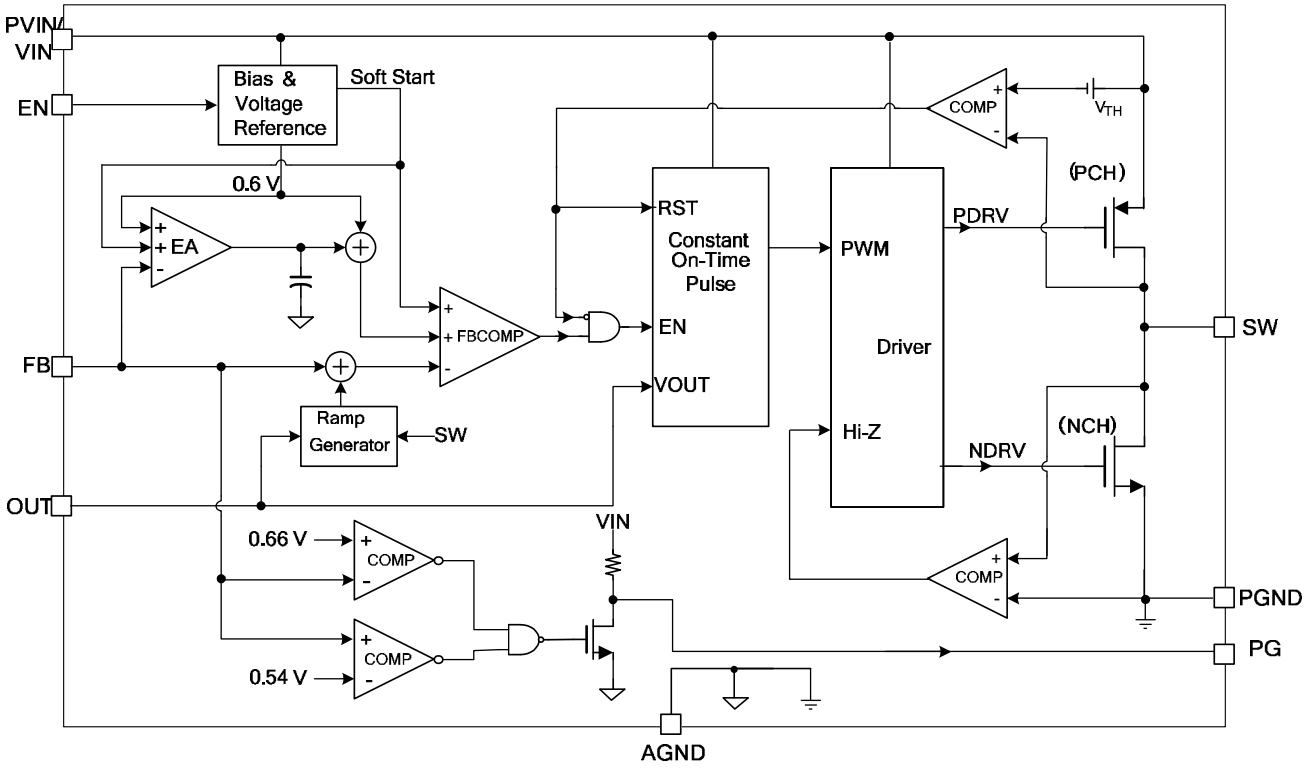


Figure 1—Functional block diagram

OPERATION

The MP2131 uses constant-on-time (COT) control with input voltage feed forward to stabilize the switching frequency over a full input range. At light load, the MP2131 employs a power-save mode that forces the part to operate in discontinuous conduction mode (DCM) to improve efficiency.

Constant-On-time (COT) Control

Compared to fixed frequency PWM control, constant-on-time (COT) control offers the advantage of a simpler control loop and faster transient response. By using input voltage feed forward, the MP2131 maintains a nearly constant switching frequency across the input and output voltage range. The on time of the switching pulse can be estimated using Equation (1):

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 0.833\mu s \quad (1)$$

To prevent inductor current runaway during load transient, the MP2131 fixes the minimum off time at 100 ns. However, this minimum off time limit will not affect operation in steady state.

AAM Operation at Light Operation

The MP2131 has advanced asynchronous modulation (AAM) power-save mode with a current zero-crossing detector (ZCD) circuit for light load.

AAM current (I_{AAM}) is fixed internally. If the high-side MOSFET (HS-FET) on time is less than the AAM blanking time (600 ns, typically), AAM is disabled, and the HS-FET on time is determined by the loop. Otherwise, the HS-FET turns on until I_L reaches the value set by the AAM current. Simplified AAM control is shown in Figure 2.

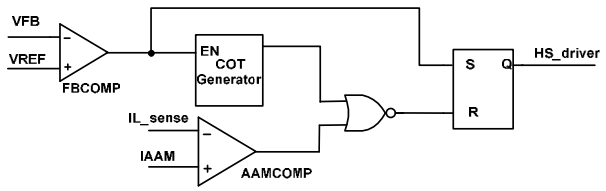


Figure 2—Simplified AAM control logic

The AAM threshold decreases as Ton gradually increases (see Figure 3).

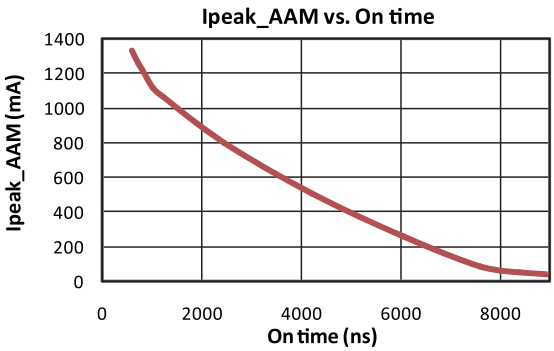


Figure 3—AAM vs. on time

The MP2131 has a current zero-crossing detector (ZCD) circuit to monitor if the inductor current begins to reverse. When the inductor current reaches the ZCD threshold, the low-side MOSFET (LS-FET) is turned off.

The combination of AAM mode and the ZCD circuit allow the MP2131 to always operate in DCM at light load, even if the V_{OUT} voltage is close to V_{IN}.

Enable (EN)

When the input voltage is greater than the under-voltage lockout threshold (2.48 V, typically), the MP2131 is enabled by pulling EN higher than 1.2 V. Floating EN or pulling it down to ground disables the MP2131. There is an internal 1 megohm resistor from EN to ground.

Soft Start/Stop

The MP2131 has a built-in soft start that ramps up the output voltage in a controlled slew rate, avoiding overshoot at start-up. The soft-start time is about 0.5 ms typically. When EN shuts down, ZCD is disabled, and the MP2131 ramps down the internal reference, thus allowing the load to discharge the output linearly. The soft-stop time is typically 0.8 ms.

Power Good Indicator (PG)

The MP2131 has an open drain with a 400 kΩ pull-up resistor pin for the power good indicator (PG). When FB is within +/-10% of the regulation voltage (i.e., 0.6 V), PG is pulled up to VIN by the internal resistor. If the FB voltage is out of the +/-10% window, PG is pulled down

to ground by an internal MOSFET. The MOSFET as a maximum Rdson of less than 100 Ω.

Current Limit

The MP2131 has a typical 7.5 A current limit for the HS-FET and a 3.5 A current limit for the LS-FET. Once the HS-FET hits the current limit, the HS-FET is turned off, and the LS-FET is turned on, reducing the inductor current. The LS-FET is turned off if the current drops to the valley current limit, which turns on the HS-FET. If the HS-FET hits the peak current limit and the LS-FET hits the valley current limit every cycle for 150 μs, the MP2131 will remain at the hiccup threshold until the current decreases. This prevents the inductor current from continuing to build up, which results in damage to the components.

Short Circuit and Recovery

If the output voltage of the buck converter is shorted to GND, the current limit is triggered. Once the current limit is triggered every cycle for 150 μs, the MP2131 enters hiccup mode; the MP2131 disables the output power stage, discharges the soft-start capacitor, and then automatically tries to soft-start again. If the short-circuit condition still holds after the soft-start ends, the MP2131 repeats this operation cycle until the short circuit is removed, and the output rises back to the regulation level.

APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see Typical Application on page 1). The feedback resistor R1 cannot have too large or too small a value considering the trade-off between a dynamic circuit and stability in the circuit. Choose R1 around 50 kΩ to 200 kΩ. Choose a larger resistance to get lower leakage or a smaller resistance to avoid noise. R2 is then given using Equation (2):

$$R2 = \frac{R1}{\frac{V_{out}}{0.6} - 1} \quad (2)$$

The feedback circuit is shown in Figure 4.

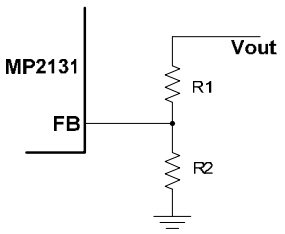


Figure 4—Feedback network

Table 1 lists the recommended resistor values for common output voltages.

Table 1—Resistor selection for common output voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.0	200(1%)	300(1%)
1.2	200(1%)	200(1%)
1.8	200(1%)	100(1%)
2.5	200(1%)	63.2(1%)
3.3	200(1%)	44.2(1%)

Selecting the Inductor

A 0.82 µH to 2.2 µH inductor is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 15 mΩ. For most designs, the inductance value is derived from Equation (3).

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_S} \quad (3)$$

Where ΔI_L is the inductor ripple current, and f_S is the switching frequency.

Choose an inductor current approximately 30 percent of the maximum load current. The maximum inductor peak current is calculated using Equation (4)

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (4)$$

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 22 µF capacitor is sufficient. For a higher output voltage, a 47 µF may be needed for a more stable system.

Since the input capacitor absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated using Equation (5) and Equation (6):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

The worse case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose an input capacitor with a RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, a small, high-quality ceramic capacitor (i.e., 0.1 µF) should be placed as close to the IC as possible. When using ceramic capacitors, make sure they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated using Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

Selecting the Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage.

Low ESR ceramic capacitors can be used to keep the output ripple low. Generally, a 22 µF output ceramic capacitor will suffice. For a higher output voltage condition, a 47 µF capacitor may be needed for a more stable system.

When using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is caused mainly by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

When using tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (9)

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (9)$$

The characteristics of the output capacitor affect the stability of the regulation system.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 5 and follow the guidelines below:

1. Place the input decoupling capacitor as close as possible to the IC pins (a 0805 ceramic capacitor is used).
2. Ensure the two ends of the ceramic capacitor are connected directly to PVIN (pin 1) and PGND (pin 3).

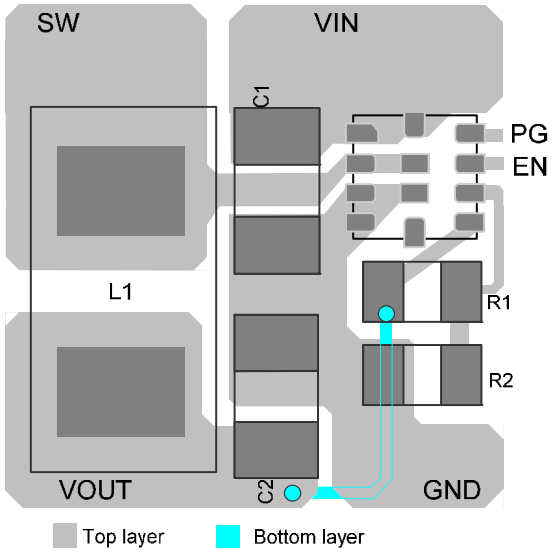


Figure 5—Recommended PCB layout: Connect two ends of the input decoupling capacitor close to pin 1 and pin 3

Design Example

Table 2 shows a design example when ceramic capacitors are applied.

Table 2—Design example

V_{IN}	5 V
V_{OUT}	1.2 V
I_{OUT}	4 A

The detailed application schematic is shown in Figure 6. The typical performance and waveforms have been shown in the “Typical Characteristics” section. For additional device applications, please refer to the related evaluation board datasheet.

TYPICAL APPLICATION CIRCUITS

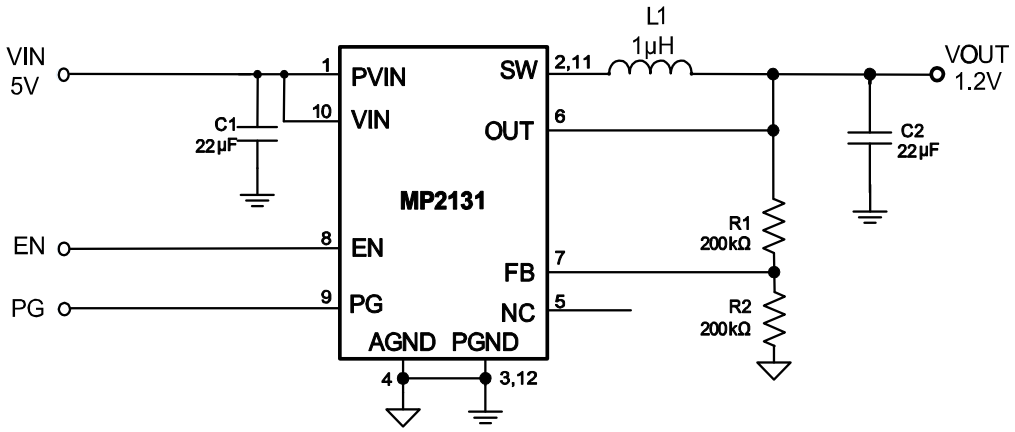


Figure 6—$5V_{IN}$, 1.2 V/4 A

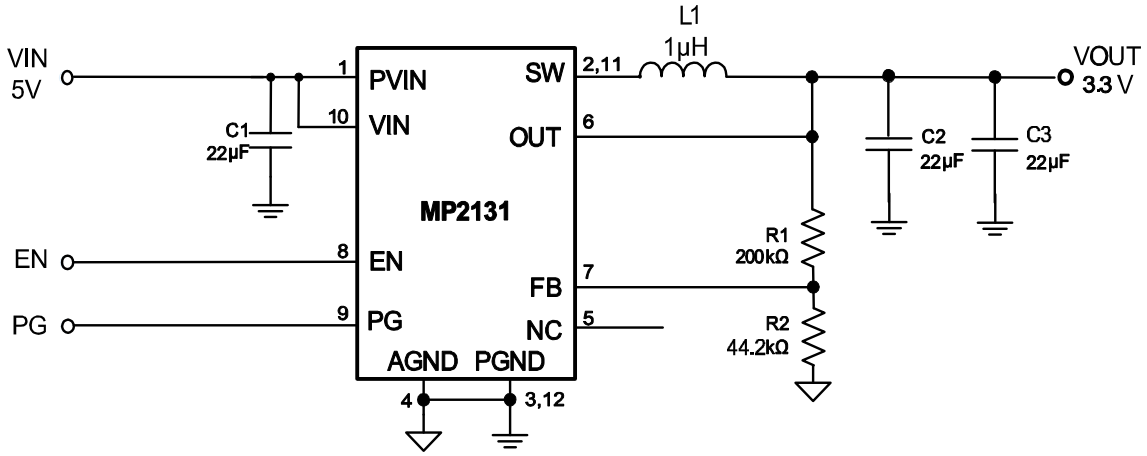
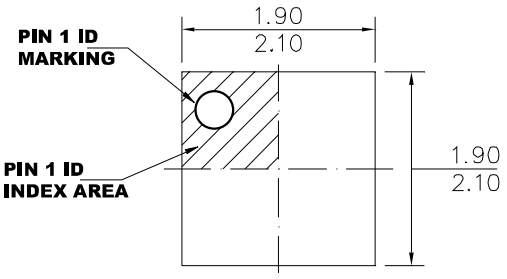


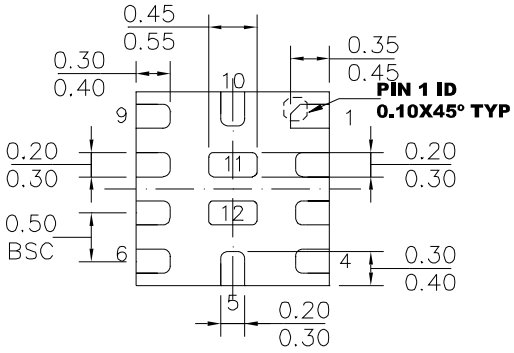
Figure 7—$5V_{IN}$, 3.3 V/4 A

PACKAGE INFORMATION

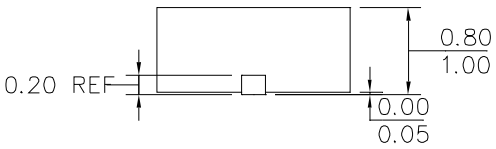
QFN-12 (2mm x 2mm)



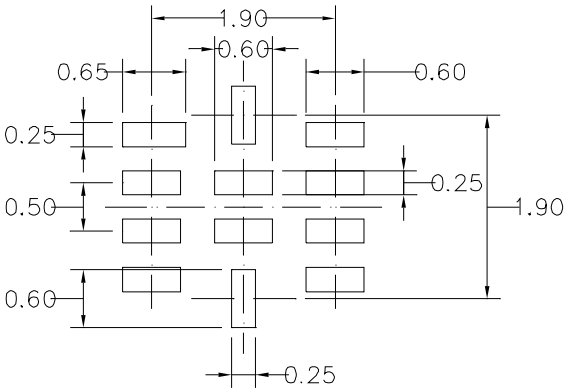
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.1	5/8/2021	Update the last page for the POD due to POD0092 has been updated from r3.0 to r4.0 per package dept.	P16