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NTE5470 thru 5476
Silicon Controlled Rectifier (SCR)
5 Amp, TO64

Description:

The NTE5470 through NTE5476 are multi−purpose PNPN silicon controlled rectifiers in a TO64 type stud mount package suitable for industrial and consumer applications.

Features:

- Uniform Low−Level Noise−Immune Gate Triggering
- Low Forward “ON” Voltage
- High Surge−Current Capability

Absolute Maximum Ratings: (Apply over operating temperature range unless otherwise specified)

Peak Repetitive Forward and Reverse Blocking Voltage (Note 1), V_{DRM}, V_{RRM}
- NTE5470 . . . . . 50V
- NTE5471 . . . . . 100V
- NTE5472 . . . . . 200V
- NTE5473 . . . . . 300V
- NTE5474 . . . . . 400V
- NTE5475 . . . . . 500V
- NTE5476 . . . . . 600V

Forward Current RMS, I_TRMS 8A
Peak Forward Surge Current (One Cycle, 60Hz, T_J = −40° to +100°C), I_{TSM} 100A
Circuit Fusing (T_J = −40° to +100°C, t ≤ 8.3ms), I^2t . . . . . $40A^2$sec
Peak Gate Power, P_{GM} 5W
Average Gate Power, $P_{G(AV)}$ 0.5W
Peak Gate Current, I_{GM} 2A
Peak Gate Voltage (Note 2), V_{GM} 10V
Operating Temperature Range, T_J . . . . . −40° to +100°C
Storage Temperature Range, T_{stg} . . . . . −40° to +150°C
Thermal Resistance, Junction−to−Case, R_{thJC} . . . . . 2.5°C/W
Stud Torque . . . . . 15 in. lb.

Note 1. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage applied exceeds the rated blocking voltage.

Note 2. Devices should not be operated with a positive bias applied to the gate concurrently with a negative potential applied to the anode.

Electrical Characteristics: (T_C = +25°C unles otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current	I_{DRM}, I_{RRM}	Rated V_{DRM} or V_{RRM}, Gate Open	T_J = +25°C	–	–	10	μA
			T_J = +100°C	–	–	2	mA
Gate Trigger Current, Continuous DC	I_{GT}	V_D = 7V, R_L = 100Ω, Note 3		–	10	30	mA
			T_C = −40°C	–	–	60	mA
Gate Trigger Voltage, Continuous DC	V_{GT}	V_D = 7V, R_L = 100Ω		–	0.75	1.5	V
			T_C = −40°C	–	–	2.5	V
			T_J = +100°C	0.2	–	–	V
Forward “ON” Voltage	v_{TM}	I_{TM} = 15.7A, Note 4		–	1.4	2.0	V
Holding Current	I_H	V_D = 7V, Gate Open		–	10	30	mA
			T_C = −40°C	–	–	60	mA
Turn−On Time (t_d + t_r)	t_{on}	I_G = 20mA, I_F = 5A, V_D = Rated V_{DRM}		–	1	–	μs
Turn−Off Time	t_{off}	I_F = 5A, I_R = 5A, V_D = Rated V_{DRM}, dv/dt = 30V/μs		–	15	–	μs
			T_J = +100°C	–	25	–	μs
Forward Voltage Application Rate (Exponential)	dv/dt	Gate Open, T_J = +100°C, V_D = Rated V_{DRM}		–	50	–	V/μs

Note 3. For optimum operation, i.e. faster turn−on, lower switching losses, best di/dt capability, recommended I_{GT} = 200mA minimum.

Note 4. Pulsed, 1ms Max, Duty Cycle ≤ 1%.