REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Drawing updated to reflect current requirements. - lgt	01-07-13	Raymond Monnin

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV	A	A	A	A	A	A	A	A												
SHEET	15	16	17	18	19	20	21	22												

REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
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DRAWING APPROVAL DATE
06 May 1991

MICROCIRCUIT, LINEAR, 8-BIT ANALOG I/O SYSTEM, MONOLITHIC SILICON

REVISION LEVEL	SIZE	CAGE CODE	
A	A	**67268**	**5962-89629**

SHEET 1 OF 22

DSCC FORM 2233
APR 97

5962-E488-01

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-89629	01	L	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Relative Accuracy
01	AD7569S	8-bit analog I/O system	±1 LSB for DAC and ADC
02	AD7569T	8-bit analog I/O system	±1/2 LSB for DAC and ADC

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line
3	CQCC1-N28	28	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage (V_{DD}) to $AGND_{DAC}$ or $AGND_{ADC}$ ..... -0.3 V dc to +7.0 V dc
Supply voltage (V_{DD}) to DGND ..... -0.3 V dc to +7.0 V dc
V_{DD} to V_{SS} ..... -0.3 V dc to +14 V dc
$AGND_{DAC}$ or $AGND_{ADC}$ to DGND ..... -0.3 V dc to V_{DD} +0.3 V dc
$AGND_{DAC}$ or $AGND_{ADC}$ ..... ±5.0 V dc
Logic voltage to DGND ..... -0.3 V dc to V_{DD} +0.3 V dc
CLK input voltage to DGND ..... -0.3 V dc to V_{DD} +0.3 V dc
Output voltage to $AGND_{DAC}$ 1/ ..... V_{SS} -0.3 V dc to V_{DD} +0.3 V dc
Input voltage to $AGND_{ADC}$ ..... V_{SS} -0.3 V dc to V_{DD} +0.3 V dc
Storage temperature range ..... -65°C to +150°C
Lead temperature (soldering, 10 seconds) ..... +300°C
Power dissipation (P_D) ..... 450 mW 2/
Thermal resistance, junction to case (θ_{JC}) ..... See MIL-STD-1835
Thermal resistance, junction to ambient (θ_{JA}) ..... 120°C/W
Junction temperature (T_J) ..... +150°C

1.4 Recommended operating conditions.

Supply voltage to ground (V_{SS}) ..... -4.75 V dc to –5.25 V dc
Supply voltage to ground (V_{DD}) ..... +4.75 V dc to +5.25 V dc
Ambient operating temperature range (T_A) ..... -55°C to +125°C

1/ Output may be shorted to any voltage in the range V_{SS} to V_{DD} provided that the power dissipation of the package is not exceeded.
2/ Derate above T_A = +75°C at 6.0 mW/°C.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 -- Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 -- List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Pin descriptions. The pin descriptions shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Input/output voltage ranges and unipolar/bipolar code tables. The input/output voltage ranges and unipolar/bipolar code tables shall be as specified on figure 4.

3.2.5 Logic diagram. The logic diagram shall be as specified on figure 5.

3.2.6 Load circuits. The load circuits shall be as specified on figure 6.

3.2.7 Write cycle timing waveforms. The write cycle timing waveforms shall be as specified on figure 7.

3.2.8 ADC mode 1 interface timing waveforms. The ADC mode 1 interface timing waveforms shall be as specified on figure 8.

3.2.9 ADC mode 2 interface timing waveforms. The ADC mode 2 interface timing waveforms shall be as specified on figure 9.

3.2.10 Equivalent input voltage circuit. The equivalent input voltage circuit shall be as specified on figure 10.

3.2.11 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ C_L = 100 pF to $AGND_{DAC}$ R_L = 2.0 kΩ -55°C ≤ T_A ≤+125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DAC specifications							
Relative accuracy	INL		01	1, 2, 3		±1.0	LSB
			02	1		±1.0	
				2, 3, 12		±1/2	
Differential nonlinearity	DNL	Guaranteed monotonic	01	1, 2, 3		±1.0	LSB
			02	1		±1.0	
				2, 3, 12		±3/4	
Unipolar offset error		DAC data is all zeros, V_{SS} = 0 V	ALL	1		±2.0	LSB
			01	2, 3		±2.5	
			02	2, 3		±2.0	
				1, 12		±1.5	
Bipolar zero offset error		DAC data is all zeros, V_{SS} = -5.0 V	ALL	1		±2.0	LSB
			01	2, 3		±2.5	
			02	2, 3		±2.0	
				1, 12		±1.5	
Full-scale error		V_{DD} = 5.0 V 2/	ALL	1		±2.0	LSB
			01	2, 3		±4.0	
			02	2, 3		±3.0	
				12		±1.0	
$\frac{\Delta \text{Full scale}}{\Delta V_{DD}}$		T_A = +25°C, V_{OUT} = 2.5 V, Δ V_{DD} = ±5%	ALL	1		0.5	LSB
$\frac{\Delta \text{Full scale}}{\Delta V_{SS}}$		T_A = +25°C, V_{OUT} = -2.5 V, Δ V_{SS} = ±5%	ALL	1		0.5	LSB
Digital input voltage low level	V_{IL}		ALL	1, 2, 3		0.8	V
Digital input voltage high level	V_{IH}		ALL	1, 2, 3	2.4		V
Input leakage current	I_{IL}	V_{IN} = 0 to V_{DD}	ALL	1, 2, 3		10	µA
Positive power supply current	I_{DD}	V_{OUT} = V_{IN} = 2.5 V, Logic units = 2.4 V, CLK = 0.8 V, output unloaded	ALL	1, 2, 3		13	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ C_L = 100 pF to $AGND_{DAC}$ R_L = 2.0 kΩ -55°C ≤ T_A ≤+125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DAC specifications - Continued							
Negative power supply current (dual supply)	I_{SS}	V_{OUT} = V_{IN} = -2.5 V, Logic units = 2.4 V, CLK = 0.8 V, output unloaded	ALL	1, 2, 3		4.0	mA
Input capacitance	C_{IN}	See 4.3.1d	ALL	4		10	pF
Signal-to-noise ratio	SNR	V_{OUT} = 20 kHz full scale sine wave with $f_{SAMPLING}$ = 400 kHz	01	4, 5, 6	44		dB
			02		46		
Total harmonic distortion	THD	V_{OUT} = 20 kHz full scale sine wave with $f_{SAMPLING}$ = 400 kHz	ALL	4, 5, 6		48	dB
Functional test		See 4.3.1b	ALL	7, 8			
$\overline{WR}$ pulse width	t_1	See figure 7 3/	ALL	9	80		ns
				10, 11	90		
$\overline{CS}$, $\overline{A}/B$ to $\overline{WR}$ setup time	t_2		ALL	9, 10, 11	0		
$\overline{CS}$, $\overline{A}/B$ to $\overline{WR}$ hold time	t_3		ALL	9, 10, 11	0		
Data valid to $\overline{WR}$ setup time	t_4		ALL	9	60		
				10, 11	80		
Data valid to $\overline{WR}$ hold time	t_5		ALL	9, 10, 11	10		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ f_{CLK} = 5.0 MHz -55°C ≤ T_A ≤+125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
ADC specifications							
Relative accuracy	INL		01	1, 2, 3		±1	LSB
			02	2, 3, 12		±1/2	
				1		±1	
Differential nonlinearity	DNL	No missing codes	01	1, 2, 3		±1	LSB
			02	2, 3, 12		±3/4	
				1		±1	
Unipolar offset error		V_{SS} = 0 V	ALL	1		±2.0	LSB
			01	2, 3		±3.0	
			02	2, 3		±2.5	
				1, 12		±1.5	
Bipolar zero offset error		V_{SS} = -5.0 V ±1.25 V range	ALL	1		±3.0	LSB
			01	2, 3		±4.0	
			02	2, 3		±3.5	
				12		±2.5	
Full scale error		V_{DD} = 5.0 V 2/	ALL	1	-4.0	0	LSB
				2, 3	-7.5	2.0	
$\frac{\Delta \text{Full scale}}{\Delta V_{DD}}$		V_{IN} = 2.5 V, ΔV_{DD} = ±5%	ALL	1		0.5	LSB
$\frac{\Delta \text{Full scale}}{\Delta V_{SS}}$		V_{IN} = -2.5 V, ΔV_{SS} = ±5%	ALL	1		0.5	LSB
Input voltage low level	V_{IL}		ALL	1, 2, 3		0.8	V
Input voltage high level	V_{IH}		ALL	1, 2, 3	2.4		V
Analog input current	I_{IN}	See figure 10	ALL	1, 2, 3		±300	µA
Input leakage current	I_{IL}	$\overline{CS}$, $\overline{RD}$, $\overline{ST}$, Range, $\overline{RESET}$	ALL	1, 2, 3		10	µA
CLK input current low level	I_{INL}	V_{IN} = 0 V	ALL	1, 2, 3		-1.6	mA
CLK input current high level	I_{INH}	V_{IN} = V_{DD}	ALL	1, 2, 3		40	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ f_{CLK} = 5.0 MHz -55°C ≤ T_A ≤+125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
ADC specifications - Continued							
Output voltage low level	V_{OL}	I_{SINK} = 1.6 mA	ALL	1, 2, 3		0.4	V
Output voltage high level	V_{OH}	I_{SOURCE} = 200 µA	ALL	1, 2, 3	4.0		V
Floating state leakage current	I_{OUT}		ALL	1, 2, 3		±10	µA
Positive power supply current	I_{DD}	V_{OUT} = V_{IN} = 2.5 V, Logic units = 2.4 V, CLK = 0.8 V, output unloaded	ALL	1, 2, 3		13	mA
Negative power supply current (dual supplies)	I_{SS}	V_{OUT} = V_{IN} = -2.5 V, Logic units = 2.4 V, CLK = 0.8 V, output unloaded	ALL	1, 2, 3		4.0	mA
Input capacitance	C_{IN}	See 4.3.1d	ALL	4		10	pF
Floating state output capacitance	C_{OUT}	See 4.3.1d	ALL	4		10	pF
Signal-to-noise ratio	SNR	V_{IN} = 100 kHz full scale sine wave with $f_{SAMPLING}$ = 400 kHz 4/	01	4, 5, 6	44		dB
			02		45		
Total harmonic distortion	THD	V_{IN} = 100 kHz full scale sine wave with $f_{SAMPLING}$ = 400 kHz 4/	ALL	4, 5, 6		48	dB
Conversion time with external clock		f_{CLK} = 5.0 MHz	ALL	9, 10, 11		2.0	µs
Conversion time with internal clock			ALL	9, 10, 11	1.6	2.6	µs
Functional test		See 4.3.1b	ALL	7, 8			
$\overline{ST}$ pulse width	t_6	See figure 8 3/	ALL	9, 10, 11	50		ns
$\overline{ST}$ to $\overline{BUSY}$ delay	t_7		ALL	9		110	
				10, 11		150	
$\overline{BUSY}$ to $\overline{INT}$ delay	t_8		ALL	9		20	
				10, 11		30	
$\overline{BUSY}$ to $\overline{CS}$ delay	t_9		ALL	9, 10, 11	0		
$\overline{CS}$ to $\overline{RD}$ setup time	t_{10}		ALL	9, 10, 11	0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ C_L = 100 pF to $AGND_{DAC}$ R_L = 2.0 kΩ -55°C ≤ T_A ≤+125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
ADC specifications - Continued							
$\overline{RD}$ pulse width determined by t_{13}	t_{11}	See figure 8 3/ 5/	ALL	9	60		ns
				10, 11	90		
$\overline{CS}$ to $\overline{RD}$ hold time	t_{12}		ALL	9, 10, 11	0		
Data access time after $\overline{RD}$	t_{13}	See figure 8 3/ 6/ C_L = 20 pF	ALL	9	60		
				10, 11	90		
Data access time after $\overline{RD}$		See figure 8 3/ 6/ C_L = 100 pF	ALL	9	95		
				10, 11	135		
Bus relinquish time after $\overline{RD}$ 5/ 7	t_{14}	See figure 8 3/ 7/	ALL	9	10	60	
				10, 11	10	85	
$\overline{RD}$ to $\overline{INT}$ delay	t_{15}	See figure 8 3/	ALL	9		65	
				10, 11		85	
$\overline{RD}$ to $\overline{BUSY}$ delay	t_{16}		ALL	9		120	
				10, 11		160	
Data valid after $\overline{BUSY}$	t_{17}	See figure 9 3/ 6/ C_L = 20 pF	ALL	9		60	ns
				10, 11		90	
		See figure 9 3/ 6/ C_L = 100 pF	ALL	9		90	
				10, 11		135	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

1/ Unless otherwise specified, V_{DD} = 5.0 ±5%, V_{SS} = RANGE = $AGND_{ADC}$ = DGND = 0 V; specifications apply for all output ranges including bipolar ranges with dual supply operation.

2/ Includes internal voltage reference error and is calculated after offset error has been adjusted out.

For DAC specifications :
a) Ideal unipolar full scale voltage is (FS – 1 LSB).
b) Ideal bipolar positive full scale voltage is (FS/2 – 1 LSB).
c) Ideal unipolar negative full scale voltage is (-FS/2).

For DAC specifications :
a) Ideal unipolar last code transition occurs at (FS – 3/2 LSB).
b) Ideal bipolar last code transition occurs at (FS/2 – 3/2 LSB).

3/ All input control signals are specified with $t_R = t_F$ = 5.0 ns (10% to 90% of +5.0 V) and timed from a voltage level of 1.6 V. ADC is sample tested in mode 1 only.

4/ Exact frequencies are 101 kHz and 384 kHz to avoid harmonics coinciding with sampling frequency.

5/ Tested initially and after process and design changes only.

6/ t_{13} and t_{17} are measured with the load circuits on figure 6 and defined as the time required for an output to cross either 0.8 V or 2.4 V.

7/ t_{14} is defined as the time required for the data line to change 0.5 V when loaded with circuit on figure 6.

Device type	01 and 02	01
Case outline	L	3
Terminal Number	Terminal symbol	
1	$AGND_{DAC}$	NC
2	V_{OUT}	$AGND_{DAC}$
3	V_{SS}	V_{OUT}
4	RANGE	V_{SS}
5	$\overline{RESET}$	RANGE
6	DB7	$\overline{RESET}$
7	DB6	DB7
8	DB5	NC
9	DB4	DB6
10	DB3	DB5
11	DB2	DB4
12	DGND	DB3
13	DB1	DB2
14	DB0	DGND
15	$\overline{WR}$	NC
16	$\overline{CS}$	DB1
17	$\overline{RD}$	DB0
18	$\overline{ST}$	$\overline{WR}$
19	$\overline{BUSY}$	$\overline{CS}$
20	$\overline{INT}$	$\overline{RD}$
21	CLK	$\overline{ST}$
22	$AGND_{ADC}$	NC
23	V_{IN}	$\overline{BUSY}$
24	V_{DD}	$\overline{INT}$
25	-----	CLK
26	-----	$AGND_{ADC}$
27	-----	V_{IN}
28	-----	V_{DD}

NC = No connection

FIGURE 1. Terminal connections.

Pin	Description
$AGND_{DAC}$	Analog ground for the DAC(s). Separate ground return paths are provided for the DAC(s) and ADC to minimize crosstalk.
V_{OUT}	Output voltage. V_{OUT} is the buffered output voltage from the device DAC. Four different output voltage ranges can be achieved (see input/output ranges table shown on figure 4).
V_{SS}	Negative supply voltage (-5.0 V for the dual supply or 0 V for the single supply). This pin is also used with the RANGE pin to select the different input/output ranges and changes the data format from binary (V_{SS} = 0 V) to 2s complement (V_{SS} = -5.0 V) (see input/output ranges table shown on figure 4).
RANGE	Range selection input. This is used with the V_{SS} input to select the different ranges as per input/output ranges table shown on figure 4. The range selected applies to both the analog input voltage of the ADC and the output voltage from the DAC(s).
$\overline{RESET}$	Reset input (active low). This is an asynchronous system reset which clears the DAC register(s) to all zeros and clears the $\overline{INT}$ line of the ADC (i.e., makes the ADC ready for new conversion). In unipolar operation this input sets the output voltage to 0 V; in bipolar operation it sets the output to negative full scale.
DB7	Data bit 7. Most significant bit (MSB).
DB6 – DB2	Data bit 6 to data bit 2.
DGND	Digital ground.
DB1	Data bit 1.
DB0	Data bit 0. Least significant bit.
$\overline{WR}$	Write input (edge triggered). This is used in conjunction with $\overline{CS}$ to write data into the device DAC register. It is used in conduction with $\overline{CS}$ and A/B to write data into the selected DAC register of the device. Data is transferred on the rising edge of $\overline{WR}$.
$\overline{CS}$	Chip select input (active low). The device is selected when this input is active.
$\overline{RD}$	Read input (active low). This input must be active to access data from the part. In the mode 2 interface, $\overline{RD}$ going low starts conversion. It is used in conjunction with the $\overline{CS}$ input.

FIGURE 2. Pin descriptions.

Pin	Description
$\overline{ST}$	Start conversion (edge triggered). This is used when precise sampling is required. The falling edge of $\overline{ST}$ starts conversion and drives $\overline{BUSY}$ low. The $\overline{ST}$ signal is not gated with $\overline{CS}$.
$\overline{BUSY}$	BUSY status output (active low). When this pin is active the ADC is performing a conversion. The input signal is held prior to the falling edge of $\overline{BUSY}$.
$\overline{INT}$	Interrupt output (active low). $\overline{INT}$ going low indicates that the conversion is complete. $\overline{INT}$ goes high on the rising edge of $\overline{CS}$ or $\overline{RD}$ and is also set high by a low pulse on $\overline{RESET}$.
CLK	A TTL compatible clock signal may be used to determine the ADC conversion time. Internal clock operation is achieved by connecting a resistor and capacitor to ground.
$AGND_{ADC}$	Analog ground for the ADC.
V_{IN}	Analog input. Various input ranges can be selected (see input/output ranges table shown on figure 4).
V_{DD}	Positive supply voltage (+5.0 V).

FIGURE 2. Pin descriptions – Continued.

$\overline{CS}$	$\overline{WR}$	$\overline{RESET}$	DAC FUNCTION
H	H	H	DAC register unaffected
L	L	H	DAC register unaffected
L	_|‾	H	DAC register updated
_|‾	L	H	DAC register updated
X	X	L	DAC register loaded with all zeros

L = Low H = High X = Don't care _|‾ = Low to high transition

FIGURE 3. Truth table.

Range	V_{SS}	Input/output voltage range	DB0 - DB7 Data format
0	0 V	0 to +1.25 V	Binary
1	0 V	0 to +2.5 V	Binary
0	-5.0 V	±1.25 V	2s complement
1	-5.0 V	±2.5 V	2s complement

FIGURE 4a. Input/output ranges.

DAC register contents		Analog output, V_{OUT}
MSB	LSB	
1111	1111	$+V_{REF}(255/256)$
1000	0001	$+V_{REF}(129/256)$
1000	0000	$+V_{REF}(128/256) = +V_{REF}/2$
0111	1111	$+V_{REF}(127/256)$
0000	0001	$+V_{REF}(1/256)$
0000	0000	0 V

FIGURE 4b. Unipolar (0 to +1.25 V) code table.

DAC register contents		Analog output, V_{OUT}
MSB	LSB	
0111	1111	$+V_{REF}(127/128)$
0000	0001	$+V_{REF}(1/128)$
0000	0000	0 V
1111	1111	$-V_{REF}(1/128)$
1000	0001	$-V_{REF}(127/128)$
1000	0000	$-V_{REF}(128/128) = -V_{REF}$

FIGURE 4c. Bipolar (-1.25 to +1.25 V) code table.

FIGURE 4. Input/output voltage ranges and unipolar/bipolar code tables.

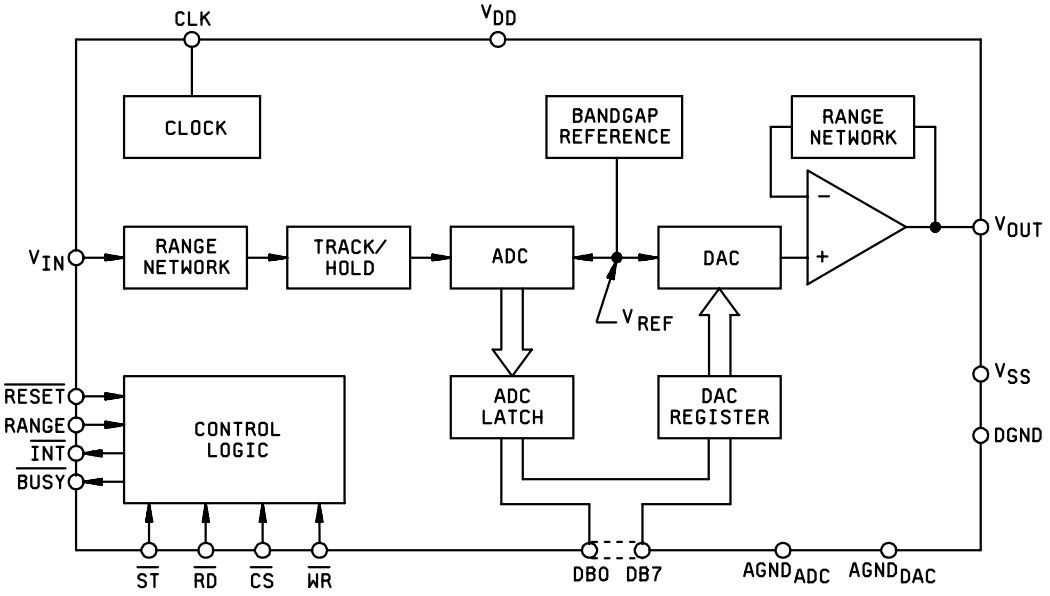
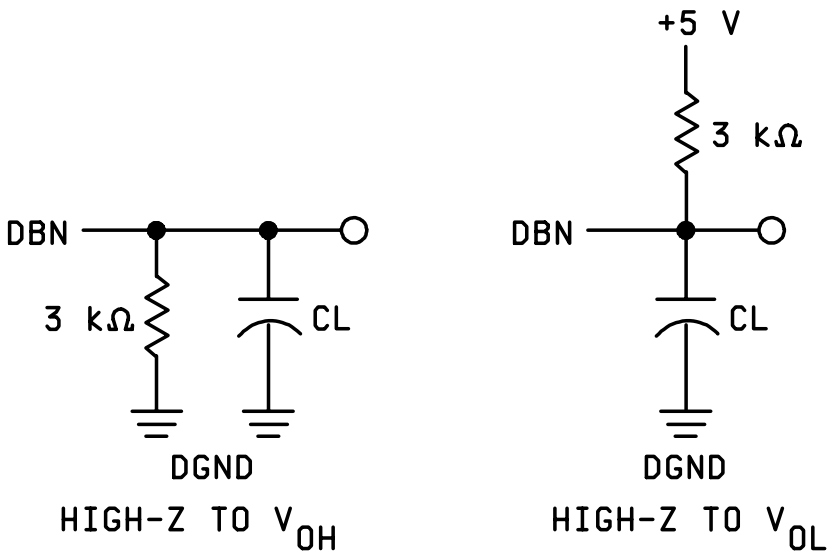
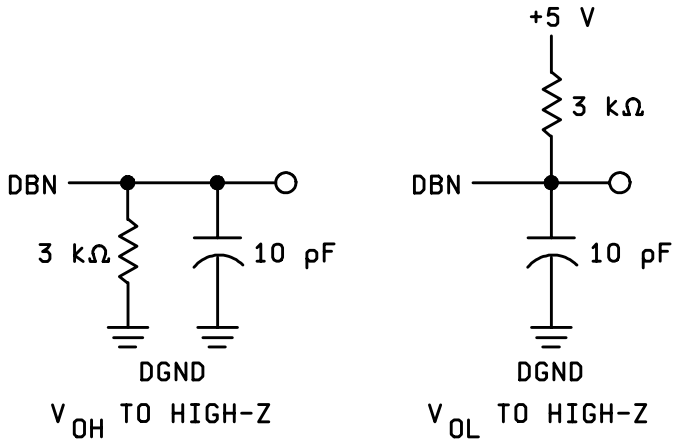


FIGURE 5. Logic diagram.

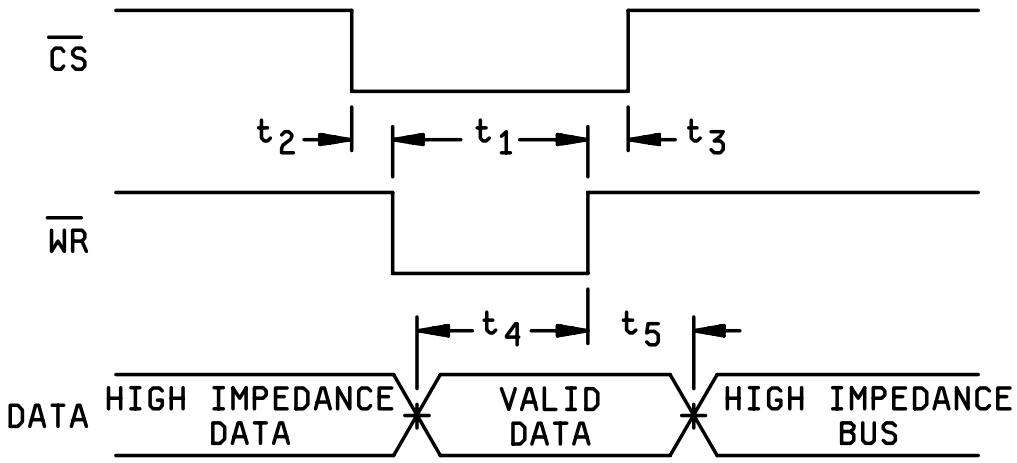


LOAD CIRCUITS FOR DATA ACCESS TIME TEST



LOAD CIRCUITS FOR DATA RELINQUISH TIME TEST

FIGURE 6. Load circuits.



NOTES:
1. All input rise and fall times measured from 10% to 90% of +5V, $t_R = t_F = 5ns$.
2. Timing measurement reference level is $\frac{V_{INH} + V_{INL}}{2}$.

FIGURE 7. Write cycle timing waveforms.

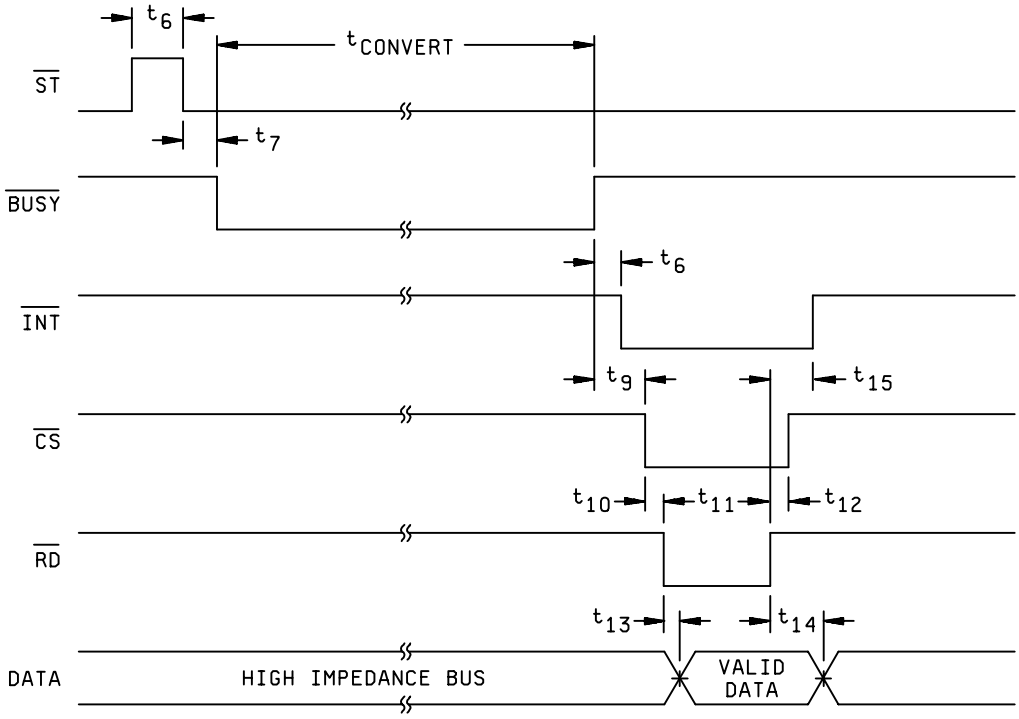


FIGURE 8. ADC mode 1 interface timing waveforms.

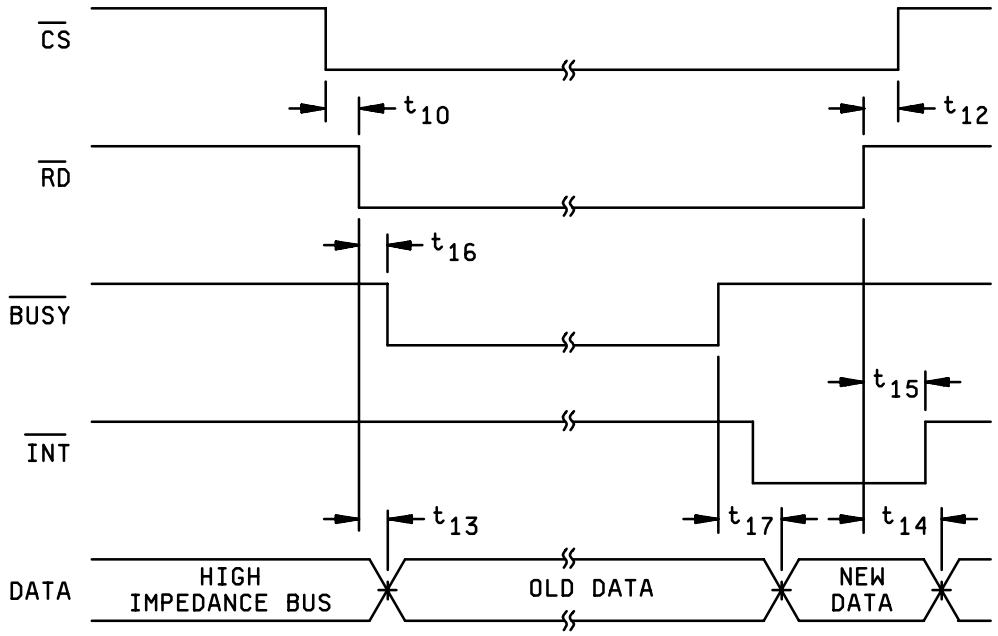
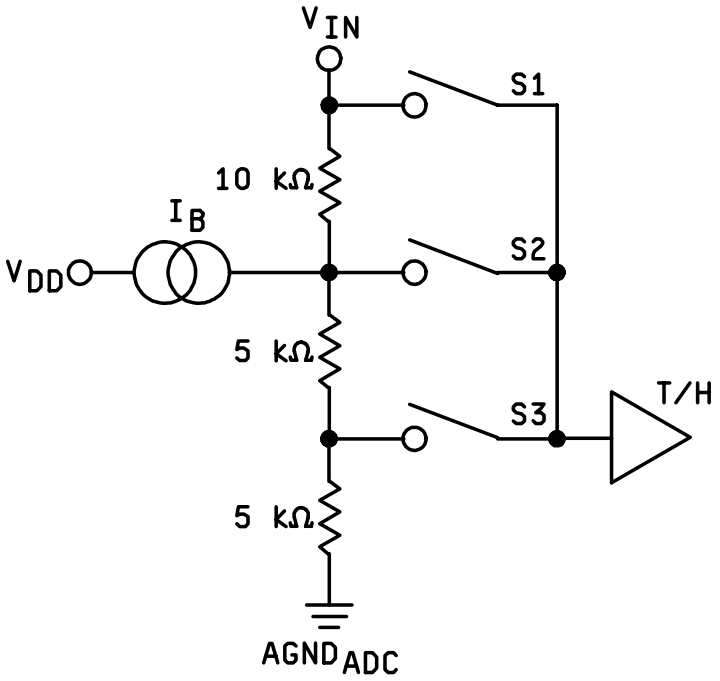


FIGURE 9. ADC mode 2 interface timing waveforms.



Voltage range	On switch	I_B
0 to +1.25 V	S1	20 μA
0 to +2.5 V	S2	20 μA
-1.25 V to +1.25 V	S2	140 μA
-2.5 V to +1.25 V	S3	280 μA

FIGURE 10. Equivalent input voltage circuit.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 4, 5, 6, 7, 8, 12
Group A test requirements (method 5005)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10**, 11**, 12
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested shall be guaranteed to the limits specified in table I herein.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7 and 8 shall include verification of the truth table.

c. Subgroup 12 is used for parts grading and selection.

d. Subgroup 4 (C_{IN}, C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 01-07-13

Approved sources of supply for SMD 5962-89629 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8962901LA	3/	AD7569SQ/883B
5962-89629013A	24355	AD7569SE/883B
5962-8962902LA	24355	AD7569TQ/883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ No longer available from an approved source of supply.

Vendor CAGE number	Vendor name and address
24355	Analog Devices, Inc. Rt. 1 Industrial Park P.O. Box 9106 Norwood, Ma. 02062 Point of Contact: Bay F-1 Raheen IND. Estate Limerick, Ireland

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.