FUJITSU SEMICONDUCTOR
DATA SHEET

DS412-00001-1v0-E

ASSP

FRAM Authentication IC

MB94R330

■ DESCRIPTION

The MB94R330 is an FRAM (Ferroelectric Random Access Memory) authentication IC using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells.

The MB94R330 adopts an original communication protocol based on the two-wire serial interface (I^2C BUS), a hardware cryptographic macro and a proprietary control core.

The MB94R330 is suitable for detecting cloned peripherals and accessories which is used in an electric equipment such as a printer, multifunction printer and so on. The Challenge and Response authentication between the host system and the peripheral enables to identify between authorized and unauthorized parts.

■ FEATURES

- Authentication algorithm : Challenge & Response
  (using pseudo random numbers generated by a hardware cryptographic macro.)
  Message Authentication Code [MAC]
  (generated by a hardware cryptographic macro and a proprietary control core)
- Life cycle : 4 types of life cycle (shipping, personalization, operation and destruction)
  Dedicated command group for life cycle
  Change of life cycle to one direction by change command
- Memory configuration : Free access area (112 bytes)
  Resource counter area (4 bytes × 8 slot)
  Protected area (8 bytes × 4 slot)
  ID area (8 bytes × 4 slot)
  One Time Write area (8 bytes × 2 slot)
  Other control information
- Interface : Two wire serial interface (I^2C BUS)
  Up to 8 slave devices are connected to one host device
  Two types of slave address definition; by external address pins, or slave address data stored in FRAM.
- Communication frequency : Maximum serial clock (SCL) frequency 400kHz
- Power supply voltage : 3.0V to 3.6V
- Operating ambient temperature : -20°C to +85°C

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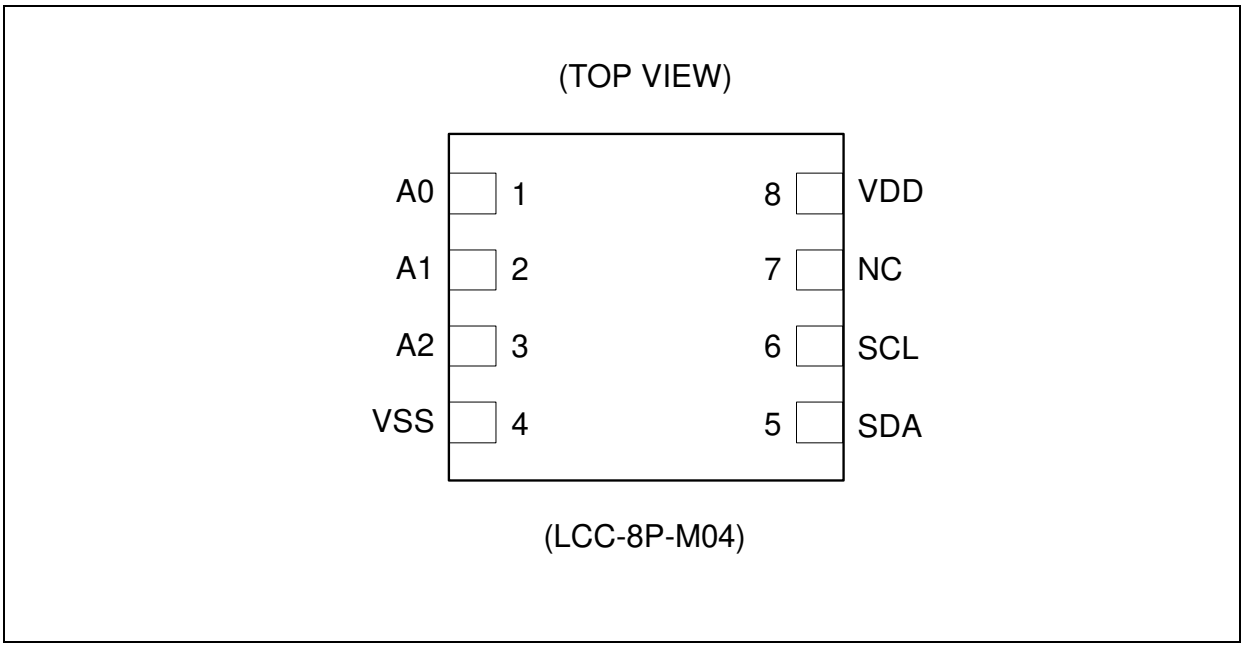
- FRAM data retention : 10 years (Operating ambient temperature=+75°C, after Rewriting/reading times=1)
- FRAM read/write endurance : 10^{12} times (Operating ambient temperature=+85°C, Total rewriting/reading times)
- Active shield : If it detects probing and physical processing to the authentication IC, it deletes the internal memory data and change to destruction phase. In destruction phase, no processing of command or response.
- Low voltage detection circuit : It monitors variation such as increase or decrease of the power supply voltage, and generates and releases a reset signal within an IC.
  Release level 2.5V (Typ@operating ambient temperature=+25°C)
  Detection level 2.35V (Typ@operating ambient temperature=+25°C)
- Package : Plastic / SON, 8-pin (LCC-8P-M04)
- Consumption power : Operating current 500µA (Typ)

■ PIN ASSIGNMENTS



■ PIN DISCRIPTIONS

Pin No.	Pin Name	Description
1 to 3	A0 to A2	Address pins The MB94R330 can be connected up to 8 devices on the same data bus. Addresses are used in order to identify each of the devices. Connect these pins to VDD or VSS externally to specify an address. When the specified address matches a slave address code inputted from the SDA pin, the device specified by the address can operate. In the open pin state, A0, A1, and A2 pins are internally pulled-down in an IC and recognized as “L”. In this case, slave address data stored in FRAM is given priority and is used to identify the device.
4	VSS	Ground pin
5	SDA	Serial Data I/O pin This is an I/O pin for performing bidirectional communication of data. It is possible to connect up to 8 devices. It is an open drain output, so a pull-up resistance is required to be connected to the external circuit.
6	SCL	Serial Clock pin This is a bidirectional I/O pin for clock of serial data I/O timing. Data is read on the rising edge of the clock and output on the falling edge. It is an open drain output, so a pull-up resistance is required to be connected to the external circuit.
7	NC	Unused pin Leave it open.
8	VDD	Power supply pin

■ HANDLING DEVICES

- Preventing latch-up

When using the device, ensure that the voltage applied does not exceed the maximum voltage rating.
In a CMOS IC, if a voltage higher than V_{DD} or a voltage lower than V_{SS} is applied to an input/output pin that is neither a medium-withstand voltage pin nor a high-withstand voltage pin, or if a voltage out of the rating range of power supply voltage mentioned in "■ELECTRICAL CHARACTERISTICS" is applied to the VDD pin or the VSS pin, a latch-up may occur.
When a latch-up occurs, power supply current increases significantly, which may cause a component to be thermally destroyed.
Be sure to apply the power supply voltage in the order of the VSS pin and the VDD pin. If the turn-on sequence is incorrect, a malfunction may occur.

- Stabilizing supply voltage

Supply voltage must be stabilized.
A malfunction may occur when power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the V_{DD} power supply voltage.
As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in V_{DD} ripple (p-p value) at the commercial frequency (50 Hz/60 Hz) falls within 10% of the standard V_{DD} value and the transient fluctuation rate becomes 0.1V/ms or less in instantaneous fluctuation for power supply switching.

- IR Reflow

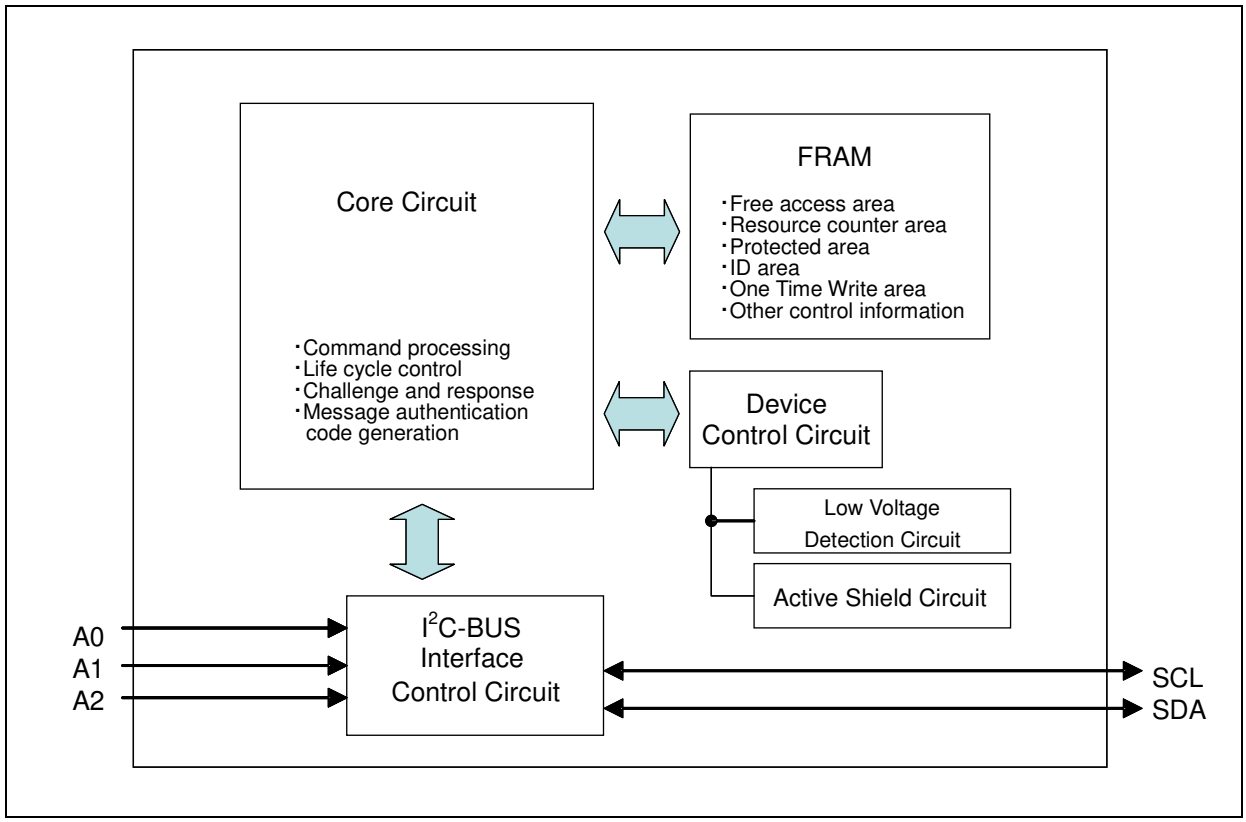
Data written in the FRAM before performing IR reflow does not guarantee the data retention after IR reflow.
Heat process during IR reflow might destroy data written in the FRAM.

■ PIN CONNECTION

- Power supply pins

Connect the current supply source with the VDD and VSS pins of this device at the lowest impedance as possible. It is also recommended that a ceramic capacitor of around 0.1 µF be connected as a bypass capacitor between the VDD and VSS pins at a location close to the device.

■ BLOCK DIAGRAM



■ MEMORY CONFIGURATION

The memory area is configured on the FRAM.

- Free Access Area

  This is the memory area of 112bytes which is freely accessible.
  It is accessible by every 1-byte.

- Protected Area

  This is the memory area which is 8 bytes × 4 slot.
  Permission to access for a memory is set by the user.
  Permission to access for a memory is managed by the control parameter for the authentication IC.

- One Time Write (OTW) Area

  This is a memory area of 8 bytes × 2 slots, where the data writing is possible only once.
  Reading is possible repeatedly within the guaranteed operating range.
  Availability of writing is managed by the control parameter for the authentication IC.

- Resource Counter Area

  This is the memory area which is 4 bytes × 8 slot.
  It is possible to increase a counter value, and impossible to decrease the value.

- ID Area

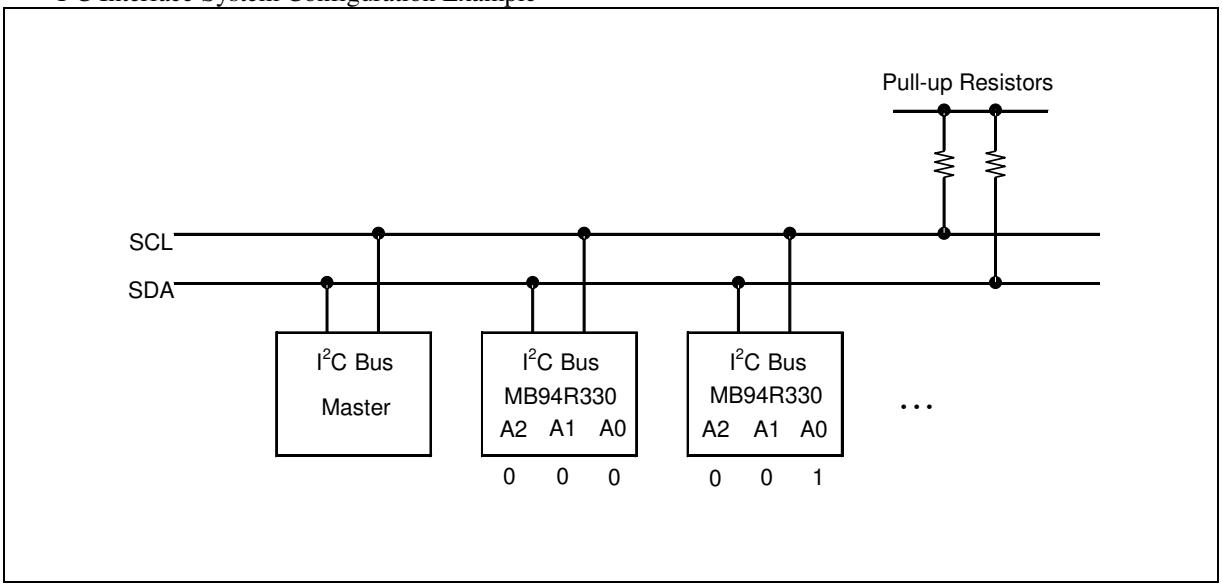
  This is the memory area which is 8 bytes × 4 slot.
  It is possible to write a user unique ID at the personalization phase.
  It is possible only to read an ID and impossible to write at the operation phase.

Memory area
Free access area (112 bytes)
Protect area (8 bytes × 4 slot)
OTW area (8 bytes × 2 slot)
Resource counter (4 bytes × 8 slot)
ID area (8 bytes × 4 slot)

■ I²C (Inter-Integrated Circuit)

The MB94R330 supports the I²C bus, and operates as a slave device. The role of the communication for the I²C bus is different from "Master" side and "Slave" side. The master side has the authority to initiate control. Furthermore, the party line can be connected which connects two or more slave devices to one master. In this case, the slave side has each unique address respectively, and after specifying the address on the slave side, the master side starts to communicate.

- I²C Interface System Configuration Example



■ I²C COMMUNICATION PROTOCOL

The SDA input should change while SCL is Low to realize communication for an I²C bus. However, as an exception, when starting (start condition) and stopping (stop condition) communication sequence, SDA is allowed to change while SCL is High.

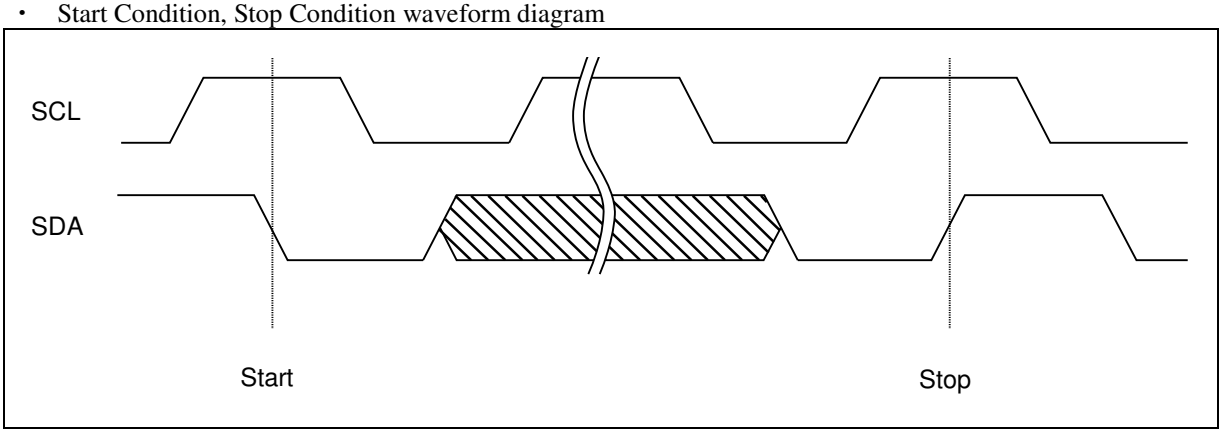
- Start Condition

To start read or write operations by the I²C bus, master side shall change the SDA input from the "H" level to the "L" level while the SCL input is in the high state.

- Stop Condition

To stop the I²C bus communication, master side shall change the SDA input from the "L" level to the "H" level while the SCL input is in the high state. In the reading operation, inputting the stop condition finishes reading and enters the standby state. In the writing operation, inputting the stop condition finishes inputting the rewrite data.

- Start Condition, Stop Condition waveform diagram



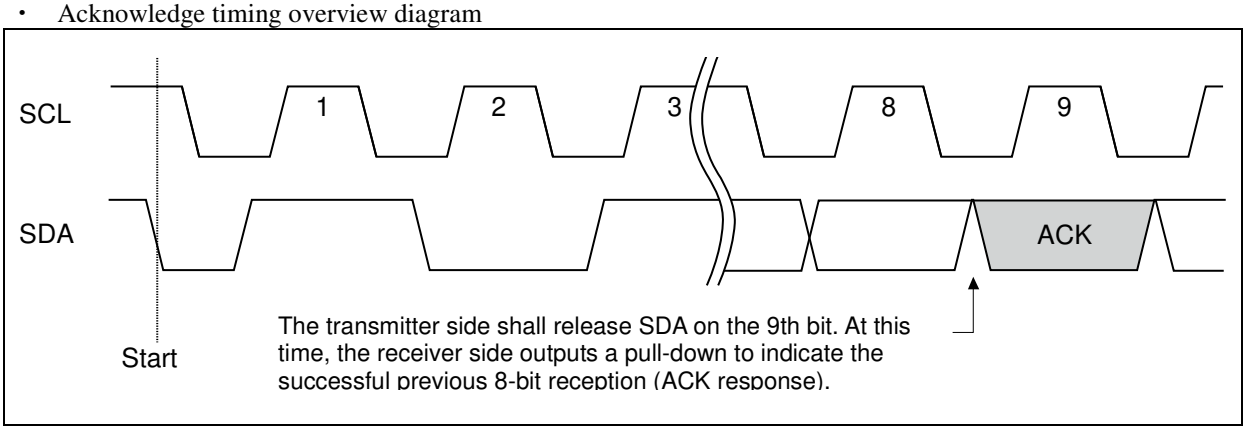
■ ACKNOWLEDGE (ACK)

In the I^2C bus, serial data including command or response data is transmitted and received in units of 8 bits. The acknowledge (ACK) signal indicates that every 8 bits of the data is successfully transmitted or received. The receiver side outputs the "L" level every time on the 9th SCL clock after every 8 bits are successfully transmitted and received. On the transmitter side, the bus is temporarily released every time on this 9th clock to allow the acknowledge signal to be received and checked. During this released period, the receiver side pulls the SDA line down to indicate that the communication is successfully received.

If the slave side receives the Stop condition before detecting the acknowledge "L" level during reading operation from the slave side, the slave side terminates the reading operation and enters the standby state.

If Stop condition is not transmitted, nor does the slave side detect the acknowledge "L" level, the slave side remains in the bus released state "H" without doing anything.

- Acknowledge timing overview diagram



■ DEVICE ADDRESS WORD (Slave address)

Following the start condition, the 8-bit device address word is inputted.
The device address word (8bits) consists of a device code (4bits), slave address code (3bits), and a read/write code (1bit).

- Device Code (4bits)

The upper 4 bits of the device address word are a device code that identifies the device type, and are fixed at "1010_B" for the MB94R330.

- Slave Address Code (3bits)

Following the device code, the 3 bits of the slave address code are input in order of A2, A1, and A0. The slave address code selects one from a maximum of 8 devices which are connected to the bus.

If external address pins A2, A1 and A0 are "000_B", the slave address information stored in the FRAM is applied preferentially.

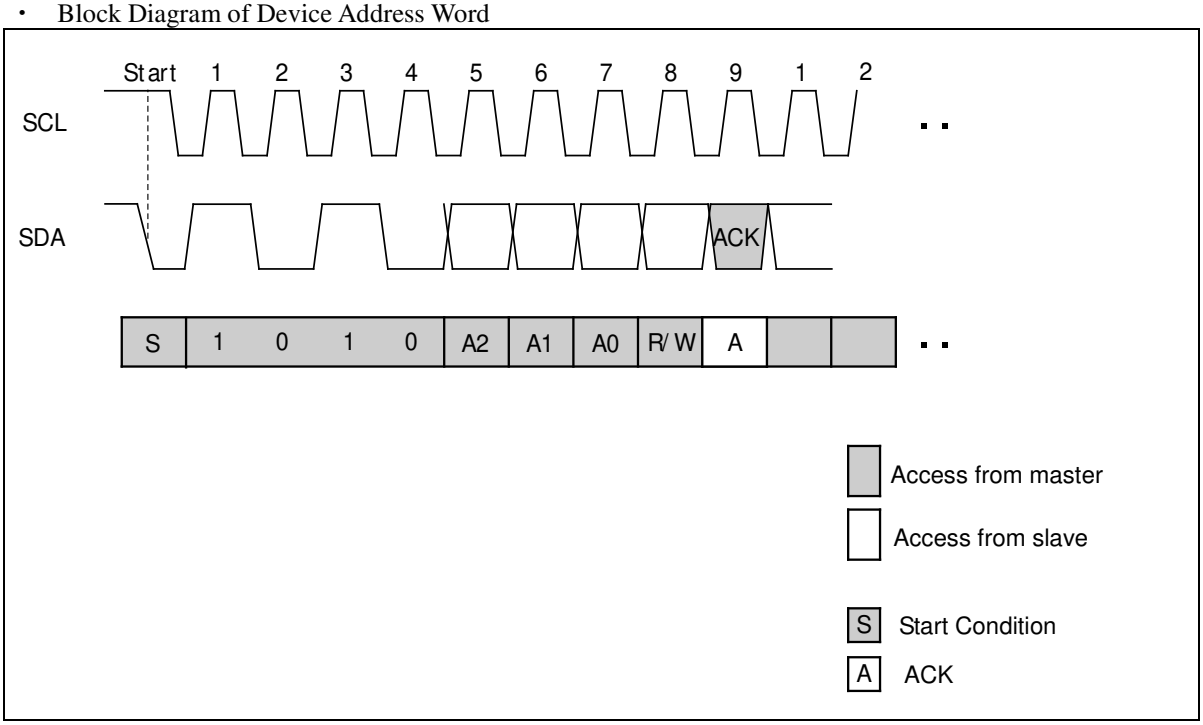
If external address pins A2, A1 and A0 are a value other than "000_B" (pull up one or more from A2, A1 and A0), the external pin state is applied preferentially as the salve address information.

The device where the slave address information matches with the inputted slave address code is selected.

- Read/Write Code (1 bit)

The 8th bit of the device address word is the R/W (read/write) code. When the R/W code is "0" input, a write operation is enabled, and the R/W code is "1" input, a read operation is enabled. Moreover, when the device code is not "1010_B" or when the slave address code does not match, the read/write operation is not enabled and the standby state is maintained.

- Block Diagram of Device Address Word



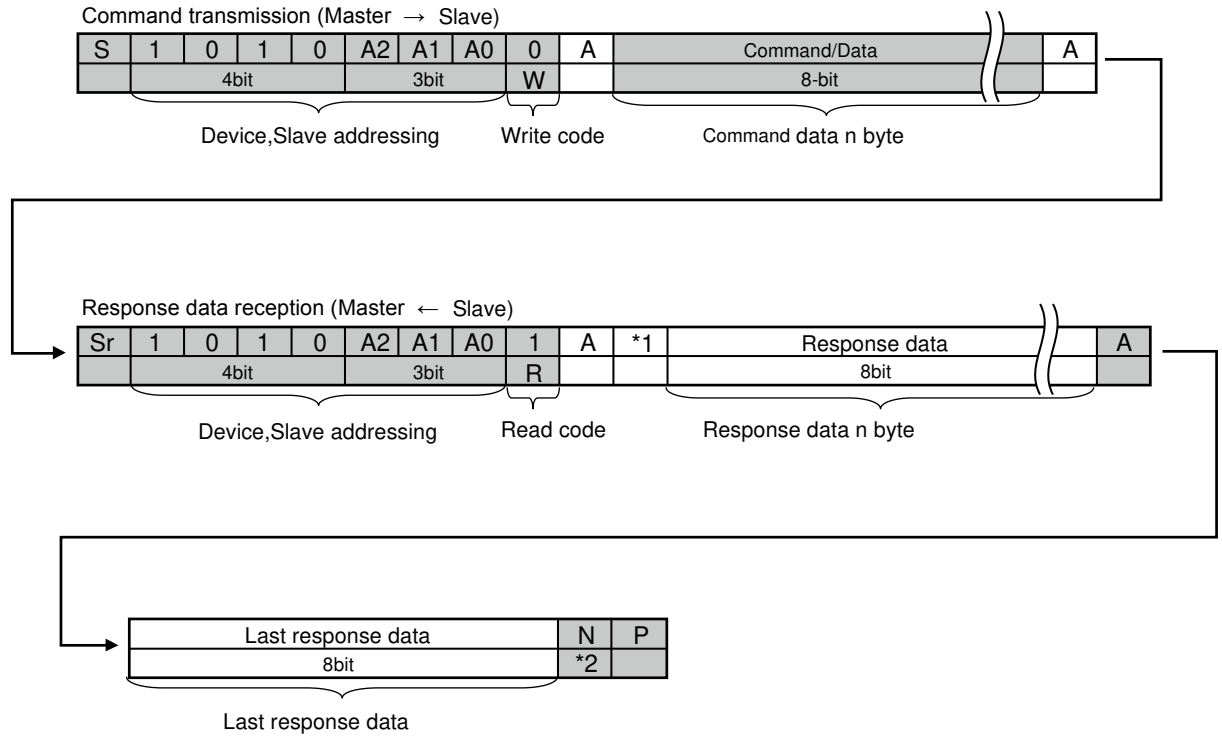
■ DATA STRUCTURE

In I^2C bus, the master side transmits the device address word (eight bits) following the start condition. The slave side replies the ACK "L" level response in the 9th bit if it receives successfully. The master side transmits each command and the argument in units of 8 bits after receiving and confirming this ACK response, and the slave side replies the ACK response every eight bits.
It is decided whether the master or the slave side drives the data line according to the R/W code of the device address word in the eighth bit. However, the master side shall drive the clock during communication.

■ DATA STRUCTURE OF PROTOCOL

Perform the response data reception from a device specified by the slave address code after transmitting each command and an argument from the master to the device. If the response data reception is executed without transmitting a command, the slave does not respond. Also, if commands are transmitted continuously, the command transmitted first becomes valid.

- Data structure diagram of protocol



: Access from master

: Access from slave

S : Start Condition
Sr : Restart Condition
P : Stop Condition
A : Acknowledge (ACK)
N : No Acknowledge (NACK)
W : Write code
R : Read code

*1: The slave fixes a clock to "L" during an internal process (clock stretch). When the internal process ends, fixed "L" in the clock is released. After that, the master receives the response data.

*2: If the error response is received for the command response where the normal response is more than 3 bytes, return ACK and transmit the stop condition because the master cannot conclude whether it is the error response beforehand.

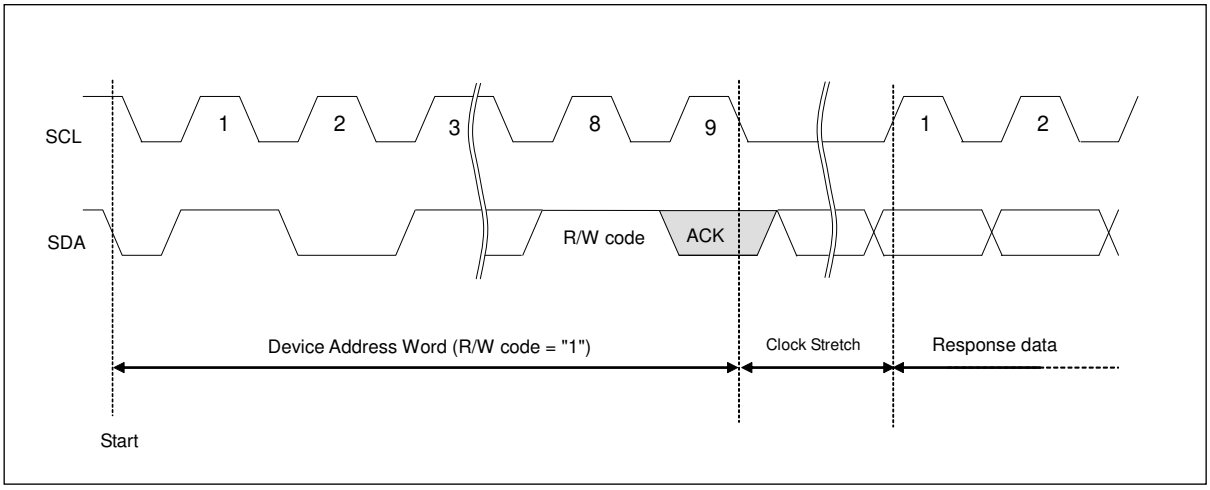
■ CLOCK STRETCH

When the master side receives a response from the slave, the slave side might have to apply WAIT to the master.

Specifically, after the slave side responds the ACK signal to the device address word (The R/W code = "1"), the slave side fixes clock signal SCL to "L" level before transmits the first bit of the response data. As a result, because the master cannot drive the clock SCL, the communication is temporarily stopped. When the slave gets ready to send the first bit of the response data, it releases the "L" level output for SCL. The master re-start the communication after the clock stretch is released.

As described above, it is called clock stretch when the slave forced to change SCL to the "L" level in order to make the master wait. The period of clock stretch depends on the processing command and conditions.

- Clock stretch diagram



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage *	V_{DD}	-0.3	+ 4.0	V
Input voltage *	V_{IN}	-0.3	V_{DD} + 0.3 (≤ 4.0)	V
Output voltage *	V_{OUT}	-0.3	V_{DD} + 0.3 (≤ 4.0)	V
Operating ambient temperature	T_A	-20	+85	°C
Storage temperature	T_{stg}	-20	+125	°C

*: These parameters are based on the condition that on VSS is 0V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage *	V_{DD}	3.0	3.3	3.6	V
"H" level input voltage *	VIH	0.8 × V_{DD}	-	V_{DD} + 0.3 (≤ 4.0)	V
"L" level input voltage *	VIL	-0.3	-	0.2 × V_{DD}	V
Operating ambient temperature	T_A	-20	-	+85	°C

*: These parameters are based on the condition that on VSS is 0V.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
Always use semiconductor devices within their recommended operating condition ranges.
Operation outside these ranges may adversely affect reliability and could result in device failure.
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min	Typ	Max	
Input leakage current	$\|I_{LI}\|$	SCL, SDA	$0.0V < V_{IN} < V_{DD}$	-	-	5	µA
Output leakage current	$\|I_{LO}\|$	SCL, SDA	$0.0V < V_{OUT} < V_{DD}$	-	-	5	µA
Operating power supply current*	I_{CC}	VDD	SCL = 400kHz	-	500	1100	µA
"L" level output voltage	V_{OL}	SCL, SDA	I_{OL} = -4.0mA	-	-	0.4	V
Input pull-down resistance	R_{PULL}	A2, A1, A0	VIN = VIL (Max)	-	80	-	kΩ
			VIN = VIH (Min)	-	6	-	MΩ

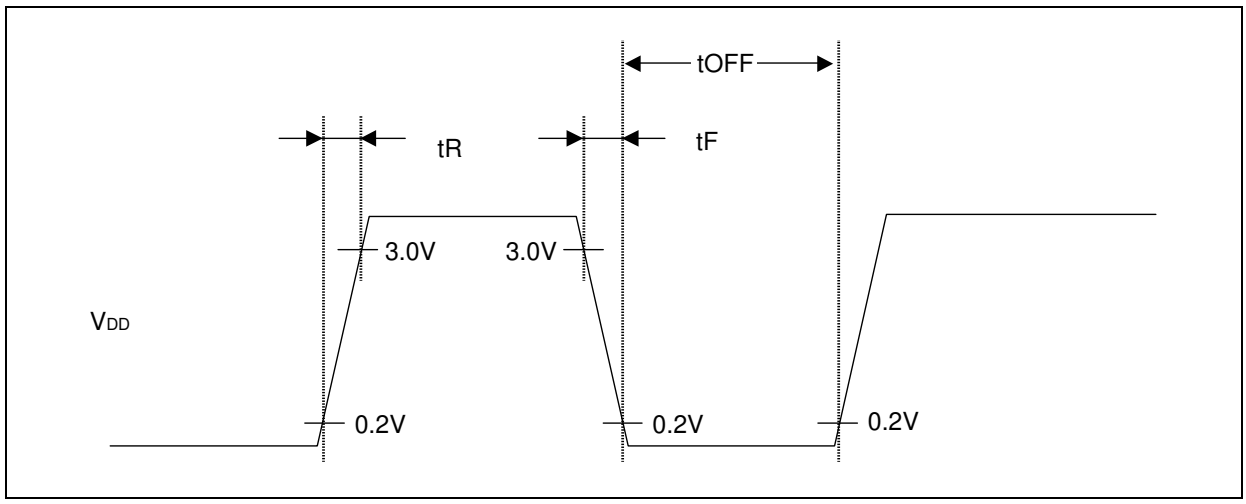
* : This is the power supply current during the command reception from the master and during the internal data process.
Furthermore, the power supply current in the command reception wait state (wait state) from the master is the same as the operating power supply current because of the continuous operating state by built-in oscillator.

(1) Power supply sequence

(within recommended operating conditions)

Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min	Typ	Max	
Power supply rise time *	tR	VDD	-	0.1	-	100	ms
Power supply fall time	tF	VDD	-	0.1	-	100	ms
Power off time	tOFF	VDD	-	1	-	-	ms

*: The slope of the power supply rise should be monotonically increasing.

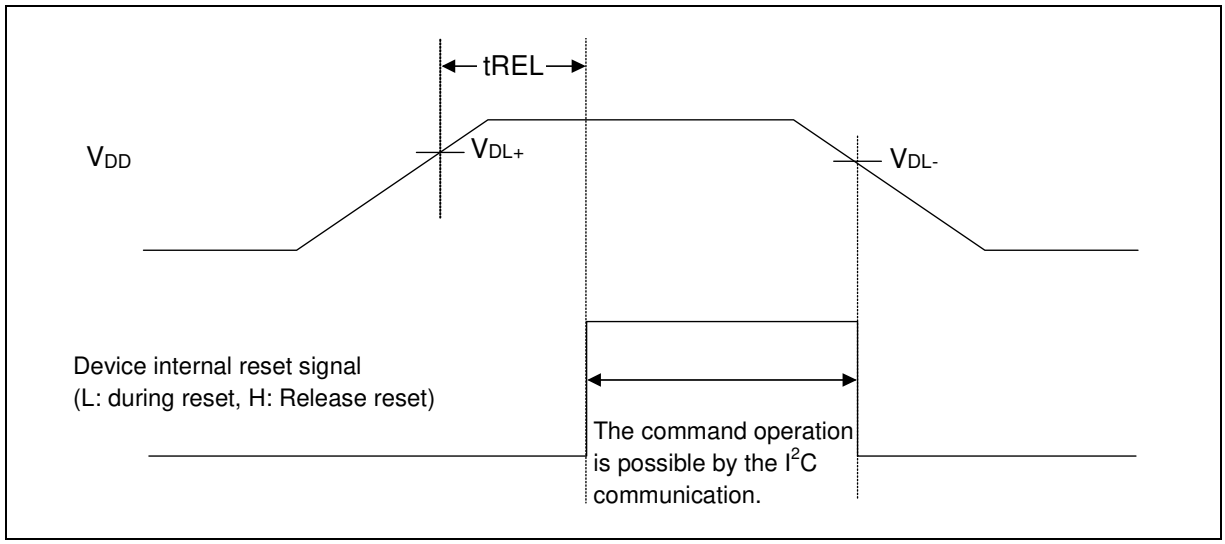


(2) Low voltage detection circuit

(within recommended operating conditions except T_A)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Release voltage	V_{DL+}	T_A = +25°C	2.0	2.5	2.65	V	Power supply voltage that the low voltage detection is released when the power supply voltage goes up.
		T_A = +85°C	1.75	2.25	2.4		
Detection voltage	V_{DL-}	T_A = +25°C	1.9	2.35	2.55	V	Power supply voltage that the device internal reset signal is generated when the power supply voltage goes down.
		T_A = +85°C	1.65	2.1	2.3		
Response time of low voltage detection	tREL	-	-	-	30	ms	Time until the device internal reset signal is released after the low voltage releases.

Note: The purpose of this low voltage detection circuit is to prevent the malfunction, misreading and miswriting FRAM at low voltage condition. It is not the purpose to guarantee the data retention time of FRAM.



2. AC Characteristics

(1) Pin capacitance

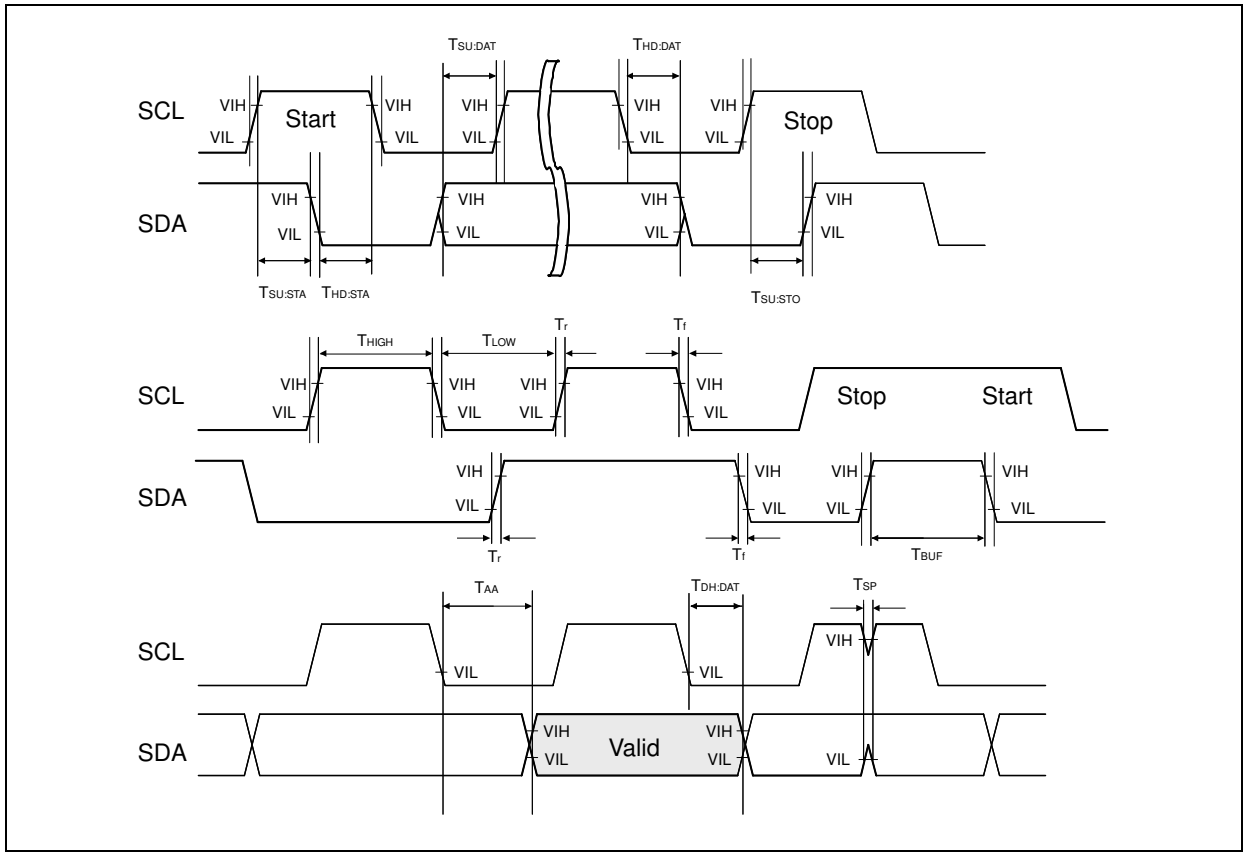
Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min	Typ	Max	
I/O capacitance	$C_{I/O}$	SCL, SDA	V_{IN} = V_{OUT} = 0V, f = 1MHz, T_A = +25°C	-	5	15	pF
Input capacitance	C_{IN}	A2,A1,A0		-	5	15	pF

(2) I^2C timing

(within recommended operating conditions)

Parameter	Symbol	Pin name	Conditions	Value				Unit
				Standard-mode		Fast-mode		
				Min	Max	Min	Max	
SCL clock frequency	FSCL	SCL	R=1kΩ, C= 100pF*	-	100	-	400	kHz
Clock High time	T_{HIGH}	SCL		4.0	-	0.6	-	µs
Clock Low time	T_{LOW}	SCL		4.7	-	1.3	-	µs
SCL/SDA rise time	T_r	SCL, SDA		-	1000	-	300	ns
SCL/SDA fall time	T_f	SCL, SDA		-	300	-	300	ns
"START condition" hold time	$T_{HD:STA}$	SCL, SDA		4.0	-	0.6	-	µs
"START condition" setup time	$T_{SU:STA}$	SCL, SDA		4.7	-	0.6	-	µs
SDA input hold	$T_{HD:DAT}$	SCL, SDA		0	-	0	-	ns
SDA input setup	$T_{SU:DAT}$	SCL, SDA		250	-	100	-	ns
SDA output hold	$T_{DH:DAT}$	SCL, SDA		0	-	0	-	ns
"STOP condition" setup time	$T_{SU:STO}$	SCL, SDA		4.0	-	0.6	-	µs
SDA output access from SCL fall	T_{AA}	SCL, SDA		-	3	-	0.9	µs
Precharge time	T_{BUF}	SCL, SDA		4.7	-	1.3	-	µs
Noise suppression time	T_{SP}	SCL, SDA		-	50	-	50	ns

*: R and C represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively.



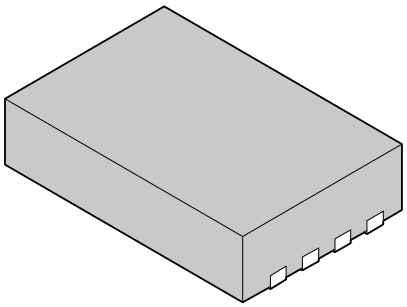
■FRAM CHARACTERISTICS

Parameter	Value		Unit	Remarks
	Min	Max		
Rewriting/reading times	10^{12}	-	cycle	Operating ambient temperature=+85°C Total rewriting/reading times
Data retention time	10	-	year	Operating ambient temperature=+75°C Data retention time after Rewriting/reading times=1

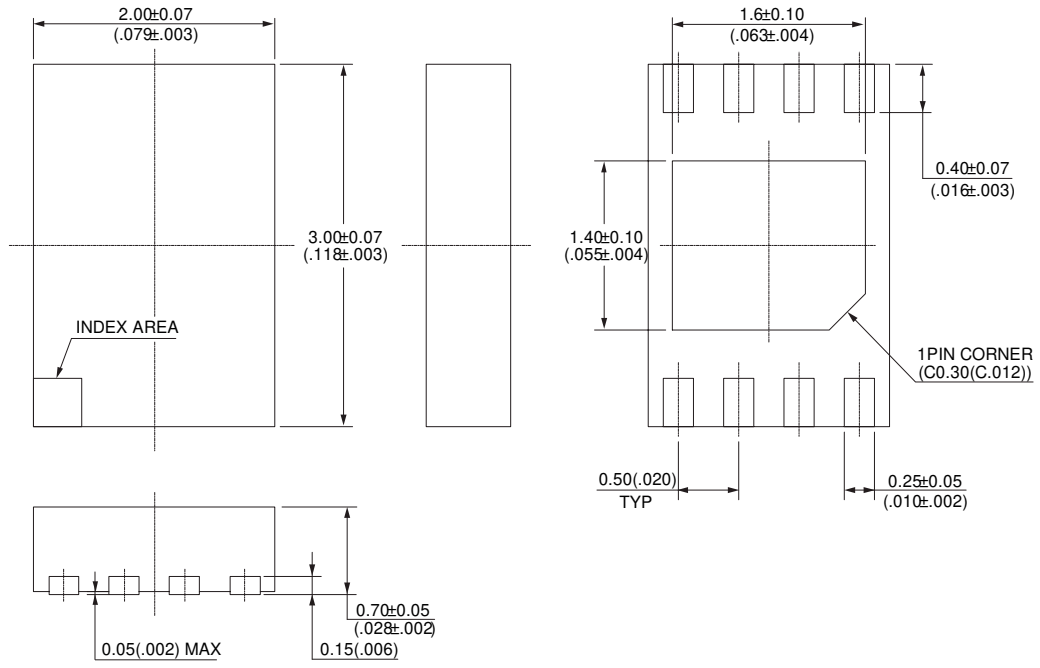
■ ORDERING INFORMATION

Part number	Package	Remarks
MB94R330PN-G-AMERE1	8-pin plastic SON (LCC-8P-M04)	Emboss taping

■ PACKAGE DIMENSIONS

8-pin plastic SON		
	Lead pitch	0.5 mm
	Package width × package length	2.0 mm × 3.0 mm
	Sealing method	Plastic mold
	Mounting height	0.75 mm MAX
	Weight	0.015g
(LCC-8P-M04)		

8-pin plastic SON
(LCC-8P-M04)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

MEMO

MEMO

MEMO

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