EVB-LAN9250 Evaluation Board User's Guide

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Signed for and on behalf of Microchip Technology Inc. at Chandler, Arizona, USA

Derek Carlson
VP Development Tools

12-Sep-14
Date

NOTES:

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Preface

NOTICE TO CUSTOMERS

All documentation becomes dated, and this manual is no exception. Microchip tools and documentation are constantly evolving to meet customer needs, so some actual dialogs and/or tool descriptions may differ from those in this document. Please refer to our web site (www.microchip.com) to obtain the latest documentation available.

Documents are identified with a "DS" number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is "DSXXXXXA", where "XXXXX" is the document number and "A" is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE online help. Select the Help menu, and then Topics to open a list of available online help files.

INTRODUCTION

This chapter contains general information that will be useful to know before using the EVB-LAN9250. Items discussed in this chapter include:

- Document Layout
- Conventions Used in this Guide
- The Microchip Web Site
- Development Systems Customer Change Notification Service
- Customer Support
- Document Revision History

DOCUMENT LAYOUT

This document describes how to use the EVB-LAN9250 Evaluation Board as a development tool for the LAN9250. The manual layout is as follows:

- **Chapter 1. "Overview"** – Shows a brief description of the EVB-LAN9250 Evaluation Board.
- **Chapter 2. "Board Details"** – Includes instructions on how to get started with the EVB-LAN9250 Evaluation Board.
- **Chapter 3. "Board Configuration"** – Provides information about the EVB-LAN9250 Evaluation Board battery charging features.
- **Appendix A. "EVB-LAN9250 Evaluation Board"** – This appendix shows the EVB-LAN9250 Evaluation Board.
- **Appendix B. "EVB-LAN9250 Evaluation Board Schematics"** – This appendix shows the EVB-LAN9250 Evaluation Board schematics.
- **Appendix C. "Bill of Materials (BOM)"** – This appendix includes the EVB-LAN9250 Evaluation Board Bill of Materials (BOM).

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

Description	Represents	Examples
Arial font:		
Italic characters	Referenced books	*MPLAB® IDE User's Guide*
	Emphasized text	...is the *only* compiler...
Initial caps	A window	the Output window
	A dialog	the Settings dialog
	A menu selection	select Enable Programmer
Quotes	A field name in a window or dialog	"Save project before build"
Underlined, italic text with right angle bracket	A menu path	*File>Save*
Bold characters	A dialog button	Click **OK**
	A tab	Click the **Power** tab
N'Rnnnn	A number in verilog format, where N is the total number of digits, R is the radix and n is a digit.	4'b0010, 2'hF1
Text in angle brackets < >	A key on the keyboard	Press <Enter>, <F1>
Courier New font:		
Plain Courier New	Sample source code	`#define START`
	Filenames	`autoexec.bat`
	File paths	`c:\mcc18\h`
	Keywords	`_asm, _endasm, static`
	Command-line options	`-Opa+, -Opa-`
	Bit values	`0, 1`
	Constants	`0xFF, 'A'`
Italic Courier New	A variable argument	*`file`*`.o`, where *`file`* can be any valid filename
Square brackets [ ]	Optional arguments	`mcc18 [options]` *`file`* `[options]`
Curly brackets and pipe character: { | }	Choice of mutually exclusive arguments; an OR selection	`errorlevel {0|1}`
Ellipses...	Replaces repeated text	`var_name [, var_name...]`
	Represents code supplied by user	`void main (void) { ... }`

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- **Emulators** – The latest information on Microchip in-circuit emulators.This includes the MPLAB REAL ICE and MPLAB ICE 2000 in-circuit emulators.
- **In-Circuit Debuggers** – The latest information on the Microchip in-circuit debuggers. This includes MPLAB ICD 3 in-circuit debuggers and PICkit 3 debug express.
- **MPLAB IDE** – The latest information on Microchip MPLAB IDE, the Windows Integrated Development Environment for development systems tools. This list is focused on the MPLAB IDE, MPLAB IDE Project Manager, MPLAB Editor and MPLAB SIM simulator, as well as general editing and debugging features.
- **Programmers** – The latest information on Microchip programmers. These include production programmers such as MPLAB REAL ICE in-circuit emulator, MPLAB ICD 3 in-circuit debugger and MPLAB PM3 device programmers. Also included are nonproduction development programmers such as PICSTART Plus and PIC-kit 2 and 3.

CUSTOMER SUPPORT

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- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

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Technical support is available through the web site at:
http://www.microchip.com/support

DOCUMENT REVISION HISTORY

Revision A (November 2015)

- Initial Release of this Document.

Chapter 1. Overview

1.1 INTRODUCTION

The LAN9250 is a full-featured, single-chip 10/100 Ethernet controller designed for embedded applications where performance, flexibility, ease of integration and system cost control are required. The LAN9250 has been specifically designed to provide high performance and throughput for 16-bit applications. The LAN9250 complies with the IEEE 802.3 (full/half-duplex 10BASE-T and 100BASE-TX) Ethernet protocol, IEEE 802.3az Energy Efficient Ethernet (EEE) [100Mbps only], and the IEEE 1588v2 precision time protocol. 100BASE-FX is supported via an external fiber transceiver.

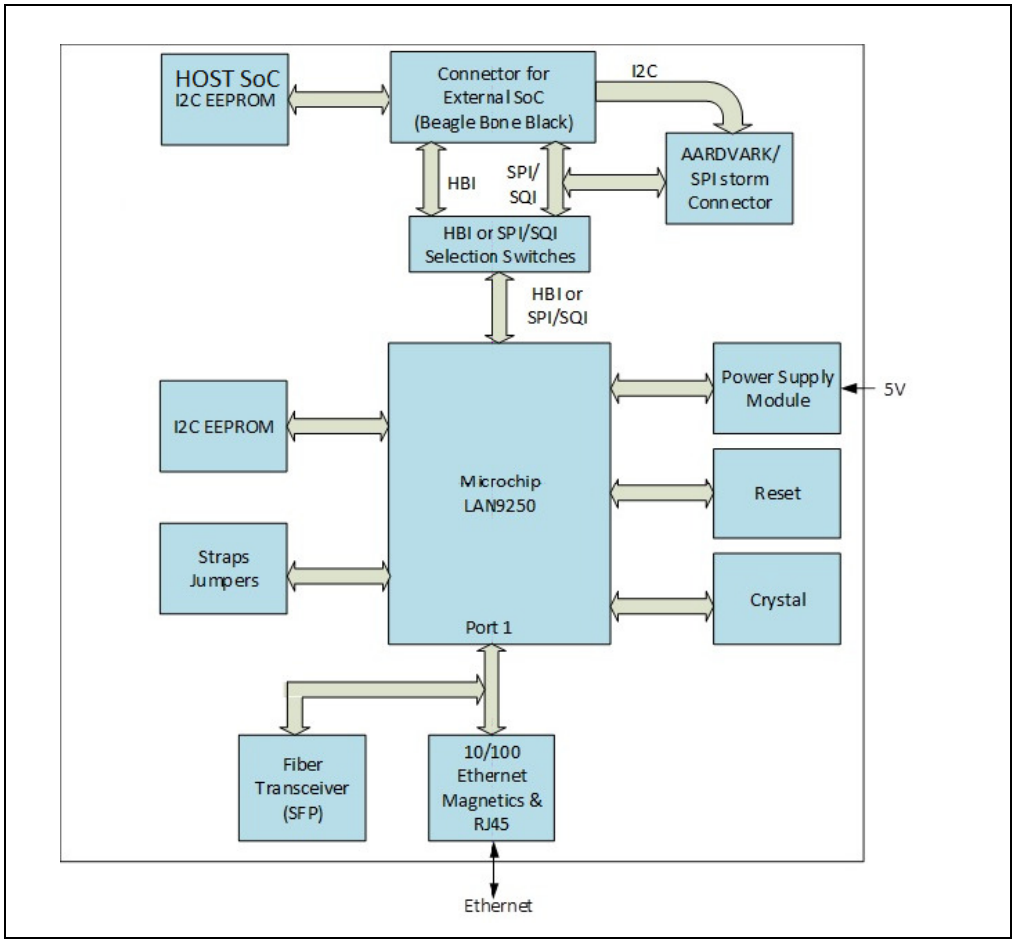
The LAN9250 includes an integrated Ethernet MAC and PHY with a high-performance SRAM-like slave interface. The integrated checksum offload engines enable the automatic generation of the 16-bit checksum for received and transmitted Ethernet frames, offloading the task from the CPU. The LAN9250 also includes large transmit and receive data FIFOs to accommodate high-latency applications. In addition, the LAN9250 memory buffer architecture allows highly efficient use of memory resources by optimizing packet granularity.

The LAN9250 also supports features which reduce or eliminate packet loss. The internal 16KB SRAM can hold over 200 received packets. If the receive FIFO gets too full, the LAN9250 can automatically generate flow control packets to the remote node, or assert back-pressure on the remote node by generating network collisions.

This manual describes the EVB designed for LAN9250 to explore its various features.

Figure 1-1 shows the block diagram.

FIGURE 1-1: LAN9250 BLOCK DIAGRAM



1.2 REFERENCES

Concepts and material available in the following documents may be helpful when reading this document. Visit www.microchip.com for the latest documentation.

Document	Location
LAN9250 Datasheet	Visit www.microchip.com.
AN8-13 Suggested Magnetics	http://www.microchip.com/wwwAppNotes/AppNotes.aspx?appnote=en562793
EVB-LAN9250 Evaluation Board Schematic	Visit www.microchip.com.

1.3 TERMS AND ABBREVIATIONS

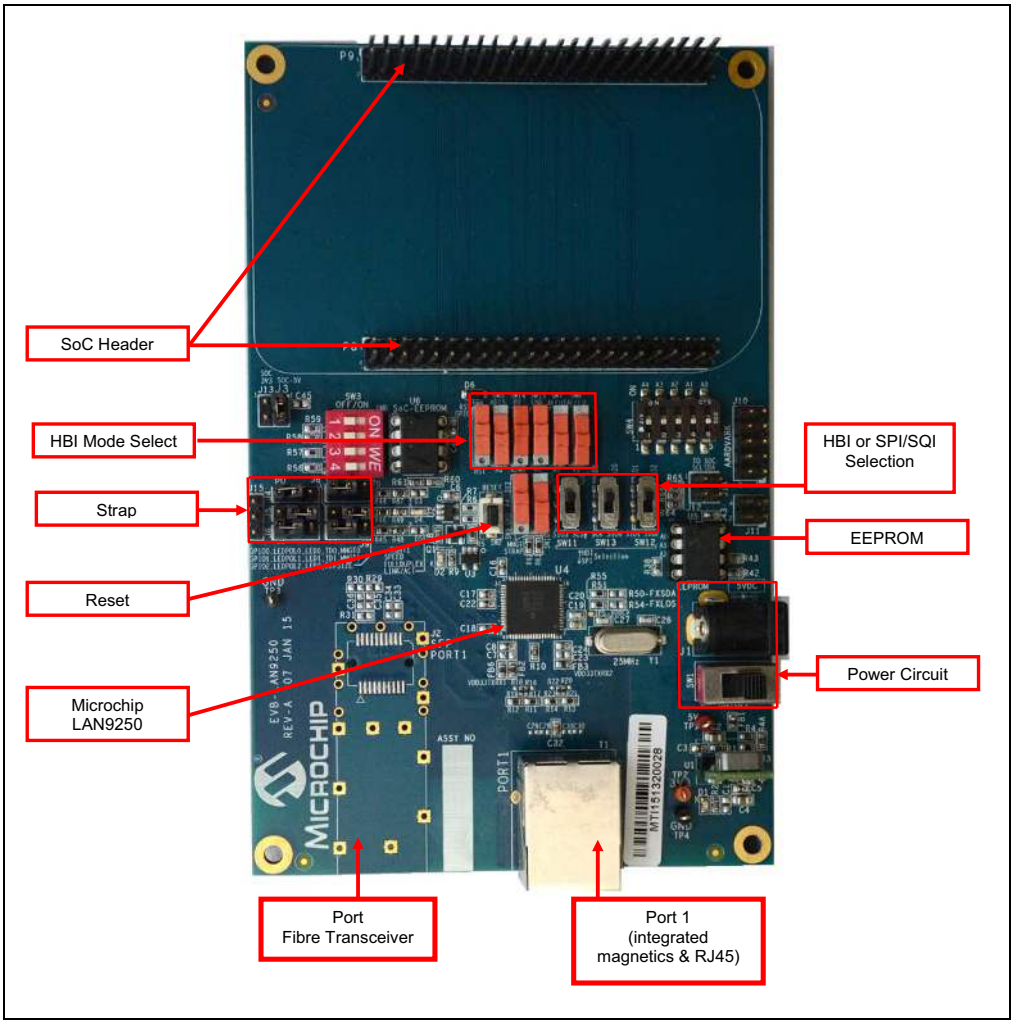
- EVB - Evaluation Board
- DNP - Do Not Populate
- 100BASE-TX- 100 Mbps Fast Ethernet, IEEE802.3u Compliant
- GPIO - General Purpose I/O
- HBI - Host Bus Interface
- SPI - Serial Peripheral Interface
- I^2C - Inter-Integrated Circuit
- EEE - Energy-Efficient Ethernet
- SFP - Small Form-factor Pluggable
- SoC - System on a Chip

NOTES:

Chapter 2. Board Details

The following sections describe the various board features, including jumpers, LEDs, test points, system connections, and switches. A top view of the EVB-LAN9250 is shown in Figure 2-1.

FIGURE 2-1: LAN9250 BOARD REV-A WITH CALL OUTS



2.1 POWER

DC 5V is applied through (J1) DC Socket, powered by a +5V external wall adapter (Manufacturer: TRIAD MAGNETICS and P/N: WSU050-3000). The switch (SW1) needs to be in the ON position for the 5V to reach the 3.3V regulator. Glowing of Green LED (D1) indicates successful generation of 3.3V o/p. This Power is supplied to the LAN9250 and it has internal 1.2 V regulator which supplies power to the internal core logic.

2.2 POWER-ON RESET

A power-on reset occurs whenever power is initially applied to the LAN9250 or if the power is removed and reapplied to the LAN9250. This event resets all circuitry within the LAN9250. After initial power-on, the LAN9250 can be reset by pressing the reset switch (SW2). The reset LED D2 will assert (Red) when the LAN9250 is in reset condition. For stability, a delay of approximately 180ms is added from the +3.3V o/p to reset release.

2.3 CLOCK

The LAN9250 requires a fixed-frequency 25MHz clock source for use by the internal clock oscillator and PLL. This is typically provided by attaching a 25MHz crystal to the OSCI and OSCO pins.

Manufacturer: Cardinal Components Inc and P/N: CSM1Z-A5B2C5-40-25.0D18-F

Chapter 3. Board Configuration

3.1 STRAP OPTIONS

The following tables describe the default settings and jumper descriptions for the EVB-LAN9250. These defaults are the recommended configurations for evaluation of the LAN9250. These settings may be changed as needed, however, any deviation from the defaults settings should be approached with care and knowledge of the schematics and datasheet. An incorrect jumper setting may disable the board.

3.1.1 GPIO Straps

The GPIO/LED Controller provides 3 configurable general purpose input/output pins, GPIO[2:0]. These pins can be individually configured to function as inputs, push-pull outputs or open drain outputs and each is capable of interrupt generation with configurable polarity. Alternatively, all 3 GPIO pins can be configured as LED outputs, enabling these pins to drive Ethernet status LEDs for external indication of various attributes of the port. All GPIOs also provide extended 1588 functionality.

Table 3-1 illustrates how the GPIO lines are multiplexed with other signals.

TABLE 3-1: GPIO STRAPS

GPIO Line	Multiplexed Signals
GPIO 0	LED0/MNGT0/TD0
GPIO 1	LED1/MNGT1/TD1
GPIO 2	LED2/E2PSIZE

3.1.2 GPIO Header

J16 is used GPIO Header for probing purpose. Respective pin details shared in Table 3-2.

TABLE 3-2: GPIO HEADER

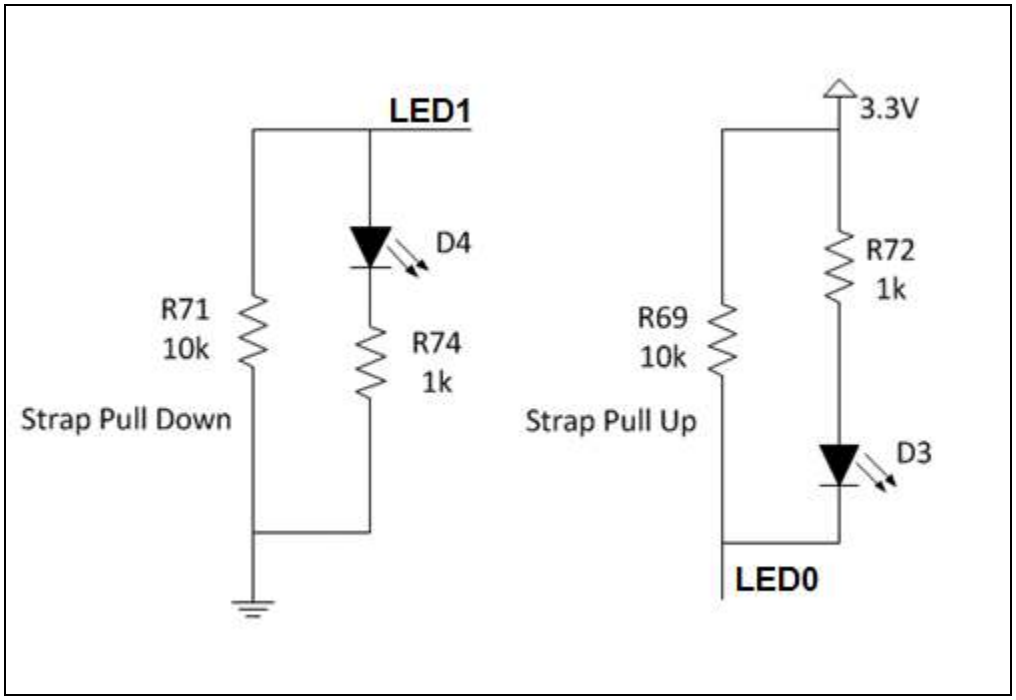
GPIO Line	Multiplexed Signals
GPIO 0	J16.1
GPIO 1	J16.2
GPIO 2	J16.3

In the context of using the GPIO signals as LED controller, the Jumpers J4-J9 (operated in pairs) are configured as below.

For example, J4 and J7 as a pair set as '0' or '1', decide whether LED0 (D3) is turned on or OFF.

Likewise, J6 and J9 as a pair set as '0' or '1', decide whether LED1 (D4) is turned on or OFF.

FIGURE 3-1: LED STRAP CIRCUIT



The following subsections detail the jumper pair settings, their associated strap settings, and the functional effects of setting the straps. All strap values are read during power-up and on the rising edge of nRST signal. Once the strap value is set, the LAN9250 will drive the LED's high or low for illumination according the strap value. For other designs which may use these pins as GPIOs refer to LAN9250 datasheet for additional information. In those cases, internal default straps must be changed by an I^2C or through EEPROM fields.

3.1.2.1 GPIO/LED CONFIGURATIONS

GPIO/LED configuration straps are used to configure the LEDs and GPIOs through jumpers as shown below in Table 3-3.

TABLE 3-3: GPIO/LED CONFIGURATIONS

Header	Pin Settings	Signal Name	Strap Value	Description
J4 & J7	1-2(default)	GPIO0 /LED0	1	The LED (D3) is set as active LOW./ Serial Management Mode Stratp:0=SMI
	2 -3		0	The LED (D3) is set as active HIGH./ Serial Management Mode Strap:1=I^2C
J5 & J8	1-2(default)	GPIO1 /LED1	1	The LED (D4) is set as active LOW.
	2 -3		0	The LED (D4) is set as active HIGH.
J6 & J9	1-2(default)	GPIO2 /LED2	1	The LED (D5) is set as active LOW./ EEPROM Size=32K bits
	2 -3		0	The LED (D5) is set as active HIGH./ EEPROM Size=1K bits

3.1.2.2 HOST INTERFACE MODE STRAP SELECTION

MNGT0 strap along with MNGT1, MNGT2 and MNGT3 configures the host mode.

MNGT0 and MNGT1 are multiplexed with GPIO0 and GPIO1 signals whereas MNGT3 and MNGT4 are multiplexed with address lines A3 and A4.

Table 3-4 illustrates the selection of Host mode based on the values of MNGT straps.

TABLE 3-4: MANAGEMENT STRAP SELECTION

MNGT1 J5 & J8	MNGT0 J4 & J7	MNGT3 SW9	MNGT2 SW10	Host Mode
0	0	X	X	SPI
0	1	0	0	HBI Multiplexed 1 Phase 8-bit
0	1	0	1	HBI Multiplexed 1 Phase 16-bit
0	1	1	0	HBI Multiplexed 2 Phase 8-bit
0	1	1	1	HBI Multiplexed 2 Phase 16-bit (Default)
1	0	X	X	HBI Indexed 8-bit
1	1	X	X	HBI Indexed 16-bit

3.1.2.3 EEPROM SIZE CONFIGURATION

The EEPROM size configuration strap (J6 & J9) [Multiplexed with GPIO2 signal] determines the supported EEPROM size range. A low selects 1Kbit (128 x 8) through 16Kbits (2K x 8)_24C16. A high selects 32Kbits (4K x 8) through 512Kbits (64K x 8) or 4Mbits (512K x 8)_24C512 as shown below in Table 3-5.

TABLE 3-5: EEPROM SIZE CONFIGURATION

Header	Pin Settings	eeprom_size_strap Value	Description
J6 & J9	1-2 (default)	1	EEPROM size = 32K bits (4k x 8) through 512K bits (64K x 8)
	2 -3	0	EEPROM size = 1K bits (128 x 8) through 16K bits (2K x 8)

3.1.3 External SoC

Purpose of External SoC is to provide HBI and SPI access to the LAN9250.

P8 and P9 connectors are used for mounting external SoC Module and which is compatible with BeagleBone (TI SoC).

The jumper J13 is used to provide on-board 3.3V to BeagleBone Black.

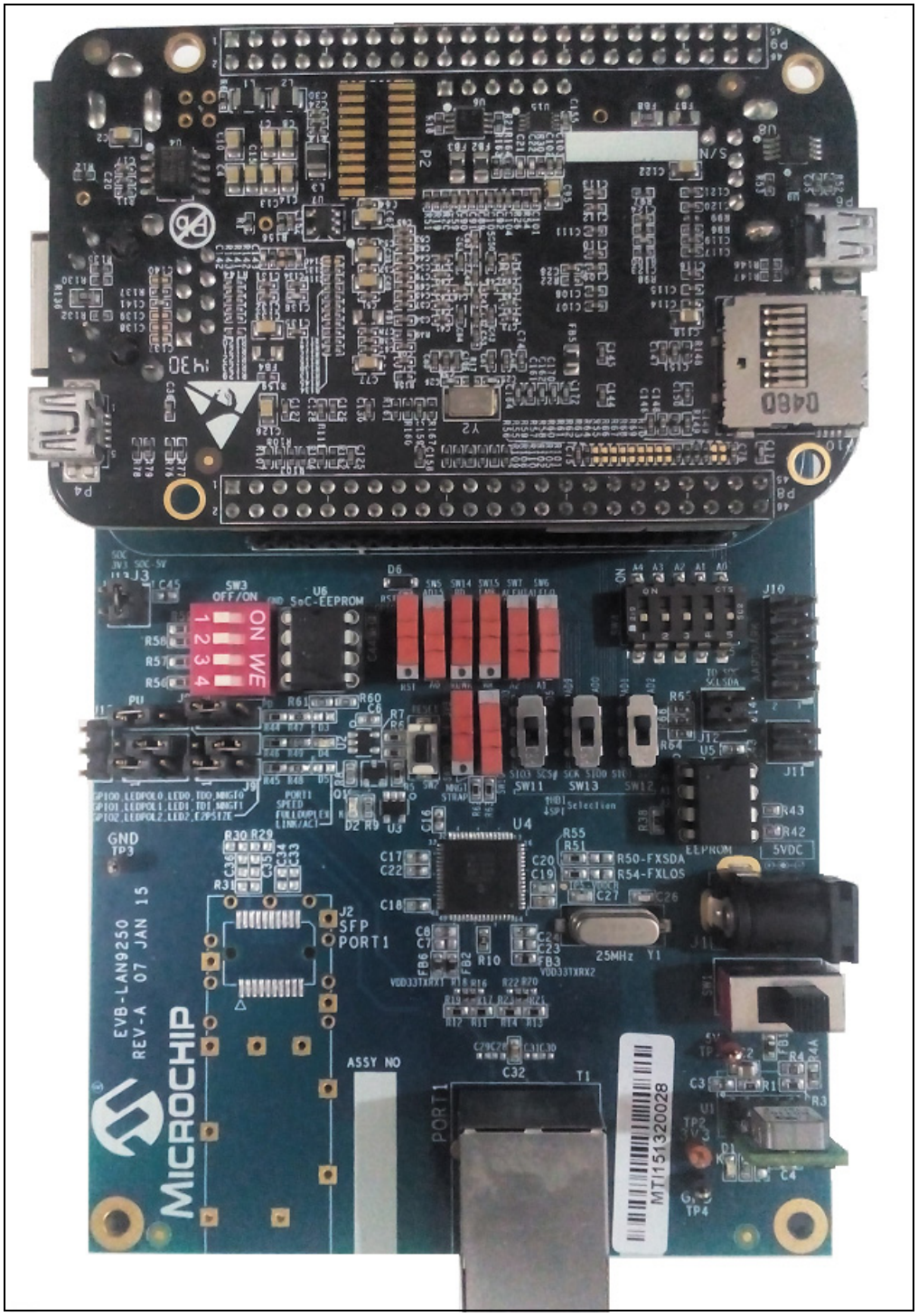
TABLE 3-6: EXTERNAL SOC SETTINGS

Header	Default Pin Settings	Signal Name
J3	1-2 (Short)	VDD_5V
J13	1-2 (Open)	VDD3V3EXP

Refer to this link for a detailed discussion on BeagleBone Black: http://www.newark.com/beagle-bone-accessories?rd=beaglebone&catalogId=15003&langId=-1&storeId=10194

Figure 3-2 shows how BeagleBone Black is mounted on EVB-LAN9250.

FIGURE 3-2: EVB-LAN9250 WITH BEAGLEBONE BLACK



3.1.4 HBI/SPI Selection

The EVB-LAN9250 supports two host interface modes of LAN9250:

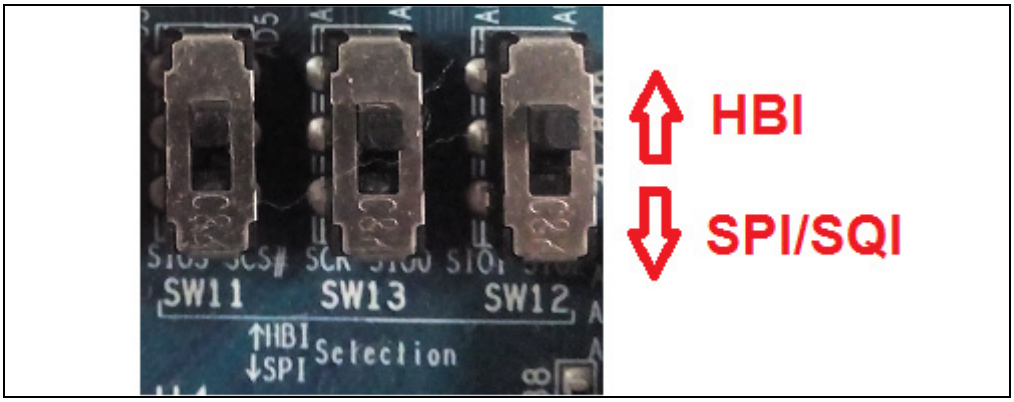
- HBI Mode (default)
- SPI/SQI Mode

The HBI or SPI/SQI configuration is selected using the DPDT SW11 to SW13 switches.

TABLE 3-7: HBI AND SPI/SQI SWITCH CONFIGURATIONS

Switch	Description	Settings
SW11 to SW13	Up	HBI Mode (Default)
SW11 to SW13	Down	SPI/SQI Mode

FIGURE 3-3: SW11-SW13 HBI AND SPI/SQI MODE SELECTION



3.1.5 HBI Mode Selection

The LAN9250 supports various HBI modes. The HBI modes (Multiplexed Modes and Indexed Modes) can be selected using the SPST switches (P/N: 450301014042-Wurth Electronics) SW4 through SW6 and SW11 through SW12. The LAN9250 HBI signals are connected to the SoC through the switches.

3.1.5.1 MULTIPLEXED MODES

The following four HBI Multiplexed Modes are supported:

1. 8-bit Multiplexed single-phase mode
2. 16-bit Multiplexed single-phase mode
3. 8-bit Multiplexed dual-phase mode
4. 16-bit Multiplexed dual-phase mode

The BeagleBone Black will be configured by installing a specific driver available from www.microchip.com. This is required to access LAN9250 through HBI Multiplexed mode.

The switch selection for Multiplexed Mode is shown in Figure 3-4. All four Multiplexed Modes utilize the same switch positions.

FIGURE 3-4: MULTIPLEXED HBI MODE SELECTION

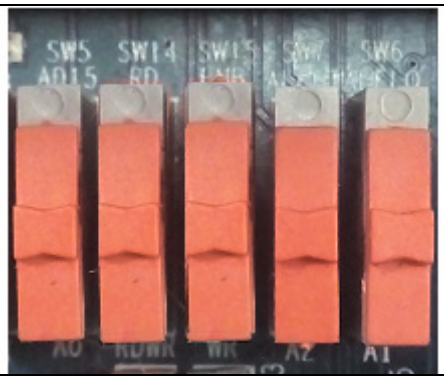


TABLE 3-8: SWITCH SELECTION FOR MULTIPLEXED MODE

Switch	Description
SW5	Down
SW14	Down
SW15	Down
SW7	Down
SW6	Down

Note: For Switches to short 1-2, knob position must be in the 1-3 position, and vice versa.

3.1.5.2 INDEXED MODE

Two Indexed modes are supported, namely 8-bit and 16-bit. The BeagleBone Black will be configured by installing a specific driver available from www.microchip.com. This is required to access LAN9250 through HBI Indexed mode.

Note: In this mode, DIP switch SW15 to ON Position for PIC32 SoC and OFF Position for SoC.

FIGURE 3-5: 8-BIT INDEXED MODE SWITCH SELECTION

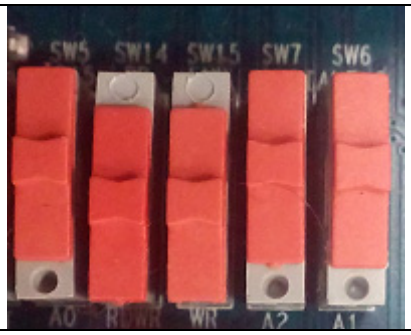


TABLE 3-9: SWITCH SELECTION FOR 8-BIT INDEXED MODE

Switch	Description
SW5	Up
SW14	Down
SW15	Down
SW7	Up
SW6	Up

Note: For Switches to short 1-2, knob position must be in the 1-3 position, and vice versa.

FIGURE 3-6: 16-BIT INDEXED MODE SWITCH SELECTION

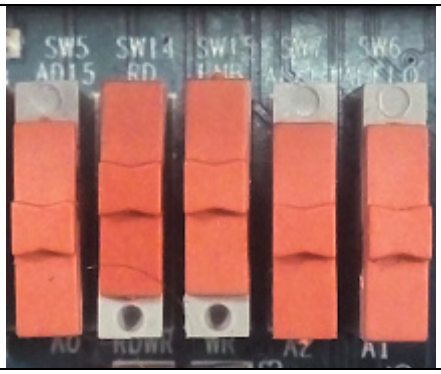


TABLE 3-10: SWITCH SELECTION FOR 16-BIT INDEXED MODE

Switch	Description
SW5	Down
SW14	Up
SW15	Up
SW7	Down
SW6	Down

Note: For Switches to short 1-2, knob position must be in the 1-3 position, and vice versa.

3.1.6 SPI/SQI Mode Selection

The LAN9250 supports SPI/SQI Mode. The SPI/SQI Mode will be selected using the DPDT SW11 to SW13 switches as shown in Figure 3-3.

3.1.7 I²C Aardvark® Header and SPI Storm Header

3.1.7.1 I²C AARDVARK HEADER

J10 connector is used for I²C Aardvark header. Respective pin details are given in Table 3-11.

TABLE 3-11: PIN NAMES FOR I²C AARDVARK HEADER

Signal Name	Pin Number
I2C2_SCL	J10.1
I2C2_SDA	J10.3
GND	J10.2 & J10.10

3.1.7.2 SPI STORM HEADER

J10+J11 connectors are used for SPI Storm header. Respective pin details are given in Table 3-12.

TABLE 3-12: PIN NAMES FOR SPI STORM HEADER

Signal Name	Pin Number
SIO1	J10.5
SCK	J10.7
SCS#	J10.9
SIO0	J10.8
SIO2	J11.3
SIO3	J11.4
GND	J10.2, J10.10, J11.1 & J11.2

3.1.8 Copper and Fiber Mode Selections

The LAN9250 supports 100BASE-TX (Copper) and 100BASE-FX (Fiber) modes. In 100BASE-FX operation, the presence of the receive signal is indicated by the external transceiver as either an open drain, CMOS level, Loss of Signal (SFP) or a LVPECL Signal Detect (SFF).

This EVB supports 100BASE-TX (Copper) and 100BASE-FX (Fiber) in SFP mode. By default, Copper Mode is active. Fiber Mode is supported as an assembly option. To select the Copper or Fiber Mode, the respective strap and signal routing resister assembly options must be configured.

Note: Vendor part number for SFP Transceiver: Finisar/FTLF1217P2.

3.1.8.1 COPPER MODE

The EVB-LAN9250 is set to Copper Mode by default. Table 3-13 details the required strap resistors settings for Copper Mode operation.

TABLE 3-13: COPPER MODE STRAP RESISTORS

Resistors	Signal Names	Description
R55 (10K)	FXLOSEN	Copper twisted pair for port 1 further determined by FXSDENA
R51 (10K)	FXSDA	Configures Port 1 to Copper Mode

Note: R54 and R50 must not be populated (DNP).

Additionally, the signal routing resistors detailed in Table 3-14 must be assembled for Copper Mode operation.

TABLE 3-14: COPPER MODE SIGNAL ROUTING RESISTORS

Resistors	Description
R17, R19, R21, R23	Port 1 Copper mode is Enabled

Note: R16, R18, R20, R22 (0402 package) must not be populated (DNP).

3.1.8.2 FIBER MODE

The LAN9250 supports SFP type 100BASE-FX mode. To enable Fiber Mode, the respective strap and signal routing resisters must be configured.

Note: Copper Mode related resistors must be DNP while Fiber Mode is active (refer to **Section 3.1.8.1 "Copper Mode"**).

Table 3-15 details the required strap resistor settings for Fiber Mode operation.

TABLE 3-15: FIBER MODE STRAP RESISTORS

Resistors	Description
R54	Port 0 Fiber mode is Enabled
R50	Port 1 Fiber mode is Enabled

Note: R51 and R55 must not be populated (DNP).

Additionally, the signal routing resistors detailed in Table 3-16 must be assembled as well for Fiber Mode operation.

TABLE 3-16: FIBER MODE SIGNAL ROUTING RESISTORS

Resistors	Description
R16, R18, R20, R22	Port 1 Fiber mode is Enabled

Note: R17, R19, R21, R23 (0402 package) must not be populated (DNP).

3.1.8.3 FX-LOS FIBER MODE STRAP

FX-LOS strap details are shown in Table 3-17. These strap settings determine if the ports are to operate in FX-LOS Fiber Mode or FX-SD/Copper Mode.

TABLE 3-17: FX-LOS MODE STRAP SETTINGS

R77 (10K)	R79 (10K)	Reference Voltage (v)	Function
Populate	DNP	3.3	A level above 2V selects FX-LOS for Port 1
DNP	Populate	0 (Default)	A level of 0V selects FX-SD / Copper twisted pair for Port 1, further determined by FXSDA

Note: The above strap details describe the LAN9250 function. This EVB does not support SFF Fiber Mode. Therefore, FX-SD related straps are not applicable.

3.2 LEDS

LED details are shown in Table 3-18.

TABLE 3-18: LEDS

Reference	Color	Indication
D1	Green	3.3V Power active
D2	Red	LAN9250 is in reset condition

3.3 TEST POINTS

Test points are shown in Table 3-19.

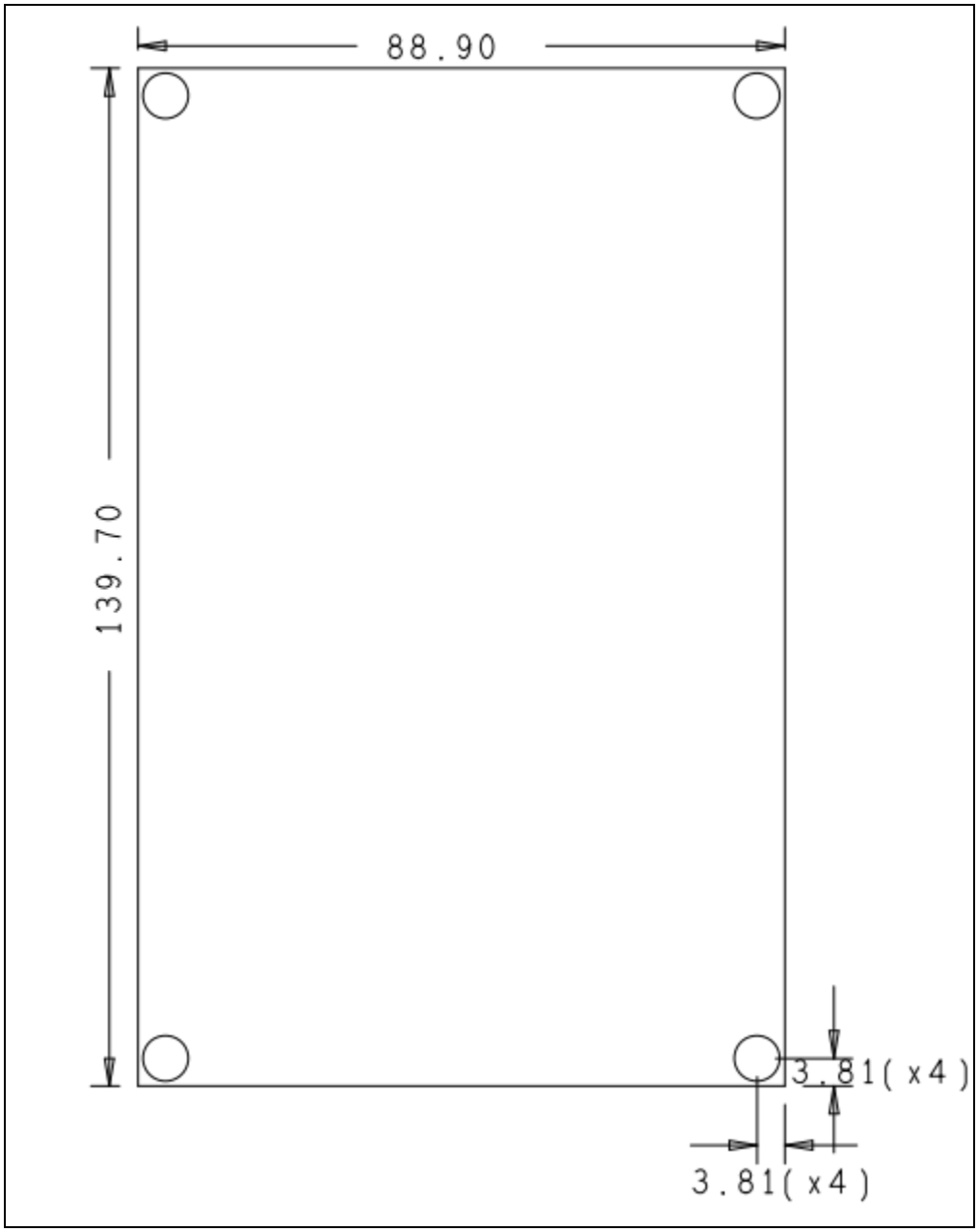
TABLE 3-19: TEST POINTS

Test Points	Description	Connection
TP1	Single-pin populated 5V	5V_EXT
TP2	Single-pin populated 3V3	3V3
TP3	Single-pin populated GND	GND
TP4	Single-pin populated GND	GND
TP5	Single-pin unpopulated VDDCR	VDDCR/1.2V

3.4 MECHANICALS

Figure 3-7 details for EVB-LAN9250 mechanical dimensions. Dimensions are in mm.

FIGURE 3-7: EVB-LAN9250 MECHANICAL DIMENSIONS



NOTES:

Appendix A. EVB-LAN9250 Evaluation Board

A.1 INTRODUCTION

This appendix shows the EVB-LAN9250 Evaluation Board.

FIGURE A-1: EVB-LAN9250 EVALUATION BOARD

NOTES:

Appendix B. EVB-LAN9250 Evaluation Board Schematics

B.1 INTRODUCTION

This appendix shows the EVB-LAN9250 Evaluation Board Schematics.

FIGURE B-1: POWER SUPPLY & RST

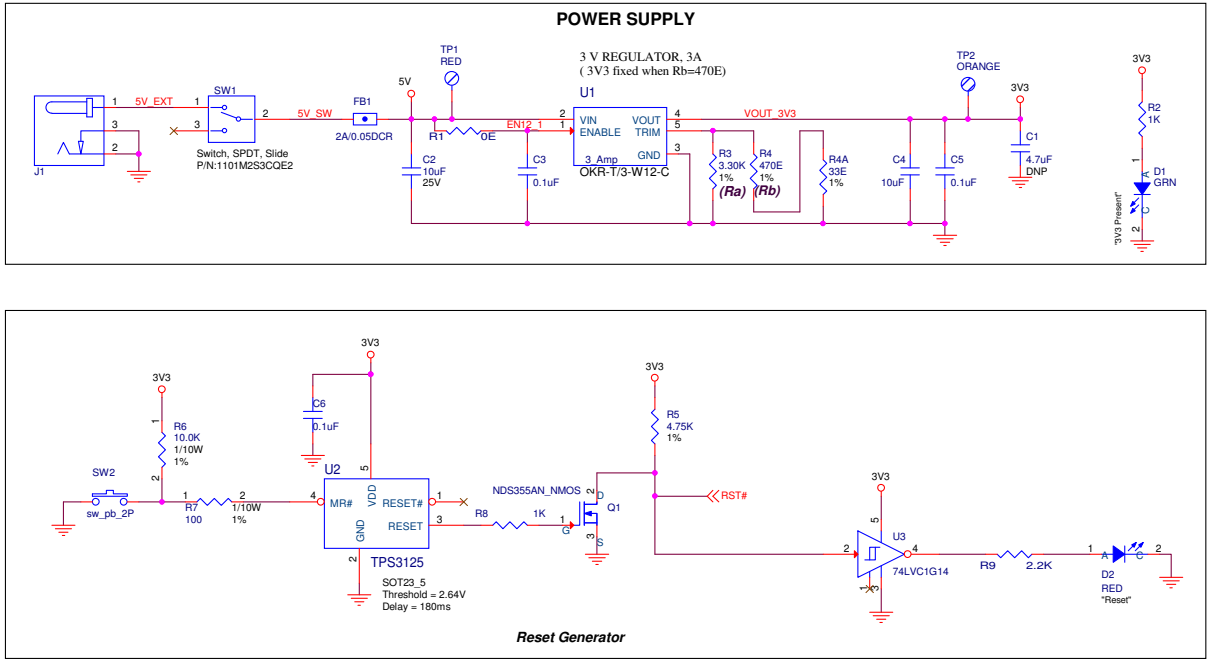


FIGURE B-2: LAN9250 (PART1)

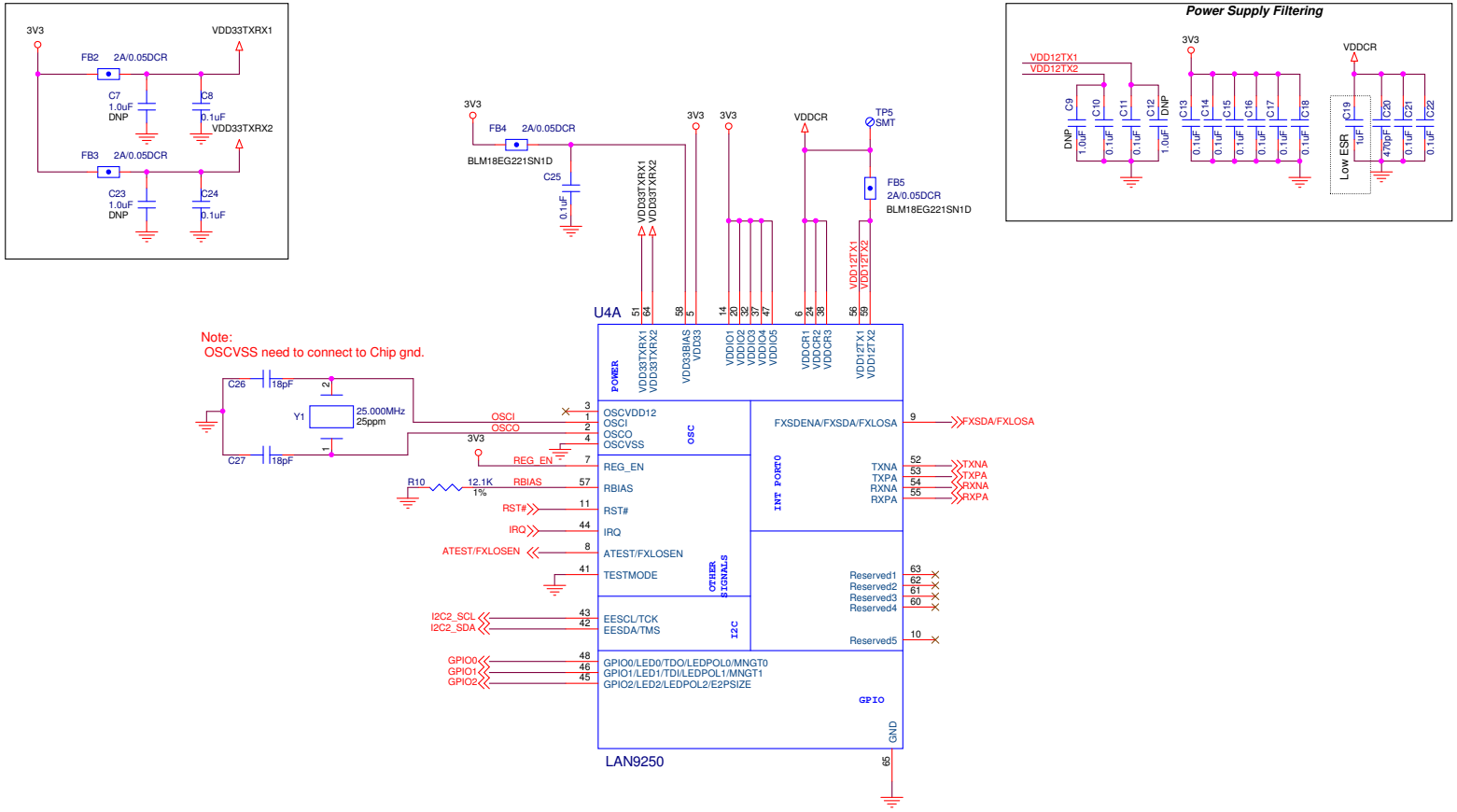


FIGURE B-3: COPPER MODE INTERFACE

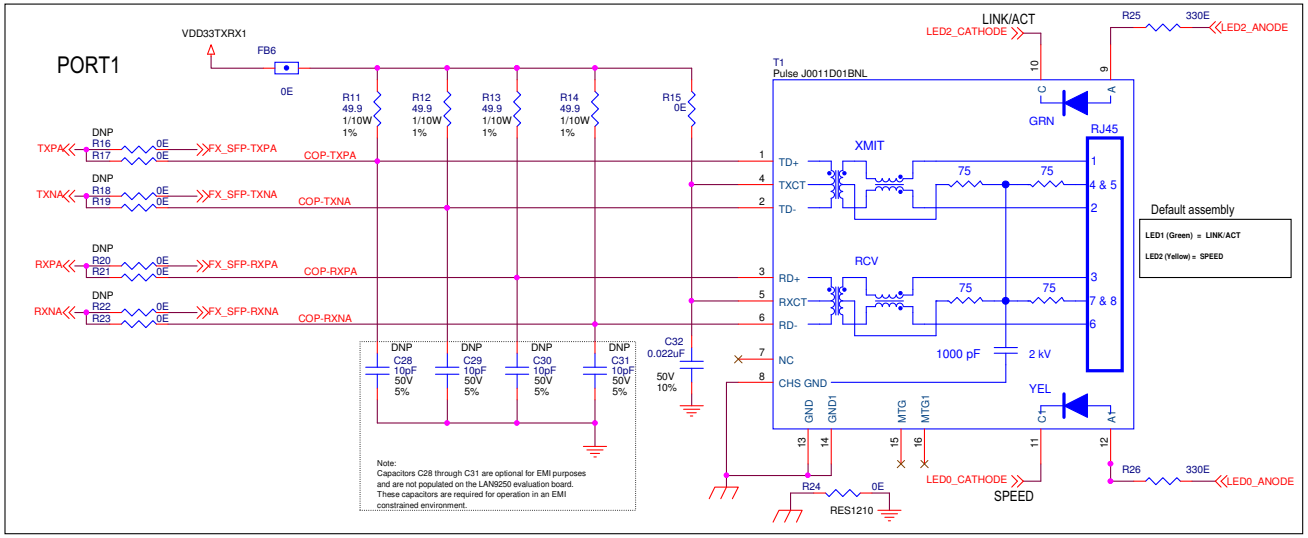
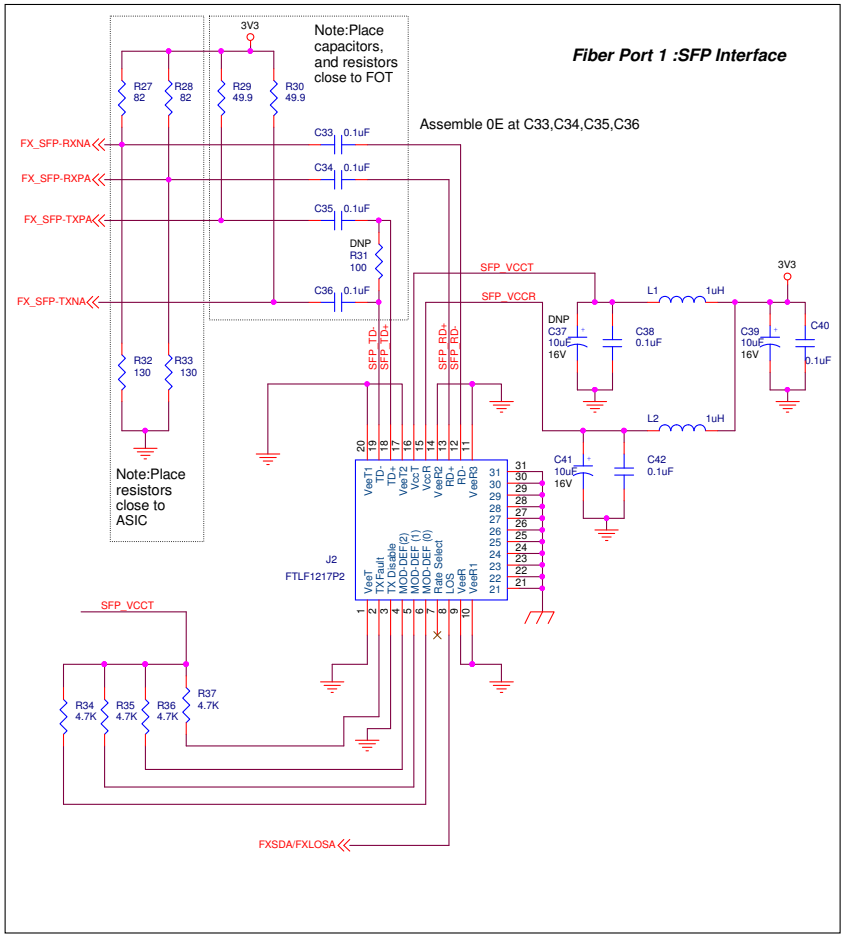
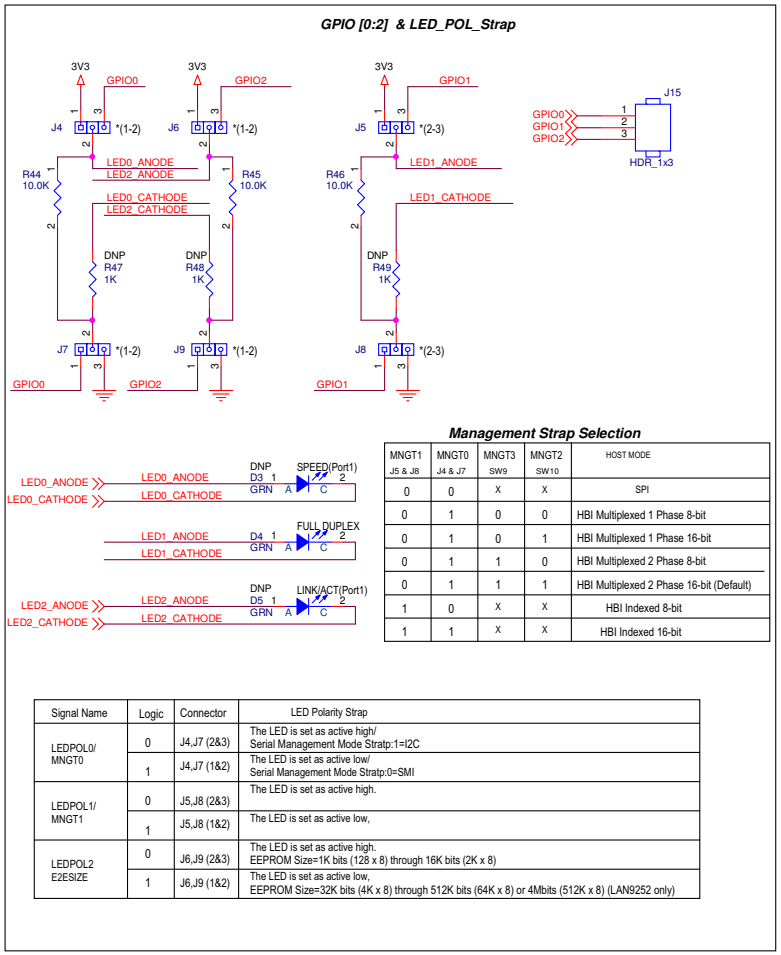


FIGURE B-4: SFP INTERFACE



Note: Fiber mode related components are Not Populated on EVB (Default)

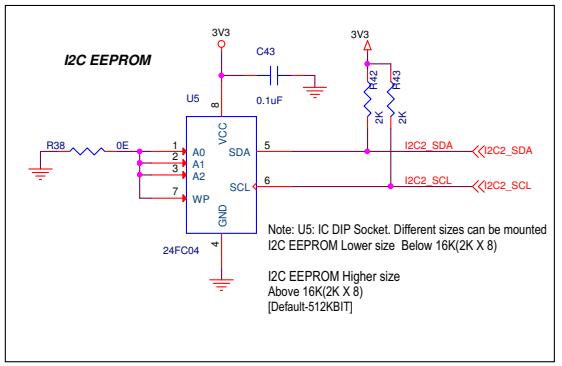
FIGURE B-5: STRAP, GPIO, I²C & FX-LOS

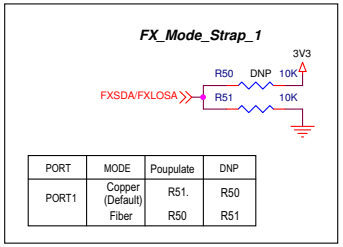


Management Strap Selection

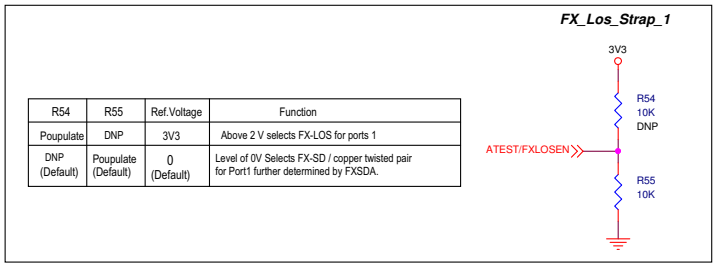
MNGT1 J5 & J8	MNGT0 J4 & J7	MNGT3 SW9	MNGT2 SW10	HOST MODE
0	0	X	X	SPI
0	1	0	0	HBI Multiplexed 1 Phase 8-bit
0	1	0	1	HBI Multiplexed 1 Phase 16-bit
0	1	1	0	HBI Multiplexed 2 Phase 8-bit
0	1	1	1	HBI Multiplexed 2 Phase 16-bit (Default)
1	0	X	X	HBI Indexed 8-bit
1	1	X	X	HBI Indexed 16-bit

Signal Name	Logic	Connector	LED Polarity Strap
LEDPOL0/ MNGT0	0	J4,J7 (2&3)	The LED is set as active high/ Serial Management Mode Stratp:1=I2C
	1	J4,J7 (1&2)	The LED is set as active low/ Serial Management Mode Stratp:0=SMI
LEDPOL1/ MNGT1	0	J5,J8 (2&3)	The LED is set as active high.
	1	J5,J8 (1&2)	The LED is set as active low,
LEDPOL2 E2ESIZE	0	J6,J9 (2&3)	The LED is set as active high. EEPROM Size=1K bits (128 x 8) through 16K bits (2K x 8)
	1	J6,J9 (1&2)	The LED is set as active low, EEPROM Size=32K bits (4K x 8) through 512K bits (64K x 8) or 4Mbits (512K x 8) (LAN9252 only)





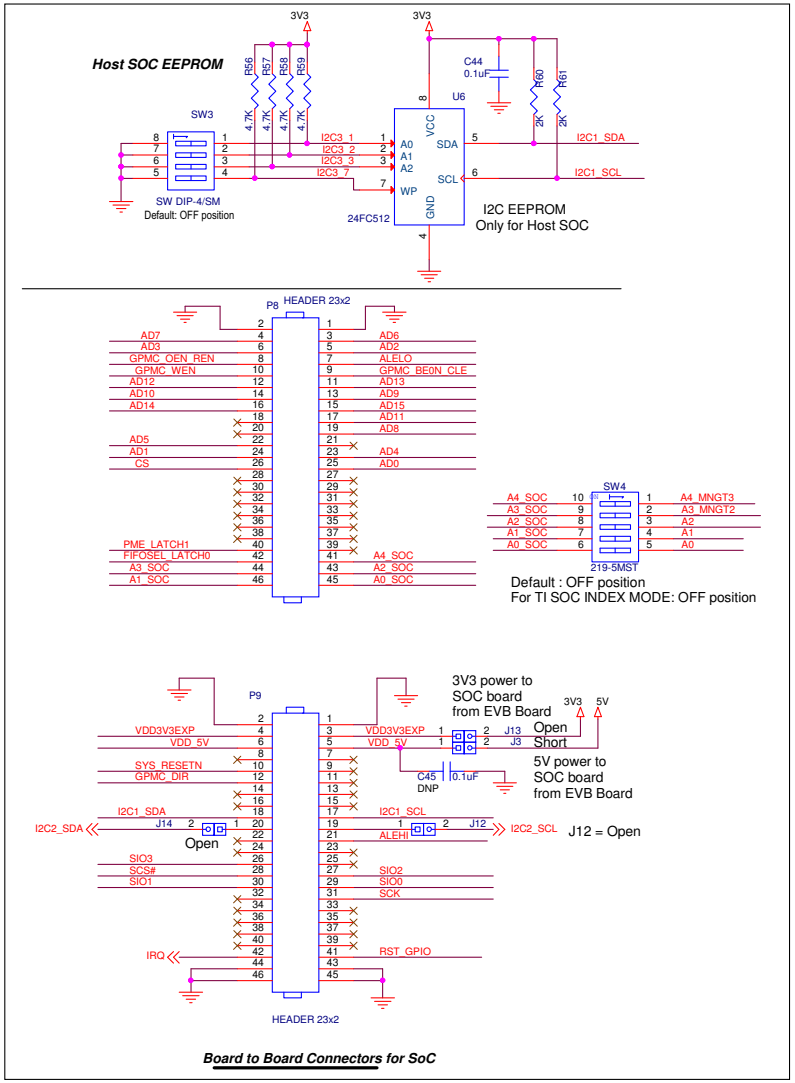
PORT	MODE	Poupulate	DNP
PORT1	Copper (Default)	R51.	R50
	Fiber	R50	R51

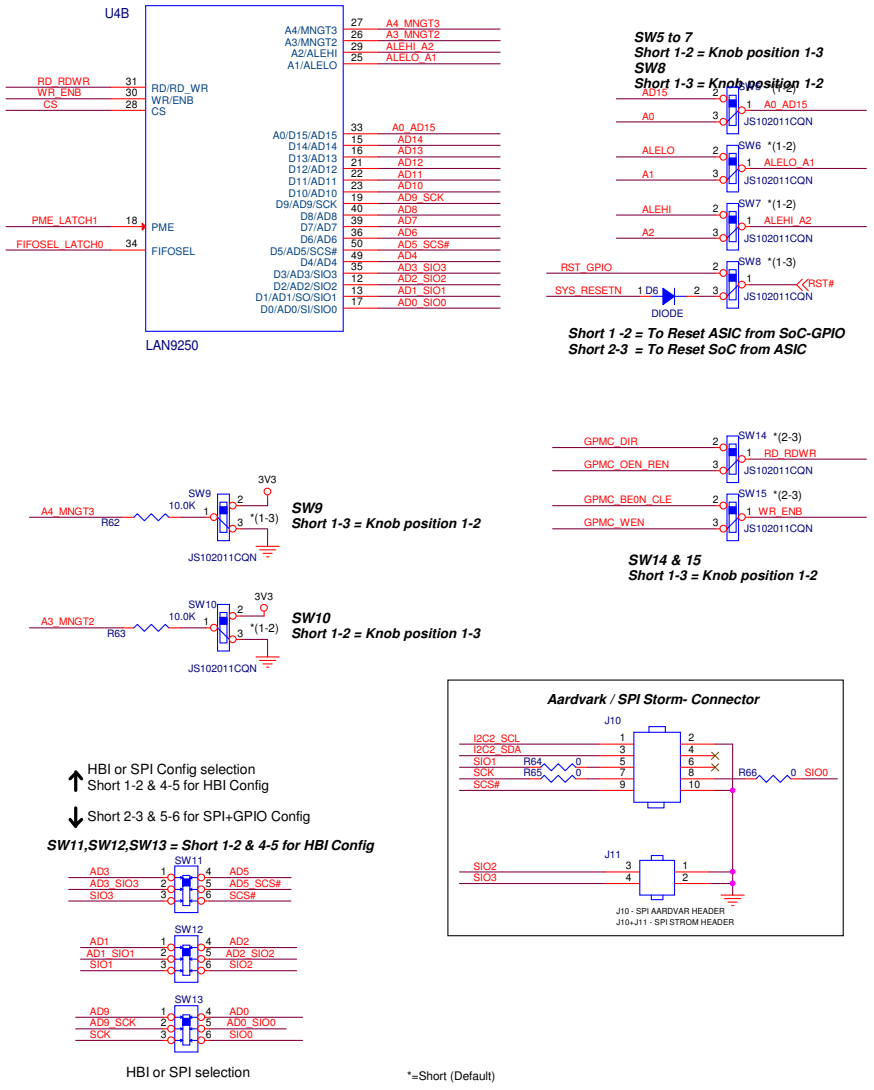


R54	R55	Ref.Voltage	Function
Poupulate	DNP	3V3	Above 2 V selects FX-LOS for ports 1
DNP (Default)	Poupulate (Default)	0 (Default)	Level of 0V Selects FX-SD / copper twisted pair for Port1 further determined by FXSDA.

*=Short (Default)

FIGURE B-6: LAN9250 (PART 2)





NOTES:

Appendix C. Bill of Materials (BOM)

C.1 INTRODUCTION

This appendix includes the EVB-LAN9250 Evaluation Board Bill of Materials (BOM).

TABLE C-1: EVB-LAN9250 EVALUATION BOARD BILL OF MATERIALS

Item	Qty	Reference	Part	PCB Footprint	DNP	Manufacturer	Manufacturer Part Number
2	2	C2,C4	10uF	CAP0805	No	Murata	GRM21BR61E106KA73L
3	18	C3,C5,C6,C8,C10,C11,C13,C14,C15, C16,C17,C18,C21,C22,C24,C25,C43, C44	0.1uF	CAP0603	No	Murata	GRM155R61E104KA7D
5	1	C19	1uF	CAP0603	No	Murata	GRM188R61C105KA93D
6	1	C20	470pF	CAP0603	No	Murata	GRM033R71E471KA01D
7	2	C26,C27	18pF	CAP0603	No	Murata	GRM1885C1H180JA01D
9	1	C32	0.022uF	CAP0603	No	Kemet	C0603C223K5RACTU
12	2	D1,D4	GRN	LED0603	No	Wurth electronics	150 060 GS7 500 0
13	1	D2	RED	LED0603	No	Wurth electronics	150 060 RS7 500 0
15	1	D6	DIODE	SOD123	No	Micro Commercial Co	1N4148W-TP
16	6	FB1,FB2,FB3,FB4,FB5,FB6	2A/0.05DCR	RES0603	No	Murata	BLM18EG221SN1D
17	1	J1	SKT_PWR_2R0mm_4A_THRU_RA	th_conn_pwrjack_dc-210_rt	No	Cui Stack	PJ-002AH
19	4	J3,J12,J13,J14	CONN_2P	th_conn_1x2p	No	FCI	68000-102HLF
20	7	J4,J5,J6,J7,J8,J9,J16	HDR_1x3	TH_CONN_1X3P	No	FCI	68000-103HLF
21	1	J10	HEADER 5X2	TH_CONN_2X5P	No	FCI	67997-210HLF
22	1	J11	HEADER 2X2	TH_CONN_2X2P	No	FCI	67997-204HLF
24	2	P8,P9	HEADER 23x2	TH_CONN_2X23P_F	No	FCI	67996-8 46 150 030 LF
25	1	Q1	NDS355AN_NMOS	sot23-NDS	No	Fairchild	NDS355AN
26	2	R2,R8	1K	RES0603	No	Panasonic	ERJ-3GEYJ102V
27	6	R1,R15,R38,R64,R65,R66	0E	RES0603	No	Panasonic	ERJ-3GEY0R00V
28	1	R3	3.30K	RES0603	No	Yageo America	9C06031A3301FKHFT
29	1	R4	470E	RES0603	No	BOURNS	CR0603-FX-4700ELF
30	1	R5	4.75K	RES0603	No	Panasonic	ERJ-3EKF4751V
31	8	R6,R44,R45,R46,R51,R55,R62,R63	10.0K	RES0603	No	Panasonic	ERJ-3EKF1002V
32	1	R7	100E	RES0603	No	Panasonic	ERJ-3EKF1000V
33	1	R9	2.2K	RES0603	No	Panasonic	ERJ-3GEYJ222V
34	1	R10	12.1K	RES0603	No	Rohm	MCR01MZPF1202
35	4	R11,R12,R13,R14	49.9E	RES0603	No	Yageo America	9C06031A49R9FKHFT
38	4	R17,R19,R21,R23	0E	RES0402	No	Panasonic	ERJ-2GE0R00X
39	1	R24	0E	RES1210	No	Vishay	CRCW12100000Z0EA
40	2	R25,R26	330E	RES0603	No	Panasonic	ERJ-3GEYJ331V

TABLE C-1: EVB-LAN9250 EVALUATION BOARD BILL OF MATERIALS (CONTINUED)

Item	Qty	Reference	Part	PCB Footprint	DNP	Manufacturer	Manufacturer Part Number
46	1	R4A	33E	RES0603	No	BOURNS	CR0603-FX-33R0ELF
47	4	R42,R43,R60,R61	2K	RES0603	No	Panasonic	ERJ-3GEYJ202V
51	4	R56,R57,R58,R59	4.7K	RES0603	No	Panasonic	ERJ-3EKF4701V
54	1	SW1	SW-SPDT-SLIDE	sw_ck_1101m2s3cqe2	No	C&K	1101M2S3CQE2
55	1	SW2	sw_pb_2P	sw_pb_2P	No	Panasonic	EVQ-PJU04K
56	1	SW3	SW DIP-4/SM	TH_SW_DIP4	No	Wurth electronics	418117270904
57	1	SW4	219-5MST	SW_DIP_5P-219-5MST	No	CTS Electrocomponents	219-5MST
58	8	SW5,SW6,SW7,SW8,SW9,SW10,SW14,SW15	JS102011CQN	TH_SW_SPST_3P_10x2p5	No	Wurth electronics	450301014042
59	3	SW11,SW12,SW13	JS202011CQN	TH_SW_DPDT_6P	No	C&K	JS202011CQN
60	1	TP1	RED	TH_TP_60D40	No	Keystone	5000
61	1	TP2	ORANGE	TH_TP_60D40	No	Keystone	5003
62	2	TP3,TP4	BLACK	TH_TP_60D40	No	Keystone	5001
64	1	T1	Pulse - J0011D01BNL	th_conn_pulse_rj45_j0026	No	Pulse Electronics	J0011D01BNL
65	1	U1	3_Amp	TH_DC-DC_VERT_5PIN_P67	No	Murata	OKR-T/3-W12-C
66	1	U2	TPS3125	SOT23_5	No	TI	TPS3125L30DBVR
67	1	U3	74LVC1G14	SOT23_5	No	TI	SN74L VCIG14DBVR
68	1	U4	LAN9250	IC_QFN64	No	Microchip	LAN9250
70	1	U5,U6	24FC512	IC_DIP8_300	No	Microchip	24FC512-I/P
71	1	Y1	25.000MHz	XTAL_HCM49	No	Cardinal Components Inc.	CSM1Z-A5B2C5-40-25.0D18-F

TABLE C-2: DNP COMPONENTS

Item	Qty	Reference	Part	PCB Footprint	DNP
1	1	C1	4.7uF	CAP0603	DNP
4	4	C7,C9,C12,C23	1.0uF	CAP0603	DNP
8	4	C28,C29,C30,C31	10pF	CAP0402	DNP
10	8	C33,C34,C35,C36,C38,C40,C42,C45	0.1uF	CAP0603	DNP
11	3	C37,C39,C41	10uF	CAP_B_3528	DNP
14	2	D3,D5	GRN	LED0603	DNP
18	1	J2	FTLF1217P2	CONN_FX_SFP_FT-LF1217P2	DNP
23	2	L1,L2	1uH	L0805	DNP
37	4	R16,R18,R20,R22	0E	RES0402	DNP
41	2	R27,R28	82E	RES0603	DNP

TABLE C-2: DNP COMPONENTS (CONTINUED)

Item	Qty	Reference	Part	PCB Footprint	DNP
42	2	R29,R30	49.9E	RES0603	DNP
43	1	R31	100E	RES0603	DNP
44	2	R32,R33	130E	RES0603	DNP
45	4	R34,R35,R36,R37	4.7K	RES0603	DNP
48	3	R47,R48,R49	1K	RES0603	DNP
49	2	R50,R54	10K	RES0603	DNP
63	1	TP5	SMT	tp-smd40	DNP

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