

**Nuvoton**  
**Advanced Power Control IC**  
**NCT3012S**

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## 1. GENERAL DESCRIPTION

The NCT3012S is Nuvoton's advanced power control IC which is specifically designed for desktop, notebook and any embedded system applications. The NCT3012S provides a mechanism to further lower the total system power consumption while the system is in S5 state. The NCT3012S could block the entire system standby power that comes from the ATX power supplier while the system is in S5 state, and it is fulfilled via the control of the external transistor. The NCT3012S is the only active IC under that circumstance so the total system power consumption is minimized. The system standby power could be resumed by the pushing of the external power button. The NCT3012S is powered by the 5VSB from the ATX power supplier, and communicates with the system through 2-wire System Management Bus (SMBus<sup>TM</sup>) serial interface. The package is 8-pin ESOP green package.

## 2. FEATURES

### 2.1 General Description

- IC Communication Interface: I<sup>2</sup>C® Compatible System Management Bus (SMBus<sup>TM</sup>) Serial Interface
- IC Operation Power Source: 5 Volt VSB Power from ATX Power Supply
- Supports ACPI (Advanced Configuration and Power Interface) Power Sequence
- Supports Programmable Configuration Settings
- Supports Deep S5 Power Saving Control

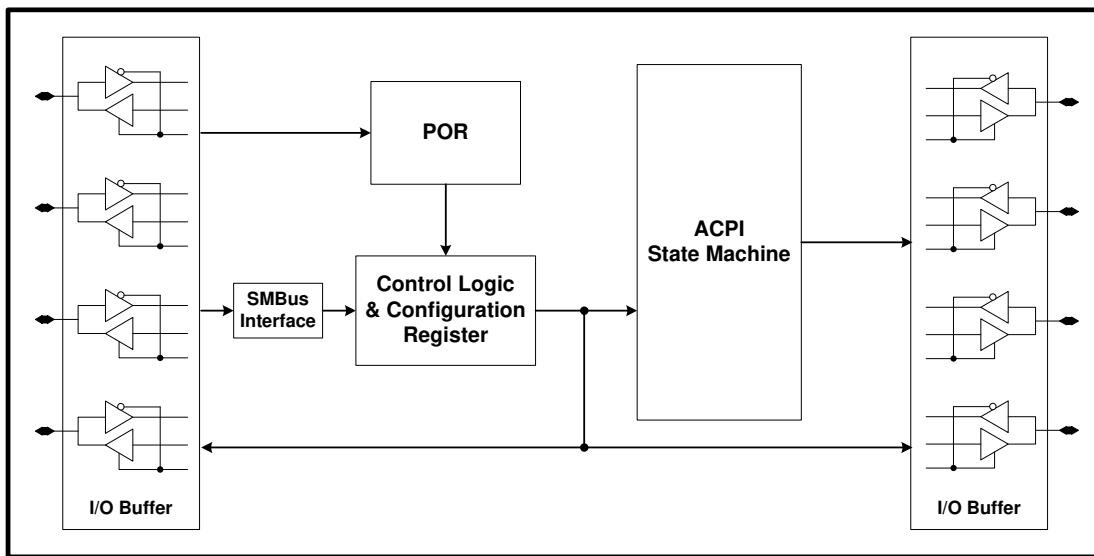
### 2.2 PACKAGE

- SOP-8 150mil with Exposed Pad Package
- Lead Free (ROHS Compliant) and Halogen Free SOP-8

### 2.3 APPLICATION

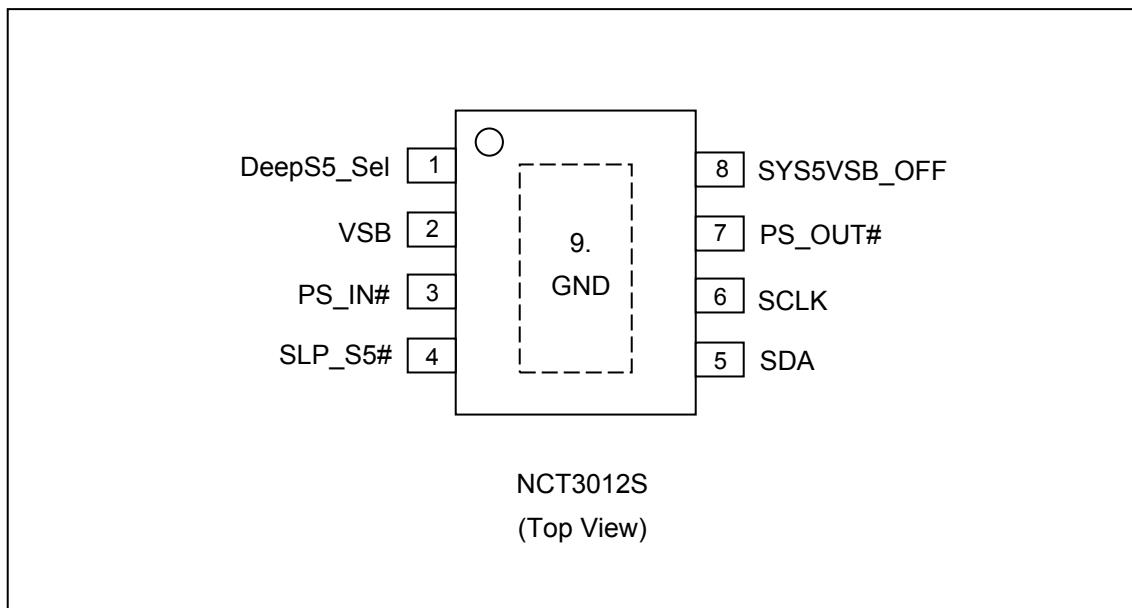
- Desktop and Notebook Computers
- Servers
- Embedded Applications

### 3. BLOCK DIAGRAM



## 4. PIN CONFIGURATION

- NCT3012S PIN CONFIGURATION



## 5. PIN DESCRIPTION

### ● PIN TYPE DESCRIPTION

| PIN TYPE             | PIN ATTRIBUTE  |
|----------------------|--|
| I/OD <sub>12TS</sub> | TTL level and schmitt trigger open drain output with 12 mA sink capability |
| I/O <sub>12TS</sub>  | TTL level and schmitt trigger with 12 mA source and sink capability        |
| I/OD <sub>12</sub>   | Bi-directional pin and open-drain output with 12mA sink capability         |
| OD <sub>12</sub>     | Open-drain output pin with 12 mA sink capability                           |
| IN <sub>TS</sub>     | TTL level input pin and schmitt trigger                                    |
| AIN                  | Input pin (Analog)   |
| AOUT                 | Output pin (Analog)  |
| IN                   | Input pin  |
| OUT                  | Output pin   |
| P                    | Power or Ground Pin  |

### ● NCT3012S PIN DESCRIPTION

| PIN | SYMBOL     | I/O                      | POWER WELL | FUNCTION   |
|-----|------------|--------------------------|------------|--|
| 1   | DeepS5_Sel | Strapping                | VSB        | <p>Function Selection. Strapped by VSB</p> <ul style="list-style-type: none"> <li>● Strapped to <b>high</b> : DeepS5_Sel = 1:<br/>System will enter the deep S5 state after 6 sec delays when AC power on.</li> <li>● Strapped to <b>low</b> : (Default)<br/>DeepS5_Sel = 0:<br/>System will not enter the deep S5 state when AC power on. System is in normal ACPI S5 state.</li> </ul> |
| 2   | VSB        | P                        | VSB        | 5V stand-by power supply for the digital circuits.   |
| 3   | PS_IN#     | IN <sub>TS</sub>         | VSB        | Panel Switch Input. (Support 5V and 3V pull-high.)   |
| 4   | SLP_S5#    | IN <sub>TS</sub>         | VSB        | SLP_S5# input.   |
| 5   | SDA        | I/<br>OD <sub>12TS</sub> | VSB        | SMBus slave bi-directional Data. (5V or 3V)  |

|   |                                 |                          |     |  |
|---|---------------------------------|--------------------------|-----|--|
| 6 | SCLK                            | IN <sub>TS</sub>         | VSB | <b>SMBus Address: 0x6C</b><br>SMBus slave clock. Support 100K (5V or 3V)   |
| 7 | PS_OUT#<br>(DETECT<br>SYS_3VSB) | AIN/<br>OD <sub>12</sub> | VSB | Panel Switch Output. This signal is used to wake-up the system from S3/S5 state.<br>(Detect Level: 2.95V)<br><br>The circuit must use 1KΩ resistor and connect to SYS_3VSB or 3VDual power source for power detection. |
| 8 | SYS5VSB_OFF                     | OD <sub>12</sub>         | VSB | This pin is to control system power for entering deeper power saving mode (Deep S3/ S5 State).   |
| 9 | GND                             | P                        | VSB | Ground.  |

## 6. CONTROL AND STATUS REGISTER

### 6.1 Deep Sleep Enable Control Register (DPSENCTRL)

Location: **Address 00<sub>HEX</sub>**

Type: **Read / Write**

Power Well : **VSB**

Reset: **Power On Reset**

Default Value: **3C<sub>HEX</sub> / 3D<sub>HEX</sub>**

| Bit  | 7        | 6 | 5                  | 4 | 3                | 2 | 1        | 0       |
|------|----------|---|--------------------|---|------------------|---|----------|---------|
| Name | Reserved |   | PSOUT_N_WIDTH[5:4] |   | PSOUT_N_DLY[3:2] |   | Reserved | DpS5_En |

| Bit | Description   |
|-----|---|
| 7-6 | <b>Reserved, don't change the default value</b>   |
| 5-4 | <b>Deep sleep wake-up PS_OUT# pulse width:</b><br>When system wake up from deep sleep mode, system will occur a low pulse via PS_OUT#.:<br>00: Don't occur low pulse<br>01: Pulse Width 32ms<br>10: Pulse Width 64ms<br>11: Pulse Width 160ms (default)                                 |
| 3-2 | <b>Deep sleep wake-up PS_OUT# delay time :</b><br>When system wake up from deep sleep mode, system will occur a low pulse via PS_OUT# after SYS_3VSB ready and wait a delay time..<br>00: Delay 5ms<br>01: Delay 20ms<br>10: Delay 80ms<br>11: Delay 160ms (default)                    |
| 1   | <b>Reserved, don't change the default value</b>   |
| 0   | <b>Deep S5 Enable :</b><br><b>Default value was determined by pin1 power on strapping.</b><br><b>Strapping to High, the default value of the bit is set to "1".</b><br><b>Strapping to Low, the default value of this bit is set to "0".</b><br>0: Disable Deep S5<br>1: Enable Deep S5 |

## 6.2 Deep S5 Delay Time Control (DELAYCTRL)

Location: **Address 15<sub>HEX</sub>**  
 Type: **Read / Write**  
 Power Well : **VSB**  
 Reset: **Power On Reset**  
 Default Value: **00<sub>HEX</sub> / 02<sub>HEX</sub>**

| Bit  | 7        | 6        | 5        | 4        | 3                        | 2 | 1 | 0 |
|------|----------|----------|----------|----------|--------------------------|---|---|---|
| Name | Reserved | Reserved | Reserved | Reserved | Delay_Time_Control [1:0] |   |   |   |

| Bit | Description   |
|-----|---|
| 7-2 | Reserved  |
| 1-0 | <b>Delay_Time_Control:</b> Delay (0 / 3 / 6 / 10) seconds to enter deep S5 state<br><b>Default value was determined by pin1 power on strapping.</b><br><b>Strapping to High, the default value of these two bits is set to “10” (6 seconds).</b><br><b>Strapping to Low, the default value of these two bits is set to “00” (0 second).</b><br>00: 0 second;<br>01: 3 seconds;<br>10: 6 seconds;<br>11: 10 seconds. |

## 6.3 Chip and Version ID Register (CVID)

Location: **Address 20<sub>HEX</sub>**  
 Type: **Read Only**  
 Power Well : **VSB**  
 Reset: **Power On Reset**  
 Default Value: **88<sub>HEX</sub>**

| Bit  | 7            | 6 | 5 | 4 | 3 | 2 | 1           | 0 |
|------|--------------|---|---|---|---|---|-------------|---|
| Name | Chip_ID[4:0] |   |   |   |   |   | Ver_ID[2:0] |   |

| Bit | Description                            |
|-----|--|
| 7-3 | <b>Chip ID :</b><br>10001 (default)    |
| 2-0 | <b>Version ID :</b><br>000 : (default) |

## 7. ELECTRICAL CHARACTERISTIC

### 7.1 ABSOLUTE MAXIMUM RATINGS

| PARAMETER                  | RATING          | UNIT |
|----------------------------|-----------------|------|
| Power Supply Voltage (VSB) | -0.3 ~ 6.0      | V    |
| Input Voltage              | -0.3 to VSB+0.3 | V    |
| Operating Temperature      | 0 to +70        | °C   |
| Storage Temperature        | -50 to +150     | °C   |

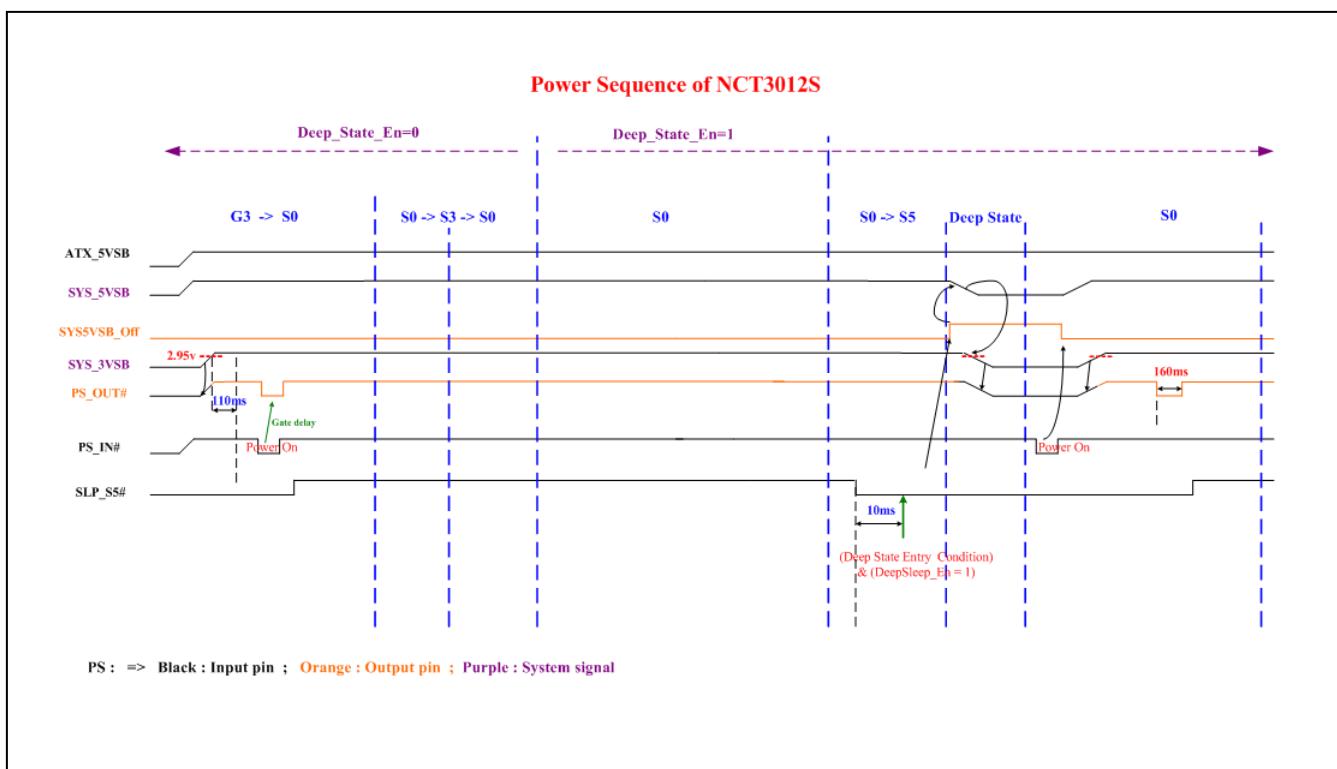
Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

### 7.2 DC CHARACTERISTICS

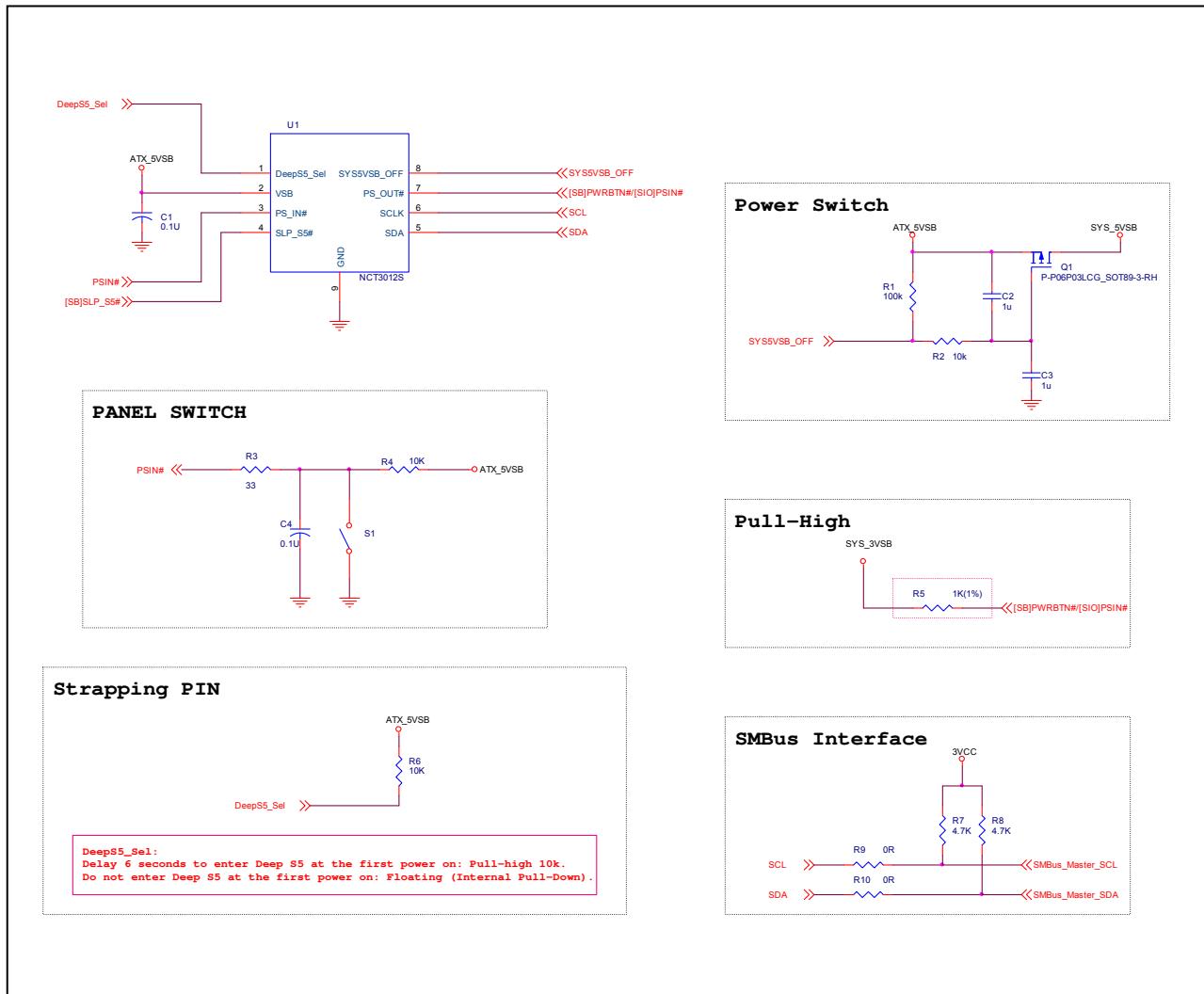
| PARAMETER   | SYM              | MIN | TYP  | MAX. | UNIT | CONDITIONS               |
|---|------------------|-----|------|------|------|--------------------------|
| <b>Supply Input Voltage</b>   |                  |     |      |      |      |                          |
| VSB Input Voltage   | VSB              |     |      | 5.5  | V    |                          |
| <b>Supply Input Current</b>   |                  |     |      |      |      |                          |
| VSB Input Current   | I <sub>VSB</sub> |     | 2    | 5    | mA   |                          |
| <b>I/O<sub>D12TS</sub> –TTL level and Schmitt trigger open-drain output with 12mA sink capability</b> |                  |     |      |      |      |                          |
| Input Low Threshold Voltage   | V <sub>t-</sub>  |     |      | 0.85 | V    |                          |
| Input High Threshold Voltage  | V <sub>t+</sub>  | 2.2 |      |      | V    |                          |
| Hysteresis  | V <sub>TH</sub>  |     | 1.25 |      |      |                          |
| Output Low Voltage  | V <sub>OL</sub>  |     |      | 0.4  | V    | I <sub>OL</sub> = 12 mA  |
| Input High Leakage  | I <sub>LIH</sub> |     |      | +10  | µA   |                          |
| Input Low Leakage   | I <sub>LIL</sub> |     |      | -10  | µA   |                          |
| <b>OUT – 3.3V output pin with 12mA source and sink capability</b>                                     |                  |     |      |      |      |                          |
| Output Low Voltage  | V <sub>OL</sub>  |     |      | 0.4  | V    | I <sub>OL</sub> = 12 mA  |
| Output High Voltage   | V <sub>OH</sub>  | 2.4 |      |      | V    | I <sub>OH</sub> = -12 mA |
| <b>OD<sub>12</sub> – Open-drain output pin with 12mA sink capability</b>                              |                  |     |      |      |      |                          |
| Output Low Voltage  | V <sub>OL</sub>  |     |      | 0.4  | V    | I <sub>OL</sub> = 12 mA  |
| <b>IN – TTL-level input pin</b>   |                  |     |      |      |      |                          |
| Input Low Voltage   | V <sub>IL</sub>  |     |      | 0.8  | V    |                          |
| Input High Voltage  | V <sub>IH</sub>  | 2.0 |      |      | V    |                          |
| Input High Leakage  | I <sub>LIH</sub> |     |      | +10  | µA   |                          |
| Input Low Leakage   | I <sub>LIL</sub> |     |      | -10  | µA   |                          |

| PARAMETER   | SYM              | MIN | TYP  | MAX. | UNIT | CONDITIONS |
|---|------------------|-----|------|------|------|------------|
| <b>IN<sub>TS</sub> – TTL-level, Schmitt-trigger input pin</b> |                  |     |      |      |      |            |
| Input Low Threshold Voltage                                   | V <sub>t-</sub>  |     |      | 0.85 | V    |            |
| Input High Threshold Voltage                                  | V <sub>t+</sub>  | 2.2 |      |      | V    |            |
| Hysteresis  | V <sub>TH</sub>  |     | 1.25 |      | V    |            |
| Input High Leakage  | I <sub>LH</sub>  |     |      | +10  | μA   |            |
| Input Low Leakage   | I <sub>LIL</sub> |     |      | -10  | μA   |            |

### 7.3 AC CHARACTERISTICS

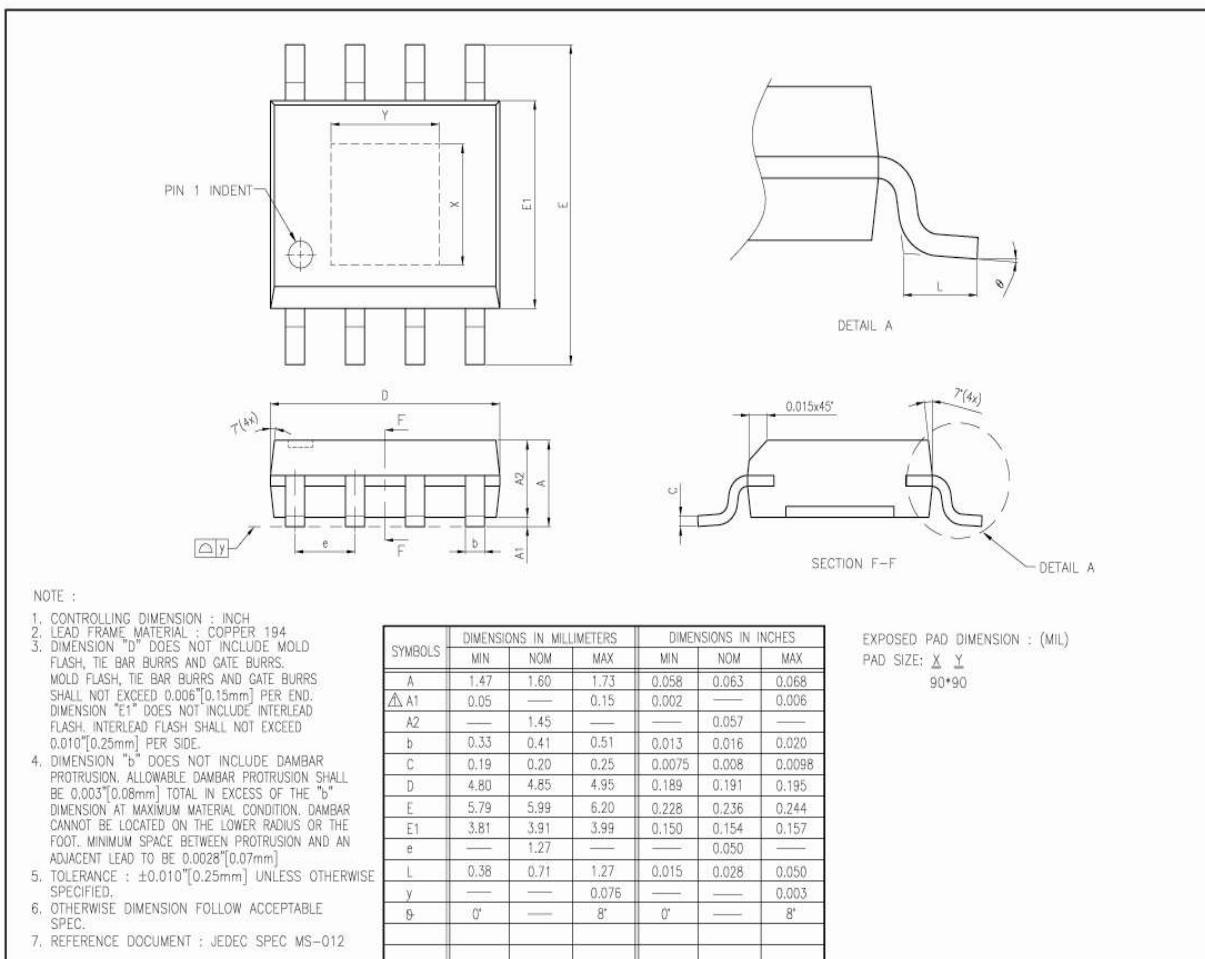


## 8. TYPICAL APPLICATION REFERENCE CIRCUIT

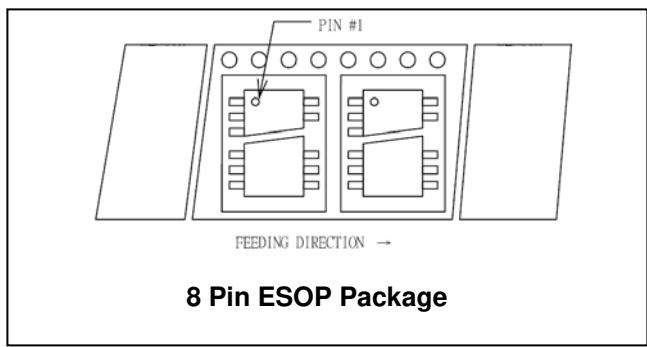


## 9. PACKAGE SPECIFICATIONS

### ESOP-8 (150mil) PKG Outline



### 9.1 Taping Specification



## 10. Ordering Information

| PART NUMBER | PACKAGE TYPE              | SUPPLIED AS      | PRODUCTION FLOW          |
|-------------|---------------------------|------------------|--------------------------|
| NCT3012S    | 8PIN ESOP (Green package) | 2,500 units/ T&R | Commercial, 0°C to +70°C |

## 11. TOP MARKING SPECIFICATIONS



1<sup>st</sup> line: nuvoton – company name  
2<sup>nd</sup> line: 3012S – the part number  
3<sup>rd</sup> line: Tracking code 922 A X  
922: Packages assembled in Year 09', week 22  
A: Assembly house ID  
X: The IC version (A means A; B means B...etc)

## 12. REVISION HISTORY

| VERSION | DATE       | PAGE | DESCRIPTION         |
|---------|------------|------|---------------------|
| A0      | 07/10/2009 | ALL  | Preliminary Release |
|         |            |      |                     |
|         |            |      |                     |

### Important Notice

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**Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.**

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