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PowerQUICC™ MPC8308_RDB User's Guide

The MPC8308_RDB is a system featuring the PowerQUICC™ processor, MPC8308. This low-cost, high-performance system solution consists of a printed circuit board (PCB) assembly plus a software board support package (BSP) distributed in a CD image. This BSP enables the fastest possible time-to-market for development or integration of applications including printer engines, broadband gateways, no-new-wires home adapters/access points, and home automation boxes.

This document describes the hardware features of the board including specifications, block diagram, connectors, interfaces, and hardware straps. It also describes the board settings and physical connections needed to boot the MPC8308_RDB. Finally, it considers the software shipped with the platform.

When you finish reading this document, you should:

- be familiar with the board layout
- understand the default board configuration and your board configuration options
- know how to get started and boot the board
- know about the software and further documentation that supports the board

Contents

WARNING

This is a class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

Use this manual in conjunction with the following documents:

- *MPC8308 PowerQUICC™ II Pro Integrated Communications Processor Family Reference Manual* (MPC8308RM)
- *MPC8308 PowerQUICC II Pro Processor Hardware Specifications* (MPC8308EC)
- *Hardware and Layout Design Considerations for DDR Memory Interfaces* (AN2582)

NOTE

The normal function of the product may be disturbed by strong electromagnetic interference. If so, simply reset the product to resume normal operation by following the instructions in the manual. If normal function does not resume, use the product in another location.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his/her own expense.

1 MPC8308_RDB Hardware

This section covers the features, block diagram, specifications, and mechanical data of the MPC8308_RDB.

1.1 Features

- CPU: Freescale MPC8308 running at 400/133 MHz; CPU/coherent system bus (CSB)
- Memory subsystem:
  - 128 MByte unbuffered DDR2 SDRAM discrete devices
  - 8 MByte NOR flash single-chip memory
  - 32 MByte NAND flash memory
  - 256 Kbit M24256 serial EEPROM
- Interfaces:
  - 10/100/1000 BaseT Ethernet ports:
    - eTSEC1, RGMII: one 10/100/1000 BaseT RJ-45 interface using Realtek™ RTL8211B single port 10/100/1000 BaseT PHY
    - eTSEC2, RGMII: five 10/100/1000 BaseT RJ-45 interfaces using Vitesse™ VSC7385 5-port L2 Gigabit Ethernet switch
  - USB 2.0 port:
    - High-speed host/device/OTG USB interface using external ULPI PHY interface by SMSC USB3300 USB PHY
  - PCI Express:
    - One mini PCI Express connector supporting half and full size mini PCI Express card
  - eSDHC port:
    - One SD card connector
  - Dual UART ports:
    - DUART interface: supports two UARTs up to 115200 bps for console display
  - I2C
    - I2C connected to Dallas™ DS1339 RTC with battery holder and Atmel™ AT24C08 Serial EEPROM
- Freescale MC9S08QG8 MCU (20-MHz HCS08 CPU) for fan control and soft start
  - Support for Low Power / Wake on LAN. This can be MCU controlled or logic
- Board Connectors:
  - 4 pins Power Jack connector
  - Dual RS-232C connectors
  - JTAG / COP for debugging
  - IEEE® Std. 1588™ signals for test and measurement
  - 8 pins SPI header for future expansion
- Form factor:

— Mini-ITX form factor (170 mm x 170 mm, or 6693 mils x 6693 mils)

- 6-layer PCB (4-layer signals, 2-layer power and ground) routing
- Certification
  — CE (Class A) / FCC (Class A)
- Lead-Free (RoHS)

Figure 1 shows the MPC8308_RDB block diagram.

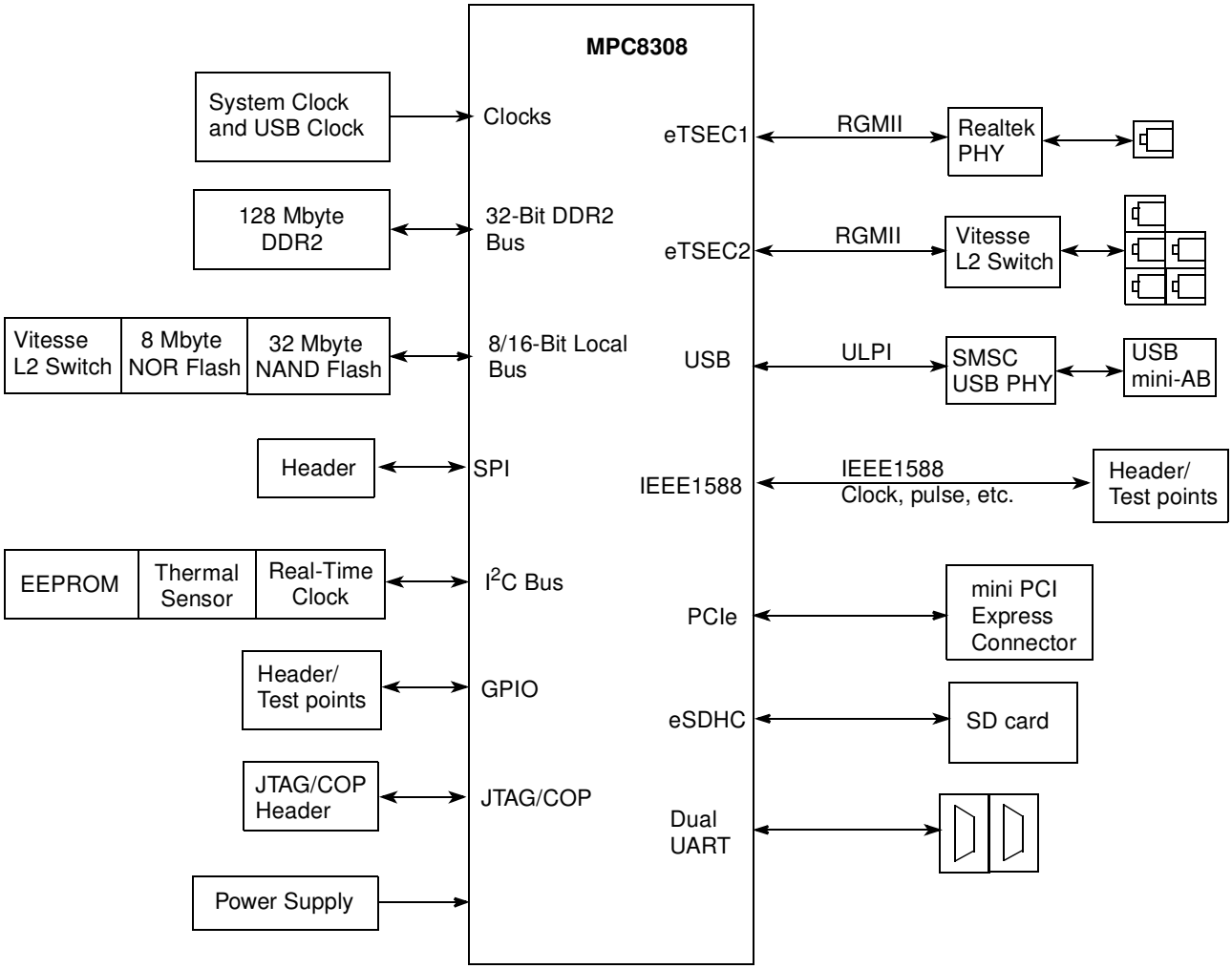

Figure 1. MPC8308_RDB Block Diagram

1.2 Specifications

Table 1 lists the specifications of the MPC8308_RDB.

Table 1. MPC8308_RDB Specifications

Characteristics	Specifications
Power requirements (without add-on card):	**Typical** **Maximum** 12 V DC 0.5 A 5.0 V DC 1.5 A
Communication processor	MPC8308 running @ 400 MHz
Addressing: Total address range Flash memory (local bus) DDR2 SDRAM	4 Gbyte (32 address lines) 8 Mbyte with one chip-select 128 Mbyte DDR2 SDRAM
Operating temperature	0^{o} C to 70^{o} C
Storage temperature	–25^{o}C to 85^{o}C
Relative humidity	5% to 90% (noncondensing)
PCB dimensions: Length Width Thickness	 6693 mil 6693 mil 62 mil

1.3 Mechanical Data

Figure 2 shows the MPC8308_RDB dimensions (in mil and [mm]). The board measures 170 mm × 170 mm (6693 mil × 6693 mil) for integration in a mini-ITX chassis.

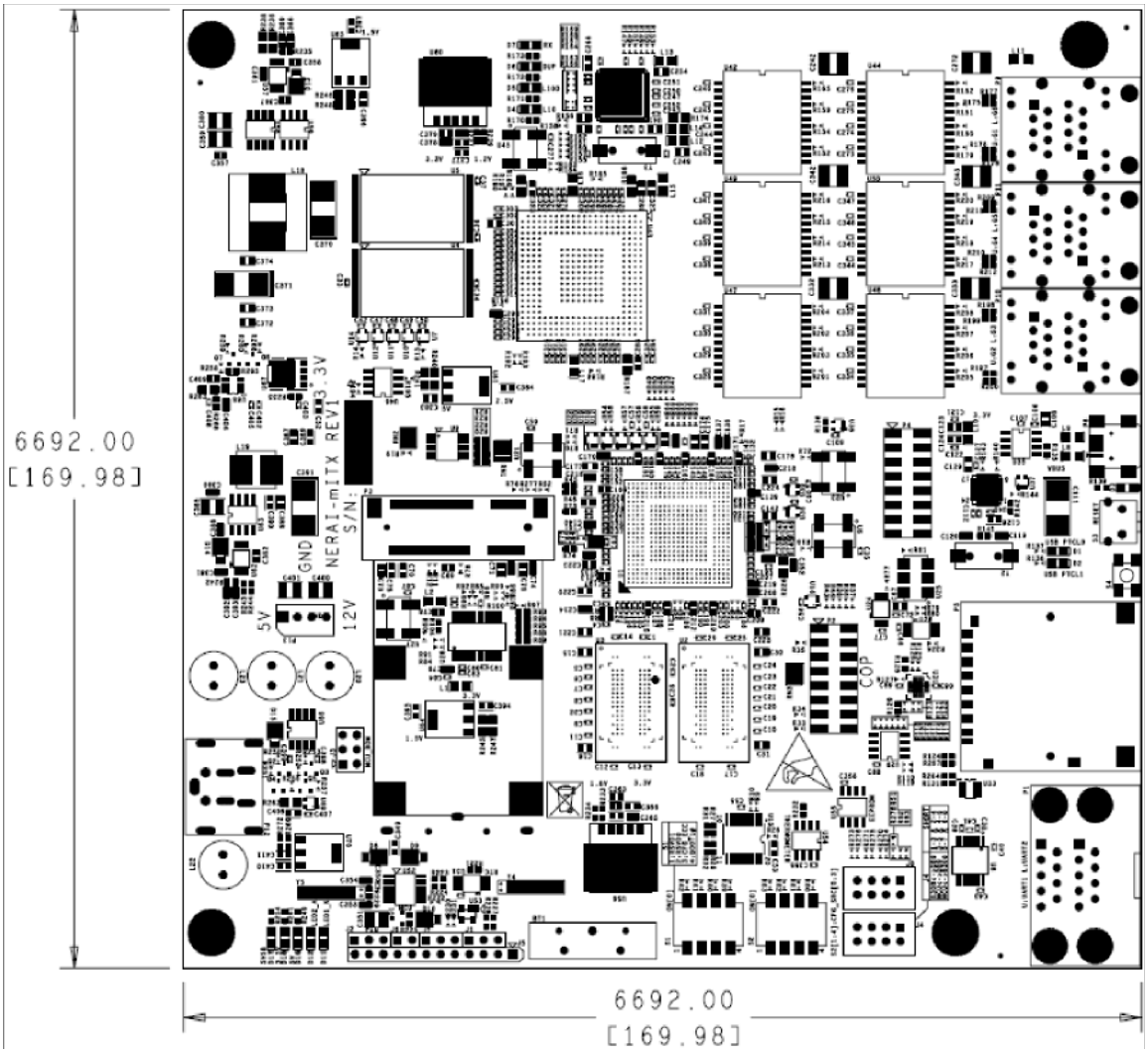

Figure 2. Dimensions of the MPC8308_RDB

2 Board-Level Functions

The board-level functions includes reset, external interrupts, clock distribution, DDR SDRAM controller, local bus controller, I^2C interfaces, SD memory card interface, USB interface, eTSEC1 and eTSEC2 10/100/1000 BaseT interface, dual RS-232 ports, PCI Express, and COP/JTAG.

2.1 Reset and Reset Configurations

The MPC8308_RDB reset module generates a single reset to the MPC8308 and other peripherals on the board. The reset unit provides power-on reset, hard reset, and soft reset signals in compliance with the MPC8308 hardware specification. Figure 3 shows the reset circuitry. Notice the following:

- $\overline{\text{PORESET}}$ (Power-on reset) is generated by the Micrel MIC811 device. When $\overline{\text{MR}}$ is deasserted and 3.3 V is ready, the MIC811 internal timeout guarantees a minimum reset active time of 150 ms before $\overline{\text{PORESET}}$ is deasserted. This circuitry guarantees a 150 ms $\overline{\text{PORESET}}$ pulse width after 3.3 V reaches the right voltage level, and this meets the specification of the $\overline{\text{PORESET}}$ input of MPC8308. Push button reset interfaces the $\overline{\text{MR}}$ signal with debounce capability to produce a manual master $\overline{\text{PORESET}}$
- $\overline{\text{PORESET}}$ (Power-on reset) is optionally generated by the MC9S08 MCU device by monitoring the 3.3V voltage level
- $\overline{\text{HRESET}}$ (Hard reset) is generated either by the MPC8308 or the COP/JTAG port.
- COP/JTAG port reset provides convenient hard-reset capability for a COP/JTAG controller. The $\overline{\text{HRESET}}$ line is available at the COP/JTAG port connector. The COP/JTAG controller can directly generate the hard-reset signal by asserting this line low. The arrangement shown in Figure 3 allows the COP to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the MPC8308 can drive $\overline{\text{HRESET}}$ as well.

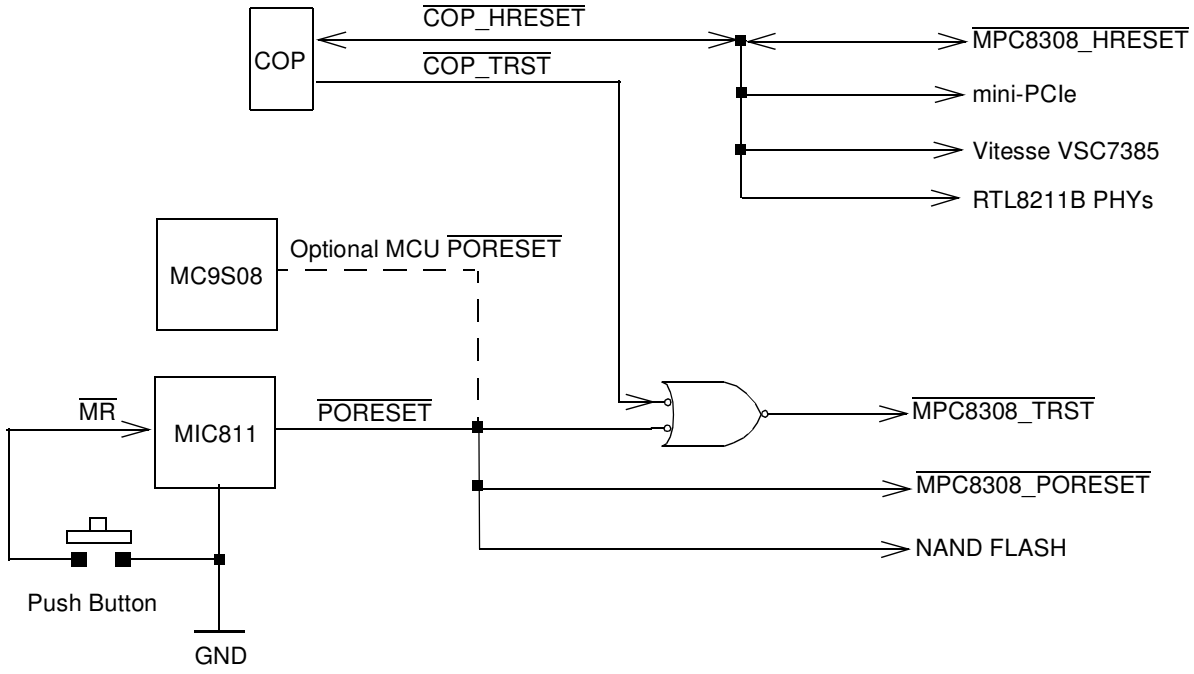

Figure 3. Reset Circuitry of the MPC8308

2.2 External Interrupts

Figure 4 shows the external interrupt circuitry to the MPC8308.

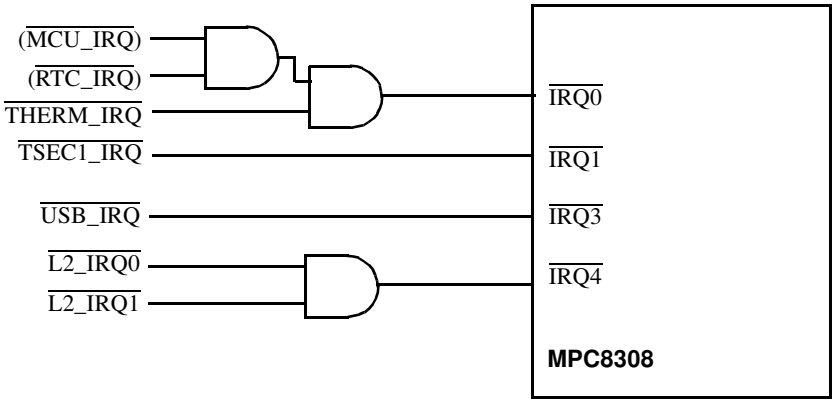

Figure 4. MPC8308 Interrupt Circuitry

Following are descriptions of the interrupt signals shown in Figure 4:

- All external interrupt signals are pulled up by 4.7 K resistors.
- MCU interrupt ($\overline{\text{MCU\_IRQ}}$), RTC interrupt ($\overline{\text{RTC\_IRQ}}$) and Thermal interrupt ($\overline{\text{THERM\_IRQ}}$). The MCU and DS1339 RTC interrupts are ANDed the thermal interrupt. However, MCU interrupt is the main function for this IRQ pin. RTC and thermal interrupt are optional so they are disconnected from the AND gate by default.
- PHY interrupt ($\overline{\text{TSEC1\_IRQ}}$). The RTL8211B GBE PHY interrupt is connected to $\overline{\text{IRQ1}}$ of the MPC8308. Therefore, the system software can detect the status of the Ethernet link and the PHY internal status.
- USB over current ($\overline{\text{USB\_IRQ}}$). The USB power supply have an over current detection circuit and generate an interrupt when the current limit reaches (2A) or a thermal shutdown or under voltage lockout (UVLO) condition occurs. It is connected to $\overline{\text{IRQ3}}$ of the MPC8308.
- L2 Switch (VSC7385) interrupt ($\overline{\text{L2\_IRQ1}}$, $\overline{\text{L2\_IRQ0}}$). The L2 Switch (VSC7385) has two IRQs that are ANDed together to generate an interrupt to the MPC8308E via the $\overline{\text{IRQ4}}$ signal.

2.3 Clock Distribution

Figure 5 and Table 2 show the clock distribution on the MPC8308_RDB.

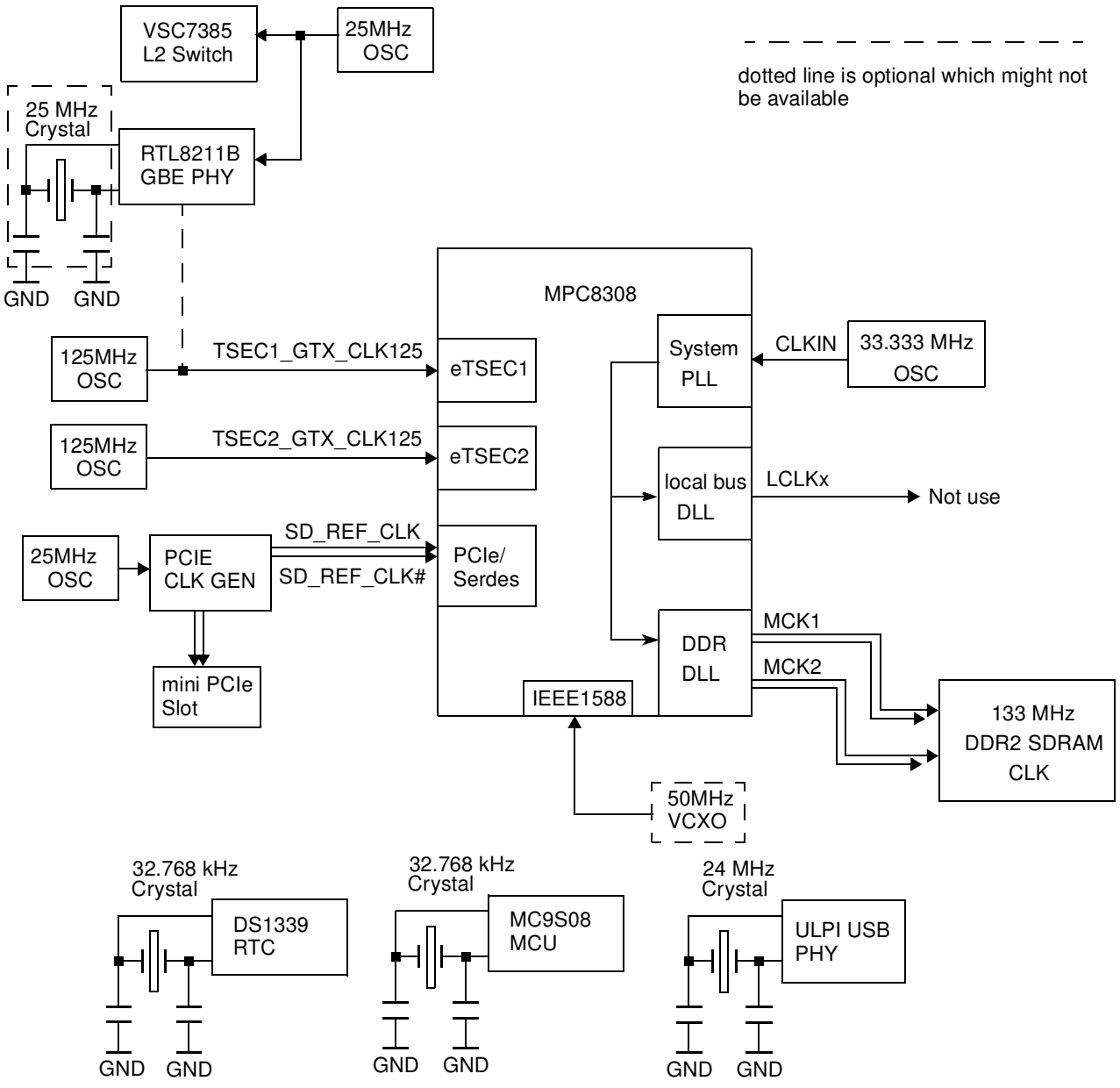

Figure 5. MPC8308_RDB Clock Scheme

Table 2. Clock Distribution

Clock Frequency	Module	Generated by	Description
33.333 MHz	MPC8308 CLKIN	33.333 MHz oscillator	The MPC8308 uses CLKIN to generate the internal system PLL. The CSB clock is generated by the internal PLL and is fed to the e300 core PLL for generating the e300 core clock.
133 MHz	DDR2 SDRAM	MPC8308	The DDR memory controller is configured to use the 2:1 mode CSB to DDR for the DDR interface (DDR266). The local bus clock uses 1:1 local to CSB clock, which is configured by hard reset configuration or SPMR register.
25 MHz	L2 Switch and GBE PHY	25 MHz oscillator	The 25 MHz oscillator provides the clock for the L2 switch and the GBE PHY
125 MHz	eTSEC1 clock	125 MHz oscillator (default) or RTL8211B (optional)	The eTSEC1 reference clock is provided by a125MHz oscillator or optionally by the gigabit Ethernet PHY (RTL8211B) on the board.
125 MHz	eTSEC2 clock	125 MHz oscillator	The eTSEC2 reference clock is provided by a 125MHz oscillator.
100 MHz	PCIe/SERDES	PCIe Clock Generator	The PCIe Clock Generator provides differential clock for PCIe/SERDES module and the PCIe & mini PCIe slots
50 MHz	IEEE1588 Clock (TMR_CLK)	50 MHz oscillator/ 50 MHz VCXO	50 MHz is used by the IEEE 1588 module. It can be an ordinary oscillator or VCXO controlled by SPI DAC.
24 MHz	ULPI external USB PHY	24 MHz crystal	Clock for ULPI USB PHY USB3300
32.768kHz	MCU MC9S08	32.768kHz Crystal	Clock for MCU
32.768kHz	RTC DS1339	32.768kHz Crystal	Clock for RTC

2.4 DDR2 SDRAM Controller

The MPC8308 processor uses DDR2 SDRAM as the system memory. The DDR2 interface uses the SSTL2 driver/receiver and 1.8 V power. A Vref 1.8 V /2 is needed for all SSTL2 receivers in the DDR2 interface. For details on DDR2 timing design and termination, refer to the Freescale application note entitled *Hardware and Layout Design Considerations for DDR Memory Interfaces* (AN2582). Signal integrity test results show this design does not require terminating resistors (series resistor (R_S) and termination resistor (R_T)) for the discrete DDR2 devices used. DDR2 supports on-die termination; the DDR2 chips and MPC8308 are connected directly. The interface is 1.8 V provided by an on-board voltage regulator. VREF, which is half the interface voltage, that is, 0.9 V, is provided by a voltage divider of the 1.8 V for voltage tracking and low cost. One pair of clock pins is provided by the MPC8308, and they are connected and shared by the two DDR2 devices. Figure 6 shows the DDR2 SDRAM controller connection.

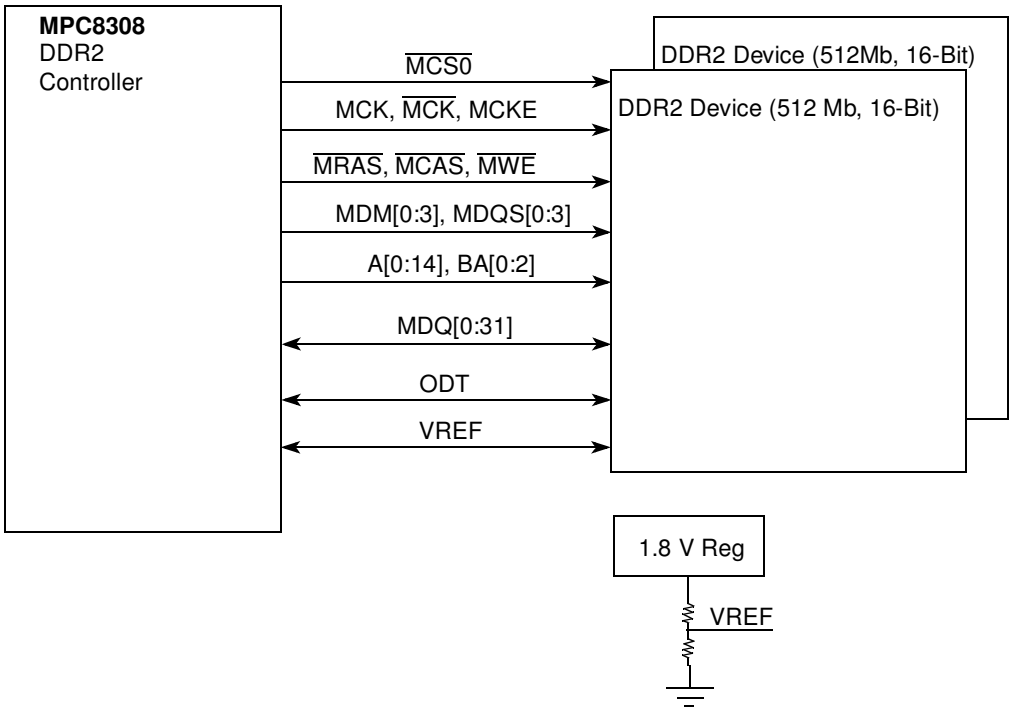

Figure 6. DDR2 SDRAM Connection

2.5 Local Bus Controller

The MPC8308 local bus controller has a 16-bit LD[0:15] data and 26-bit LA[0:25] address bus and control signals. The non multiplexed bus provides an easy and direct way to interface with other standard memory device. The followings modules are connected to the local bus of MPC8308:

- 8 MByte NOR flash memory
- 32 MByte NAND flash memory
- GBE L2 switch (VSC7385) parallel interface (PI)

2.5.1 NOR Flash Memory

Through the general-purpose chip-select machine (GPCM), the MPC8308_RDB provides 8 Mbyte of flash memory using a chip-select signal. The flash memory is used with the 16-bit port size. Figure 7 shows the hardware connections for the flash memory.

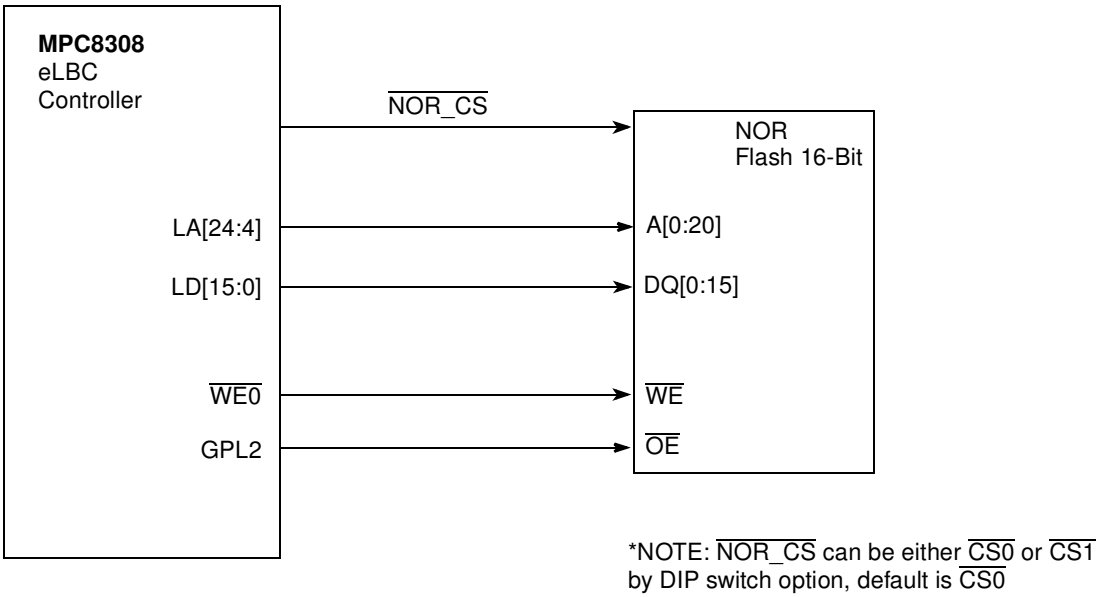

Figure 7. NOR Flash Connection

2.5.2 NAND Flash Memory

The MPC8308 has native support for NAND flash memory through its NAND flash control machine (FCM). The MPC8308_RDB implements an 8-bit NAND flash with 32 MByte in size. Figure 8 shows the NAND flash connection.

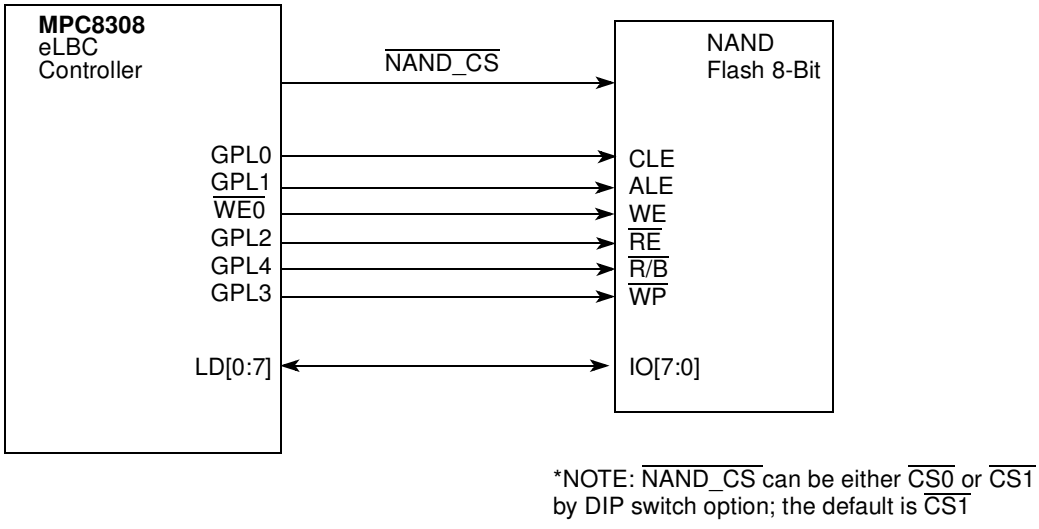

Figure 8. NAND Flash Connection

2.5.3 VSC7385 Parallel Interface

Figure 9 shows the local bus connection to the Vitesse VSC7385 parallel interface.

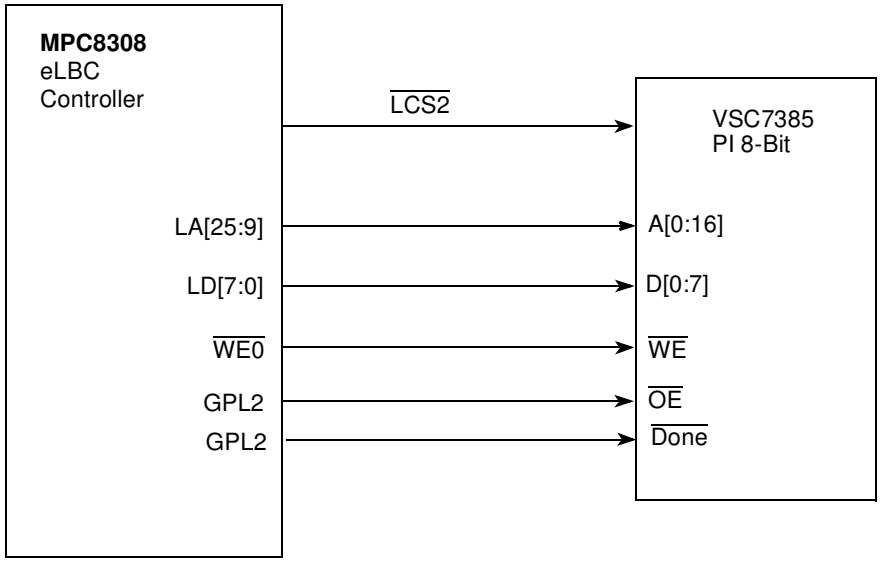

Figure 9. VSC7385 Parallel Interface connection

2.6 I²C Interfaces

The MPC8308 has two I²C interfaces. On the MPC8308_RDB, I²C1 is used as master mode and it is connected to following devices.

- MCU MC9S08QG8 at address 0x0A.
- Optional DAC AD5301 at address 0x0C.
- PCF8574 I²C expander at address 0x39.
- Thermal sensor LM75 at address 0x48.
- Serial EEPROM M24256 at address 0x50.
- Real-time clock DS1339U at address 0x68.

The M24256 serial EEPROM can be used to store the reset configuration word of the MPC8308, as well as to store the configuration registers values and user program if the MPC8308 boot sequencer is enabled. By default, the EEPROM is not used and the hard reset configuration words are loaded from local bus flash memory. For details on how to program the reset configuration word value in I²C EEPROM and the boot sequencer mode, refer to the MPC8308 reference manual.

There is a PCF8574A I²C I/O expander on the MPC8308_RDB board to provide general purpose I/O expansion via the I2C1 interface. The PCF8574A has I2C1 address 0x39 and it is able to detect the board revision number, which flash is currently used to boot and two reserved bit for future expansion. The bit definition of the PCF8574A is defined as in Table 3:

I²C2 is connected to the clock generator ICS9FG104 and mini PCI-E socket.

Table 3. PCF8574A Bit Descriptions

PCF8574A (U10) bit[0..7]	Name	Read/Write	Description
0	REV1	Read only, write has no effect	Board revision number REV[0:1] definition 00: revision 1.0 01: reserved 10: reserved 11: reserved
1	REV0		
2	RSVD1	Read only, write has no effect	Reserved for future use
3	RSVD0	Read only, write has no effect	Reserved for future use
4	BOOT0	Read only, write has no effect	Used to determine which flash is used for boot flash 0: NOR Flash is the boot flash 1: NAND Flash is the boot flash
5	Not used	—	—
6	Not used	—	—
7	Not used	—	—

2.7 SD Memory Card Interface

SD memory card interface is connected to the eSDHC interface of the MPC8308. Figure 10 shows the hardware connection.

CAUTION

Power down before inserting or removing the SD memory card.

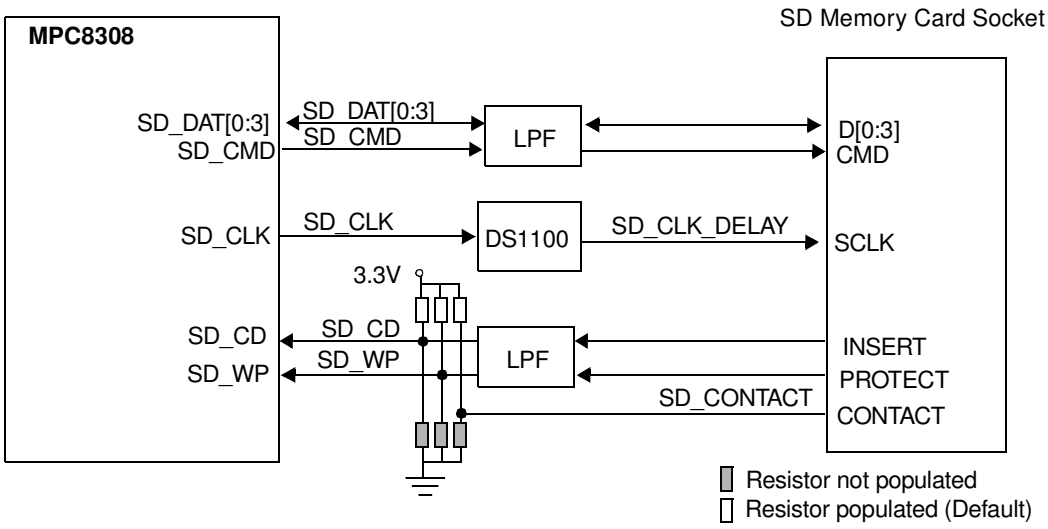

Figure 10. SD Memory Card Connection

2.8 USB Interface

MPC8308 supports a USB 2.0 high speed host/device/OTG interface through external ULPI USB PHY. The USB connection on MPC8308_RDB is shown in Figure 11.

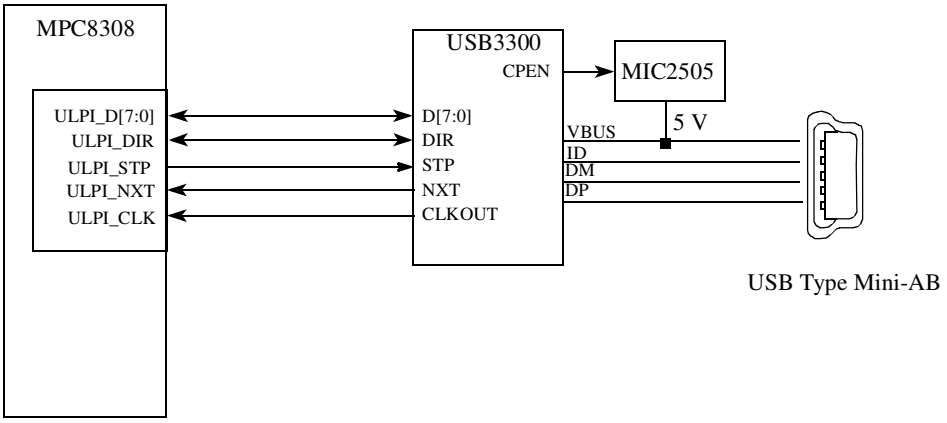

Figure 11. USB Connections

2.9 eTSEC 10/100/1000 BaseT Interface

On the MPC8308_RDB_RDB board, RGMII mode is used on both eTSEC1 and eTSEC2, which are connected to the on-board 10/100/1000 PHY (RTL8211B) and the 5-port GBE switch (VSC7385) respectively. The I/O voltage is set to 3.3 V RGMII for RTL8211B and 2.5V RGMII for VSC7385. The RGMII (1000 BaseT) is a source synchronous bus. For a transmit bus connection, it is synchronous to GTX_CLK from the eTSEC module. The receive bus connection is synchronous to RX_CLK generated

from the PHY device. The MPC8308 MII management interface is connected to the RTL8211B only. Figure 12 shows the connection between the MPC8308 eTSEC1 to the RTL8211B and eTSEC2 to the VSC7385.

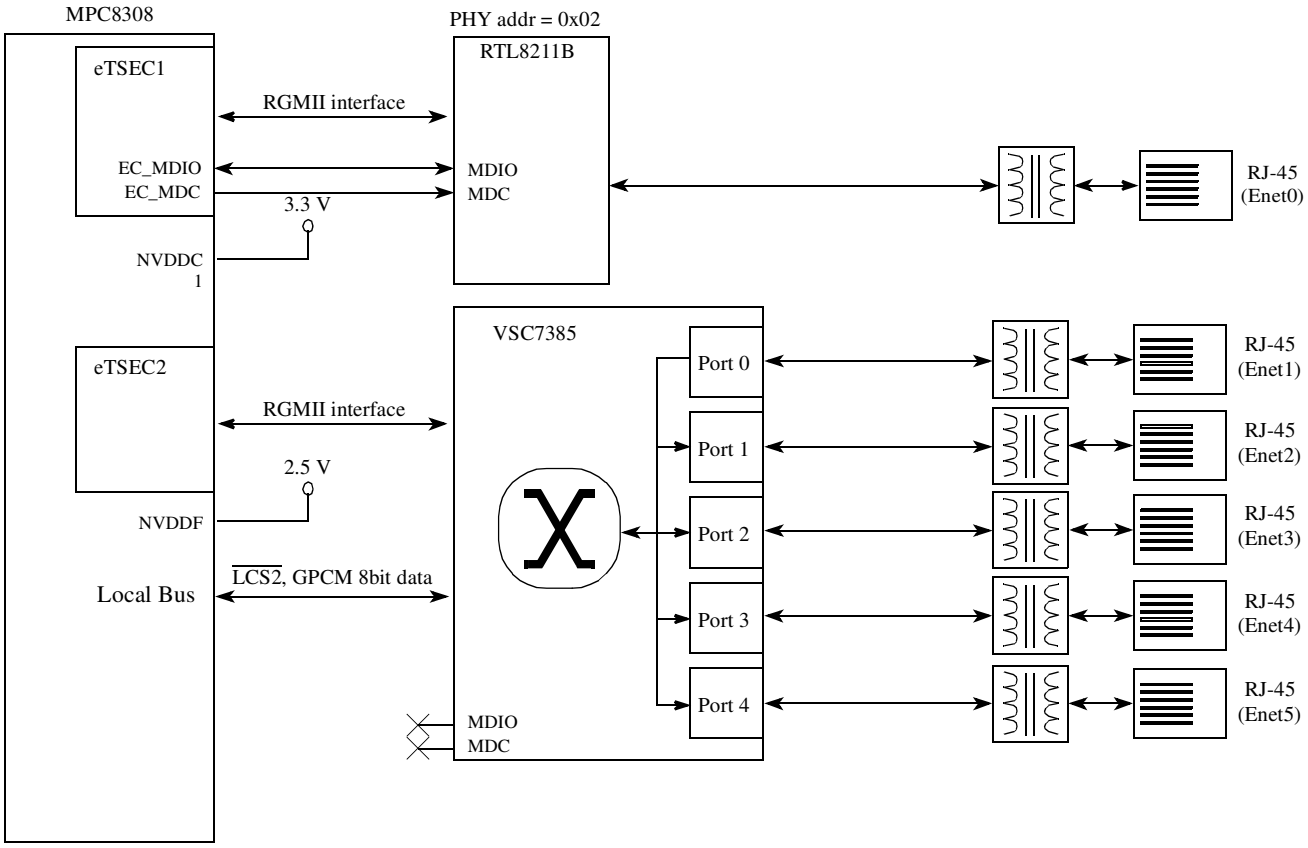

Figure 12. eTSEC Interface Connection

2.10 Dual RS-232 Ports

Dual RS-232 ports are supported on the board. Figure 13 illustrates the serial port connection using a MAX3232 3.3V RS-232 driver to interface with a 9-pin D type female connector. This serial connection runs at up to 115.2 Kbps.

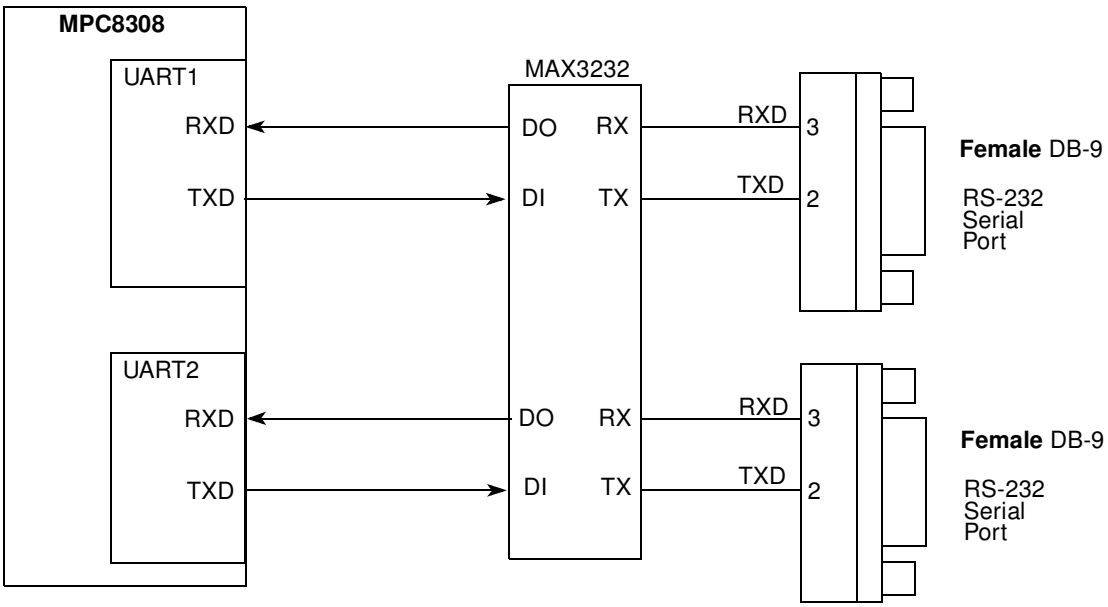

Figure 13. RS-232 Debug Ports Connection

2.11 COP/JTAG Port

The common on-chip processor (COP) is part of the MPC8308 JTAG module and is implemented as a set of additional instructions and logic. This port can connect to a dedicated emulator for extensive system debugging. Several third-party emulators in the market can connect to the host computer through the Ethernet port, USB port, parallel port, RS-232, and so on. A typical setup using a USB port emulator is shown in Figure 14.

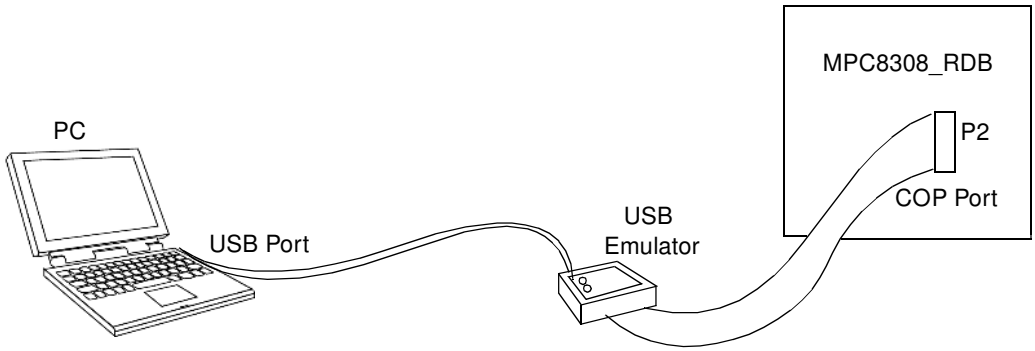

Figure 14. Connecting MPC8308_RDB to a USB Emulator

The 16-pin generic header connector carries the COP/JTAG signals and the additional signals for system debugging. The pinout of this connector is shown in Figure 15.

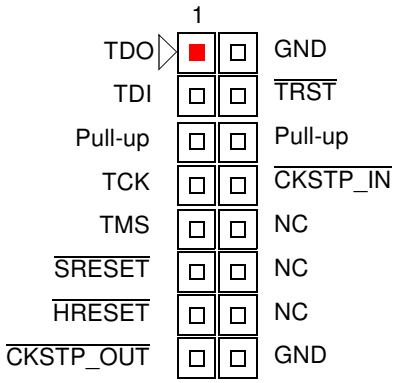

Figure 15. MPC8308_RDB COP Connector

3 Connectors, Jumpers, Switches, and LEDs

Table 4 summarizes the connectors, jumpers, switches, and LEDs on the MPC8308_RDB, and it provides the number of the section/page on which each is discussed. The rest of this section discusses each of these in the order of its appearance in the table.

Table 4. Connectors, Headers, Jumpers, Switches, and LEDs

Reference	Description
Connectors	
P1	Dual UART connector. UART1 (top), UART2 (bottom)
P2	16-pin COP/JTAG connector
P3	miniPCI Express connector
P4	IEEE 1588 connector (Optional)
P5	SD memory card socket
P8	USB mini-AB Connector (external ULPI USB PHY)
P9	RJ-45 LAN connectors Enet4 (top), Enet5 (bottom)
P10	RJ-45 LAN connectors Enet2 (top), Enet3 (bottom).
P11	RJ-45 LAN connectors Enet0 (top), Enet1 (bottom).
P12	4-pin 5V and 12V power jack connector
P13	4-pin 5V and 12V floppy disk connector for external power of mini PCI Express card
BT1	RTC battery holder, CR2032 type. The real-time clock on the RDB requires a battery when the board is powered off. When placing or replacing the battery, take care to ensure that the polarity is correct.
J3	Background Debug Mode (BDM). Header for flash programming and debug of on-board MC9S08QG8 Micro controller.
J5	Case connector

Table 4. Connectors, Headers, Jumpers, Switches, and LEDs (continued)

Reference	Description
J8	SPI interfaces connector
Jumpers	
J1	MCU battery backup enable. Install jumper 1-2 to power MCU in battery standby mode. This is required if the MCU is programmed to function as a real time clock. Install jumper 2-3 (default) to power real time clock chip DS1339 if the MCU real time clock function is not used
J2	12V fan connector
J4	RS-232C #2 select header. Selects RS-232C #2 on P1 (bottom) to be connected to either CPU UART2 (Install jumpers 1–3, 2–4 as default) or MCU SCI (Install jumpers 3–5, 4–6). Alternatively, CPU UART2 can be connected to the MCU SCI instead (Install jumpers 5–7, 6–8).
J6	MCU LED1 header. Connection to external, MCU controlled LED1. Pin 1 is Anode
J7	CPU Power-on reset source jumper. CPU Power-On Reset can be controlled by a hardware MIC811 reset chip (jumper 2–3 as default) or by MCU firmware (jumper 1–2).
Switches	
S1	Board revision and boot Flash selection switch.
S2	Reset configuration word source selection switch.
S3	Power-on push button. Powers up the MPC8308_RDB board.
S4	System reset button. Resets the MPC8308_RDB board.
LEDs	
D1	USB PHY CTL0
D2	USB PHY CTL1
D3	USB VBUS
D4	Enet1 LINK10
D5	Enet1 LINK100
D6	Enet1 DUPLEX
D7	Enet1 RX
D11	MCU LED1
D12	MCU LED2
D16	5 V Indicator
D17	5 V standby indicator
D18	3.3V Indicator

3.1 COP Connector (P2)

The COP connector allows the user to connect a COP/JTAG-based debugger to the MPC8308 for debugging. Table 5 lists the pin assignments of the COP connector.

Table 5. COP Connector Pin Assignments

Pin	Signal	Pin	Signal
1	TDO	2	GND
3	TDI	4	$\overline{\text{TRST}}$
5	$\overline{\text{QREQ}}$	6	VDD_SENSE
7	TCK	8	$\overline{\text{CKSTP\_IN}}$
9	TMS	10	NC
11	$\overline{\text{SRESET}}$	12	NC
13	$\overline{\text{HRESET}}$	14	NC
15	$\overline{\text{CKSTP\_OUT}}$	16	GND

3.2 Case Connector (J5)

The case connector (J5) connects to the case power switch, power LED, reset switch, and hard disk LED.

- PWR_SW can connect to the 2-pin power push button on the front panel.
- PWR_LED lights when the system is turned ON.
- RST_SW can connect to the 2-pin reset push button on the front panel.

Table 6 lists the pin assignments of the case connector.

Table 6. Case Connector J5 Pin Assignments

Pin	Signal
1	N/C
2	N/C
3	N/C
4	N/C
5	N/C
6	POWER LED + (Green)
7	N/C
8	POWER LED - (White)
9	RESET SW + (Blue)
10	RESET SW - (White)
11	POWER SW + (Green)
12	POWER SW - (White)

3.3 USB Connector (P8)

There is a mini-AB USB connector on the MPC8308_RDB. It is connected to the external ULPI USB PHY. Figure 16 shows the USB connectors in front panel.

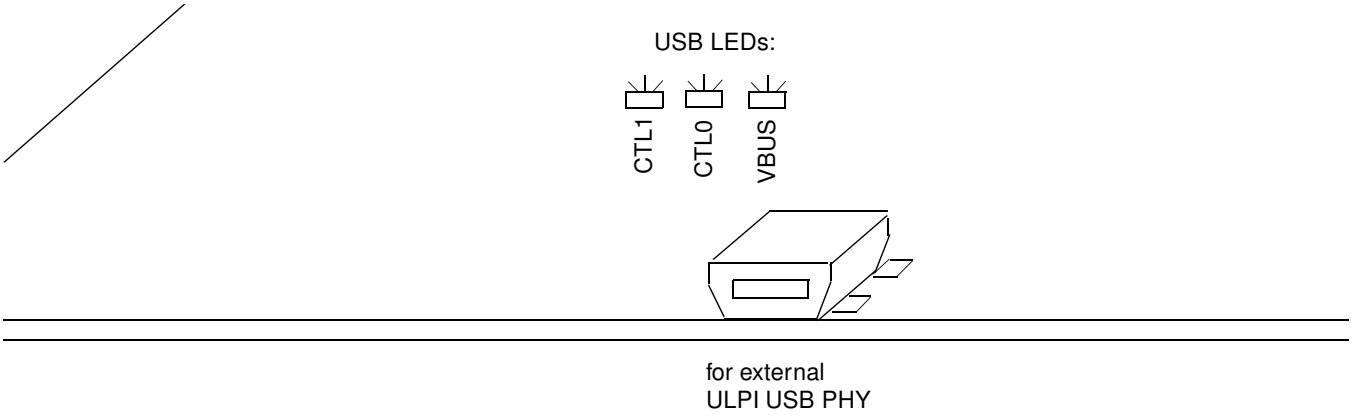

Figure 16. USB Connectors

3.4 Ethernet Connectors (P9, P10, P11)

The MPC8308_RDB has six Ethernet ports (RJ-45). Five ports (G2–G6) are supported by eTSEC2 (L2 switch), another port (G1) is supported by eTSEC1 (GBE PHY). Figure 17 shows the G1–G6 mapping viewing from the front panel.

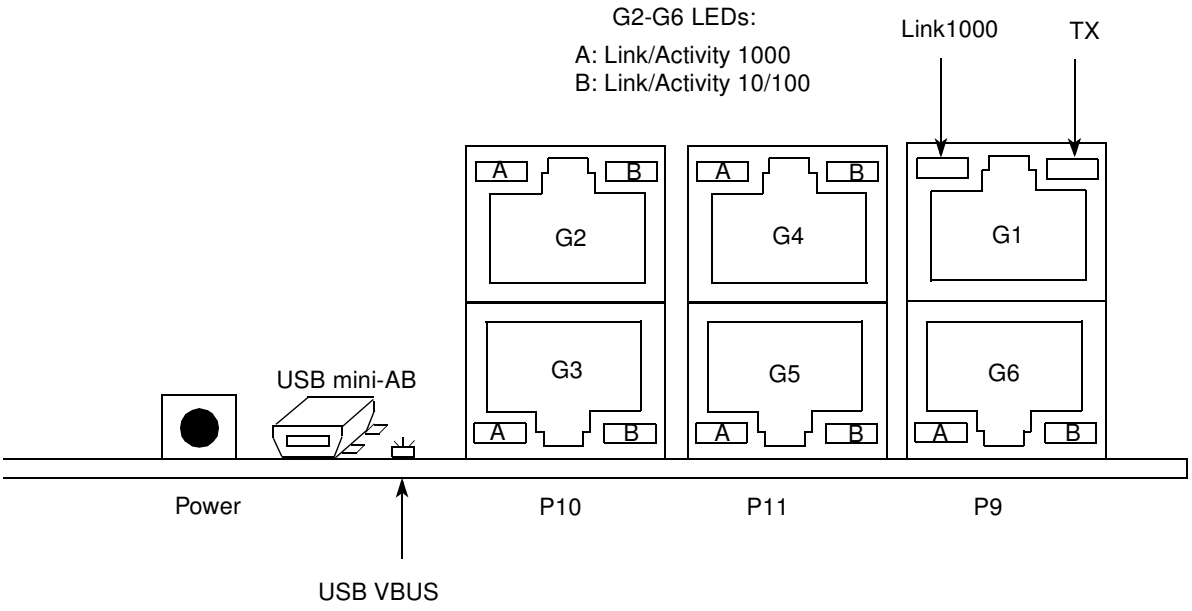

Figure 17. Ethernet ports mapping

3.5 RS-232 UART Connector (P1)

Serial interfaces are available at connector P1. It is a double deck RS-232 female connector. The upper port is UART1 and the lower port is UART2. Figure 18 shows the RS-232 UART connector front view.

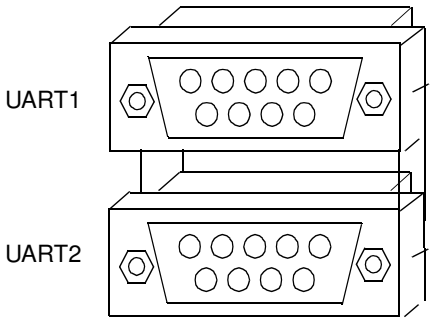

Figure 18. RS-232 UART Connectors

3.6 SD Memory Card Socket (P5)

The SD card socket (P5) for SD memory card installation is located next to the UART connector of the board. Figure 19 shows how to install a SD memory card to the board.

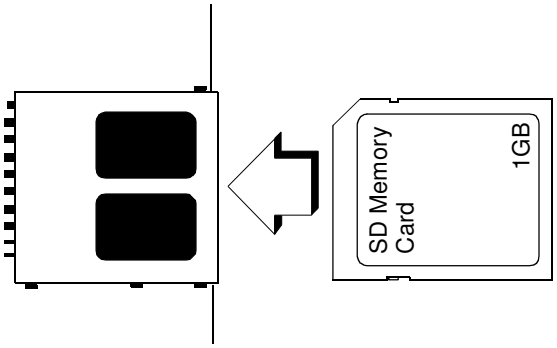

Figure 19. Installation of SD Card

3.7 Battery Holder

The MPC8308_RDB board contains an RTC that requires a battery to maintain the data inside the RTC. The battery holder (BT1) accommodates a CR-2032. Figure 20 shows how to insert a battery.

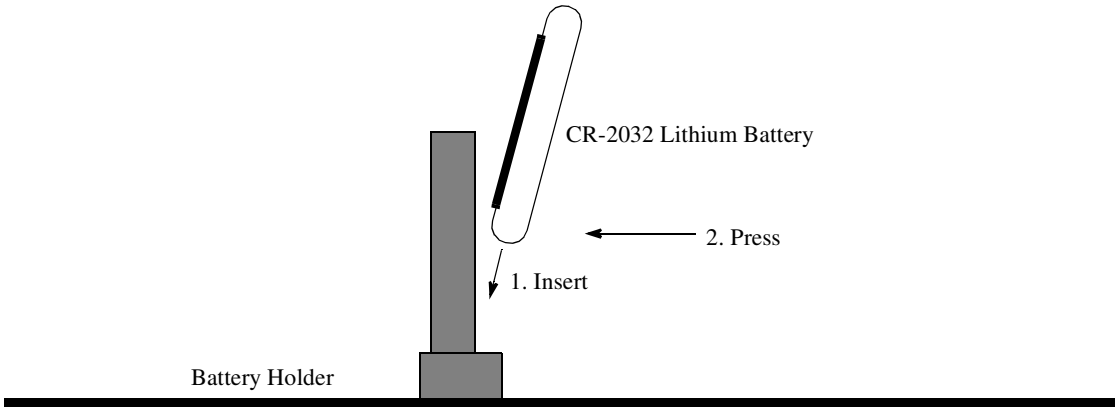

Figure 20. Installation of Battery

3.8 Mini PCI Express Connector (P3)

A Mini PCI Express connector (P3) for Mini PCI Express card installation is present on the board. Figure 21 shows how to install a Mini PCI Express card.

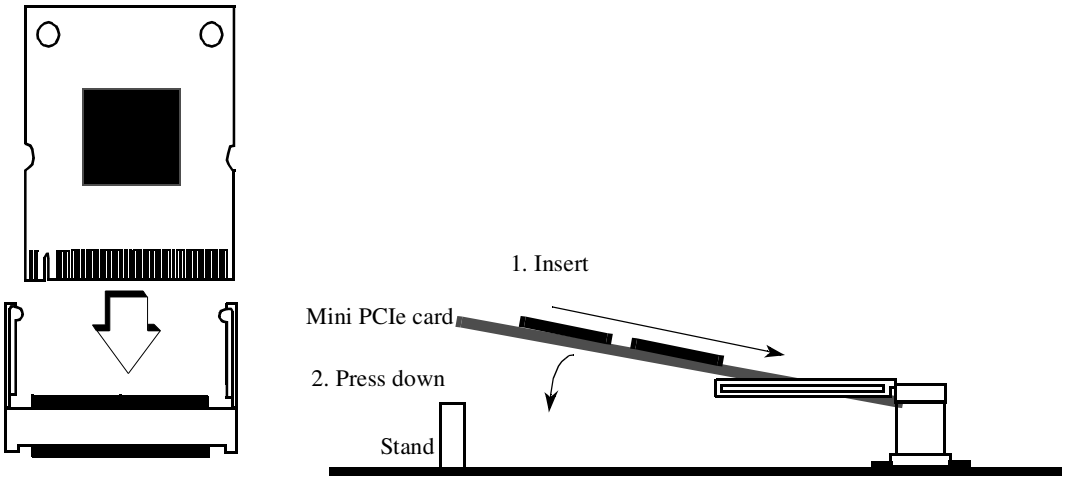

Figure 21. Installation of MiniPCI Card

3.9 IEEE 1588 Connector (P4) - Optional

An optional header (P4) is provided for IEEE 1588 signals connection. It is double row of 2 × 8 header connector. The pinout of this connector is shown in Figure 22.

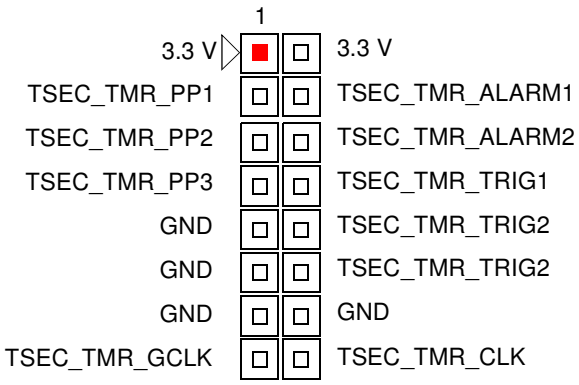

Figure 22. IEEE 1588 Connector (P4) - Optional

3.10 DIP Switch S1

DIP switch S1 on the board is shown in Figure 23, with the factory default configuration.

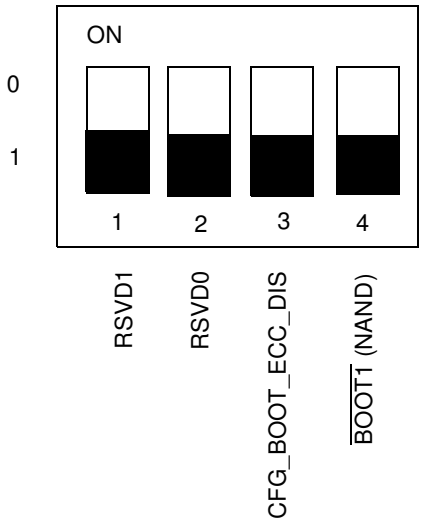

Figure 23. DIP Switch S1

RSVD[0:1] is reserved. When software options are implemented, its values can be read from a buffer on the board. CFG_BOOT_ECC_DIS switch is OFF by default to disable booting with ECC by driving HIGH to the signal LB_POR_CFG_BOOT_ECC_DIS (TSEC1_TX_ER) during power on reset. $\overline{\text{BOOT1}}$ selects the boot device on the RDB. By default, $\overline{\text{BOOT1}}$ is set, so chip-select 0 ($\overline{\text{CS0}}$) is connected to the NOR Flash. $\overline{\text{CS1}}$ is connected to the NAND flash memory. If $\overline{\text{BOOT1}}$ is cleared, $\overline{\text{CS0}}$ is connected to NAND flash memory, and $\overline{\text{CS1}}$ is connected to NOR flash memory.

3.11 DIP Switch S2

DIP switch S2 selects the reset configuration source (RST_CFG_SRC) for the MPC8308. Figure 24 shows the factory default configuration of S2.

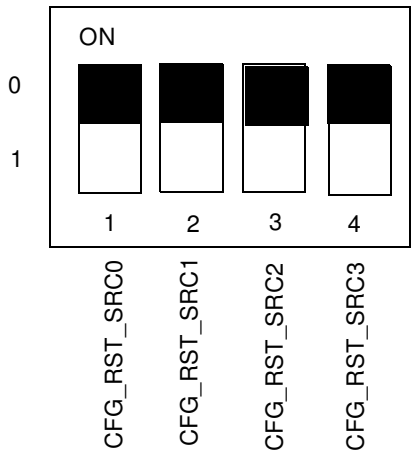

Figure 24. DIP Switch S2

Check the MPC8308 reference manual for the meaning of the CFG_RST_SRC combination. By default, the DIP switch is set to all ON, meaning CFG_RST_SRC[0..3] = 0000. In this case, the hardware reset configuration is loaded from local bus NOR flash memory.

4 MPC8308_RDB Board Configuration

This section describes the operational frequency and configuration options of the MPC8308_RDB.

4.1 Reset Configuration Word

The reset configuration word (RCW) controls the clock ratios and other basic device functions such as boot location, eTSEC mode and endian mode. The reset configuration word is divided into reset configuration word low register (RCWLR) and reset configuration word high register (RCWHR) and is loaded from the local bus during the power-on or hard reset flow. The default RCW low bit setting is 0x4406_0000. The default RCW high bit setting is 0xA060_6C00. The RCW is located at the lowest 64 bytes of the boot flash memory, which is 0xFE00_0000 if the default memory map is used.

Table 7. Default RCW in Flash Memory

Address				
FE000000:	44444444	44444444	06060606	06060606
FE000010:	00000000	00000000	00000000	00000000
FE000020:	a0a0a0a0	a0a0a0a0	60606060	60606060
FE000030:	6c6c6c6c	6c6c6c6c	00000000	00000000

The RCW definitions are shown in Figure 25 and Figure 26.

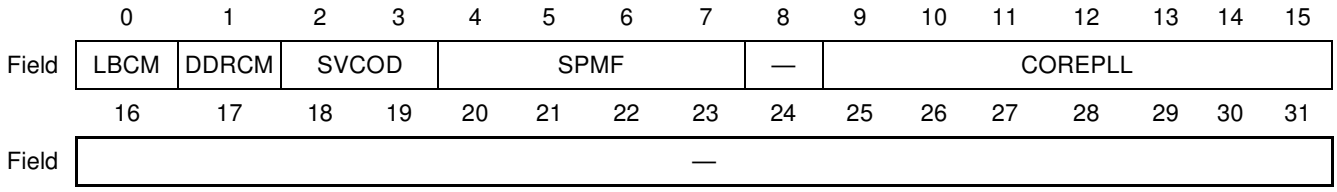

Figure 25. Reset Configuration Word Low Register (RCWLR)

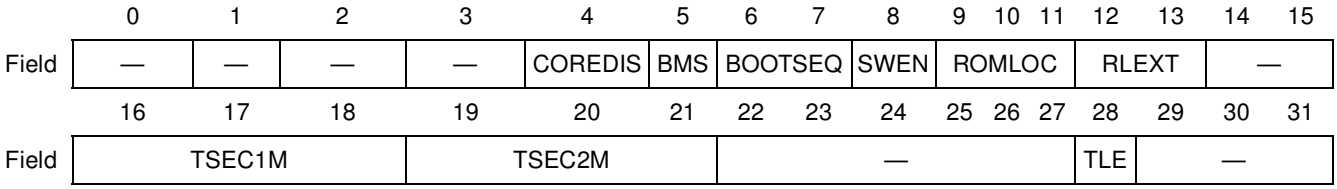

Figure 26. Reset Configuration Word High Register (RCWHR)

Table 8. RCWLR Bit Descriptions

Bits	Name	Meaning	Description	
0	LBCM	Local bus clock mode	Local Bus Controller Clock: CSB_CLK	
			0 (Default)	ratio 1:1
			1	ratio 2:1
1	DDRCM	DDR SDRAM clock mode	DDR Controller Clock: CSB_CLK	
			0	ratio 1:1
			1 (Default)	ratio 2:1
2–3	SVCOD	System PLL VCO division	VCO Division Factor	
			00 (Default)	2
			01	4
			10	8
			11	1
4–7	SPMF[0–3]	System PLL multiplication factor	0000	Reserved
			0001	Reserved
			0010	2:1
			0011	3:1
			0100 (Default)	4:1
			0101	5:1
			0110	6:1
			0111-1111	Reserved
8	—	Reserved	Must be cleared.	

Table 8. RCWLR Bit Descriptions (continued)

Bits	Name	Meaning	Description	
9–15	COREPLL [0–6]	Value	coreclk: csb_clk	VCO divider
		nn 0000 0	PLL bypassed	PLL bypassed
		11 nnnn n	n/a	n/a
		00 0001 0	1:1	2
		01 0001 0	1:1	4
		10 0001 0	1:1	8
		00 0001 1	1.5:1	2
		01 0001 1	1.5:1	4
		10 0001 1	1.5:1	8
		00 0010 0	2:1	2
		01 0010 0	2:1	4
		10 0010 0	2:1	8
		00 0010 1	2.5:1	2
		01 0010 1	2.5:1	4
		10 0010 1	2.5:1	8
		00 0011 0(Default)	3:1	2
		01 0011 0	3:1	4
		10 0011 0	3:1	8
16–31	—	Reserved.	Must be cleared.	

Table 9. RCWHR Bit Descriptions

Bits	Name	Meaning	Description	
0-3	—	Reserved	Must be cleared	
4	COREDIS	Core disable mode	0 (Default)	e300 enabled
			1	e300 disabled
5	BMS	Boot memory space	0 (Default)	0x0000_0000–0x007F_FFFF
			1	0xFF80_0000–0xFFFF_FFFF

Table 9. RCWHR Bit Descriptions

Bits	Name	Meaning	Description	
6–7	BOOTSEQ	Boot sequencer configuration	00 (Default)	Boot sequencer is disabled
			01	Boot sequencer load configuration from I^2C
			10	Boot sequencer load configuration from EEPROM
			11	Reserved
8	SWEN	Software watchdog enable	0 (Default)	Disabled
			1	Enabled
9–11	ROMLOC	Boot ROM interface location	000	DDR2 SDRAM
			001	Reserved
			010,011, 100	Reserved
			101	Local bus GPCM, 8 bits
			110 (Default)	Local bus GPCM, 16 bits
			111	Reserved
12–13	RLEXT	Boot ROM location extension	00 (Default)	Legacy mode
			01	NAND Flash mode
			10,11	Reserved
14-15	—	Reserved	Must be cleared	
16-18	TSEC1M	TSEC1 Mode	000	MII mode
			001,010	Reserved
			011 (Default)	RGMII mode
			100,101,110,111	Reserved
19-21	TSEC2M	TSEC2 Mode	000	MII mode
			001,010	Reserved
			011 (Default)	RGMII mode
			100,101,110,111	Reserved
22-27	—	Reserved	Must be cleared	
28	TLE	True little endian	0 (Default)	Big-endian mode
			1	True little endian mode
29-31	—	Reserved	Must be cleared	

4.2 Power Supply

The MPC8308_RDB board requires a power supply from the 4-pin power jack. It provides 12 V and 5 V supply to the board. Core voltage, DDR2 voltage, RGMII voltage, and PHY-specific voltages are provided by either switching or linear regulated depending on the voltage drop and current consumption requirement. Table 10 shows the power supply of each source. The MPC8308 does not require the core

supply voltage and IO supply voltages to be applied in any particular order. However, during the power ramp up, before the power supplies are stable, there may be an interval when the IO pins are actively driven. After the power is stable, as long as $\overline{\text{PORESET}}$ is asserted, most IO pins are three-stated. To minimize the time that IO pins are actively driven, apply core voltage before IO voltage and assert $\overline{\text{PORESET}}$ before the power supplies fully ramp up.

Table 10. Power Supply Usage Summary

Voltage	Usage	Budget	Solution
1V	Vcore	TBD	MIC1954EUB+ switching
1.2V	VSC7385 core	TBD	MIC37302 LDO (3A)
1.5V	RTL8211B	TBD	NCP 1117SRAR3G LDO (1A)
1.5V	mini PCIe connector	TBD	NCP 1117SRAR3G LDO (1A)
1.8V	DDR2, RTL8211B	TBD	MIC37302 LDO (3A)
2.5V	VSC7385 IO	TBD	NCP 1117SRAR3G LDO (1A)
3.3V	General IO	TBD	MIC1954EUB+ switching
5V	Switching power	TBD	Direct from Power Jack
12V	external 12V supply of mini PCIe adaptor	TBD	Direct from Power Jack

4.3 Chip-Select Assignments and Memory Map -TBD

Table 11 shows an example memory map on the MPC8308_RDB for u-boot in NOR flash memory.

Table 11. Example Memory Map, Local Access Window, and Chip-Select Assignments

Address Range	Target Interface	Chip-Select Line	Device Name	Port Size (Bits)
0x0000_0000–0x07FF_FFFF	DDR2	MCS0#	DDR SDRAM (128 Mbyte)	32
0xE000_0000–0xE00F_FFFF	Internal bus	Nil	IMMR (1 Mbyte)	—
0xE280_0000–0xE280_7FFF	NAND Controller	LCS1#	NAND Flash window (32Kbyte)	8
0xF000_0000–0xF001_FFFF	Local bus	LCS2#	VSC7385 (128Kbyte)	8
0xFE00_0000–0xFE7F_FFFF	Local bus	LCS0#	Boot Flash (8 Mbyte)	16

5 Getting Started

This section describes how to boot the MPC8308_RDB. The on-board flash memory is preloaded with a flash image from the factory. Before powering up the board, verify that all the on-board DIP switches and jumpers are set to the factory defaults according to the settings listed in Section 5.1, “Board Jumper Settings,” and make all external connections as described in Section 5.2, “External Cable Connections.”

CAUTION

Avoid touching areas of integrated circuitry and connectors; static discharge can damage circuits.

5.1 Board Jumper Settings

Figure 27 shows the top view of the MPC8308_RDB with pin 1 marked for each reference. There are two DIP switches and some jumpers.

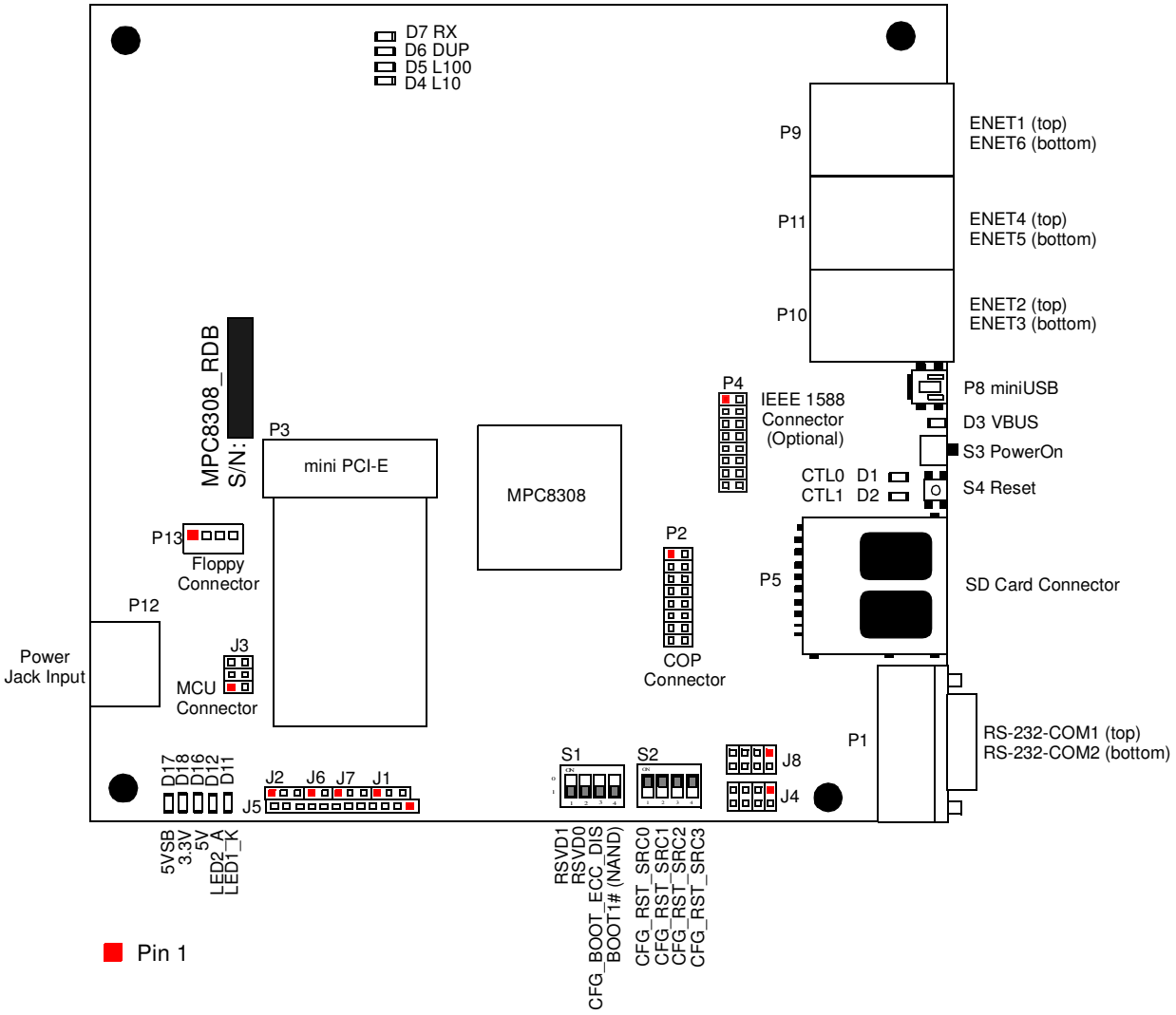

Figure 27. MPC8308_RDB Top View

The default settings of switches and jumpers are listed in Table 12.

Table 12. Default DIP Switch and Jumper Setting

Reference	Default Setting
S1	1111 (all OFF)
S2	0000 (all ON)
J1	short pin 2-3
J4	short pin 1-3 and 2-4
J7	short pin 2-3

5.2 External Cable Connections

Do not turn on power until all cables are connected and the serial port is configured as described in Section 5.3, "Serial Port Configuration (PC)." Connect the serial port of the MPC8308_RDB system and the personal computer using an RS-232 cable as in shown in Figure 28.

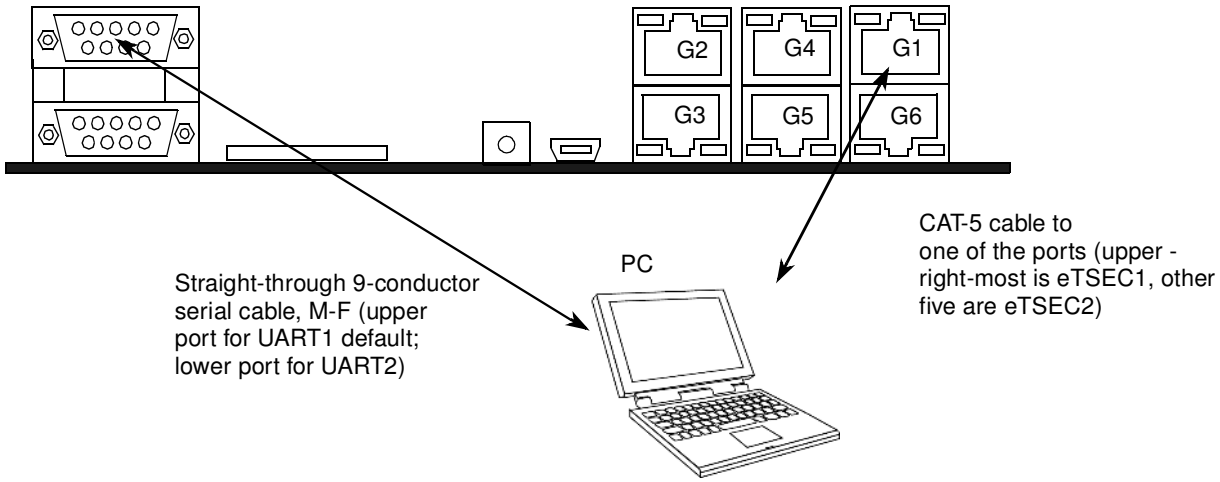

Figure 28. External Connections

5.3 Serial Port Configuration (PC)

Before powering up the MPC8308_RDB, configure the serial port of the attached computer with the following values:

- Data rate: 115200 bps
- Number of data bits: 8
- Parity: None
- Number of Stop bits: 1
- Flow Control: None

5.4 Power Up

The 4-pin power jack (P12) should be used to supply necessary DC power to the board.

WARNING

Turn off the main power for the RDB case before the power connector is attached.

Power up the power supply. A few seconds after power up, the u-boot prompt => should be received by the serial terminal program as shown here:

```
U-Boot 1.x.x (FSL Development) (Date - time) MPC83XX

Clock configuration:
         Coherent System Bus:  xxx MHz
         Core:                 yyy MHz
         Local Bus Controller: xxx MHz
         Local Bus:             yy MHz
         DDR:                  xxx MHz
         …
         Hit any key to stop autoboot:  0
=>
```

NOTE

The normal function of the product may be disturbed by strong electromagnetic interference. If so, simply reset the product to resume normal operation by following the instructions in the manual. If normal function does not resume, use the product in another location.

6 MPC8308_RDB Software

A board support package (BSP) is pre-installed on the MPC8308_RDB. This BSP consists of a bootloader (u-boot), a generic PowerPC Linux-based system, and an associated file system. U-boot, the Linux kernel, and the file system reside in the on-board flash memory. At power up, the Linux system runs on the MPC8308_RDB.

The MPC8308_RDB BSP generation takes advantage of a tool called the Linux Target Image Builder (LTIB). LTIB is a suite of tools that leverages existing open source configuration scripts and source code packages and bundles them into a single BSP-generation package. The source code packages include boot loaders and Linux kernel sources as well as many user-space source code packages to build a complete BSP. LTIB also provides compiler packages required to build the BSP. Freescale developers use LTIB to create BSPs for a multitude of Freescale development targets. LTIB leverages as many BSP elements as possible for all Freescale-supported targets, and it offers the flexibility to customize components that require platform-specific modifications.

The MPC8308_RDB BSP release package contains a file named `MPC8308_RDB-<yyyymmdd>.iso`. This file is an ISO image that can be burned to a CD-ROM or mounted directly from your hard disk. Note that `<yyyymmdd>` is the release creation date. The LTIB installation script that installs all necessary packages on

a host Linux PC and allows you to modify the BSP and packages within the BSP is in the `/ltib-MPC8308-RDB` subdirectory within the ISO image.

This ISO image contains a file called `Readme.txt` that describes how to generate and install the BSP on the MPC8308_RDB hardware platform. `Readme.txt` contains the latest information for each BSP release. The ISO image also contains `Release Notes.txt`, which describes changes to the current BSP version versus earlier releases. To rebuild the BSP package or to add application software, carefully follow the instructions in `Readme.txt`. This file contains details on how to build, run, and install the BSP. It guides the user to achieve a successful re-installation of the BSP on the MPC8308_RDB. This ISO image contains the following documents as well:

- `MPC8308RDBUG.pdf`. This user's guide document in PDF format.
- `MPC8308_RDB_schematic.pdf`. The platform schematic in PDF format.
- `LtibFaq.pdf`. Frequently asked questions for LTIB, which is a useful document describing how to use LTIB to build the ISO image.

For more information on the MPC8308_RDB, visit the Freescale web site listed on the back cover of this document. To run demonstrations or to acquire details of Freescale third-party applications for this MPC8308_RDB, contact your local Freescale sales office.

7 Revision History

Table 13 provides a revision history for this document.

Table 13. Document Revision History

Rev. Number	Date	Substantive Change(s)
1	10/2009	Initial release
2	01/2010	Updated Figure 10. Memory Card Connection Updated Figure 25. Reset Configuration Word Low Register (RCWLR) Updated Figure 26. Reset Configuration Word High Register (RCWHR) Updated Table 7. Default RCW in Flash Memory Updated Table 8. RCWLR Bit Descriptions Updated Table 9. RCWHR Bit Descriptions
3	03/2010	General document format and naming update

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