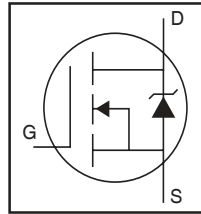


HEXFET® Power MOSFET

Applications

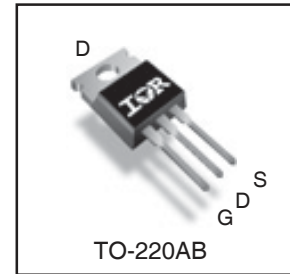
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits



V_{DSS}		150V
$R_{DS(on)}$	typ.	9.3mΩ
	max.	11mΩ
I_D (Silicon Limited)		104A

Benefits

- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead Free
- RoHS Compliant, Halogen-Free



G	D	S
Gate	Drain	Source

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFB4115PbF	TO-220	Tube	50	IRFB4115PbF

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	104	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	74	
I_{DM}	Pulsed Drain Current ①	420	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	380	W
	Linear Derating Factor	2.5	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ③	18	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

Avalanche Characteristics

E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ②	830	mJ
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Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ④	—	0.40	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient ⑦⑧	—	62	

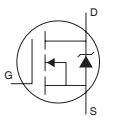
Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	150	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.18	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 3.5\text{mA}$ ①
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	9.3	11	m Ω	$V_{GS} = 10V, I_D = 62A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 150V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 150V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
R_G	Internal Gate Resistance	—	2.3	—	Ω	

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

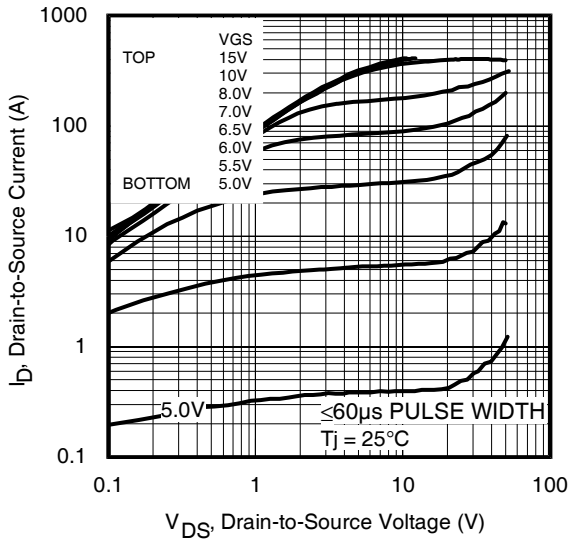
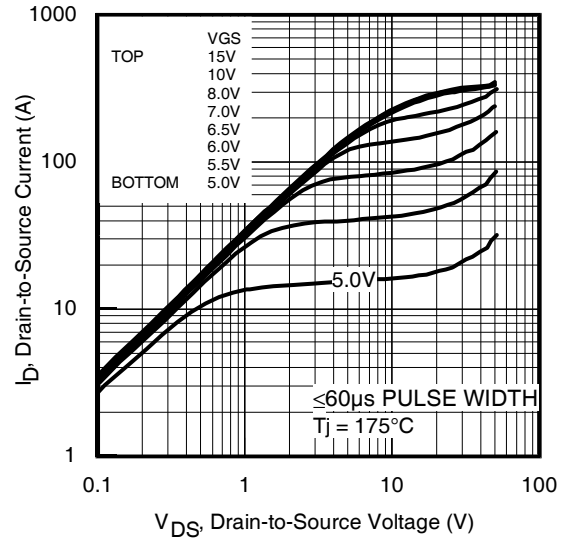
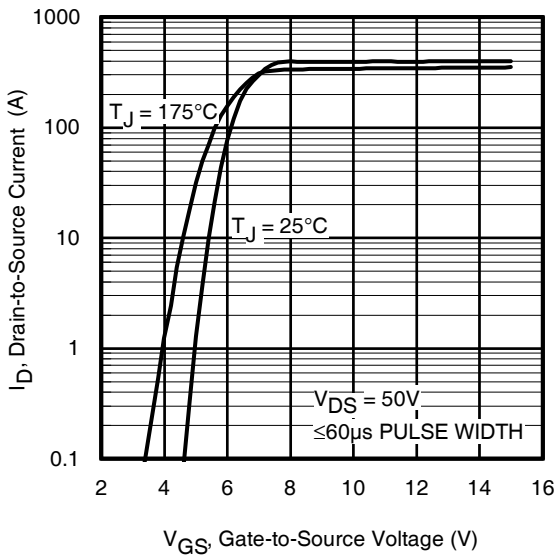
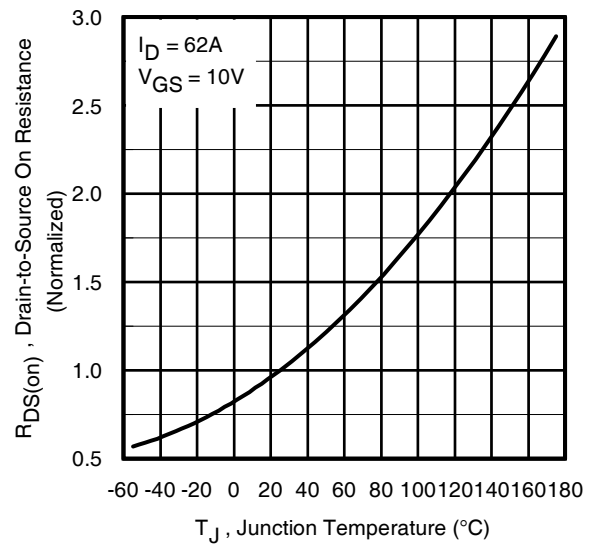
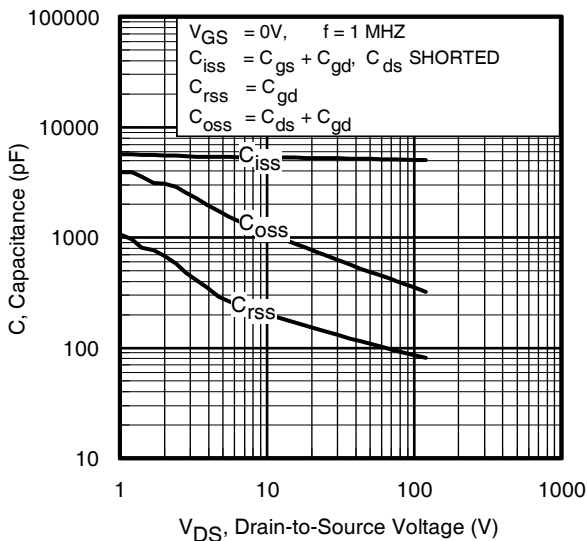
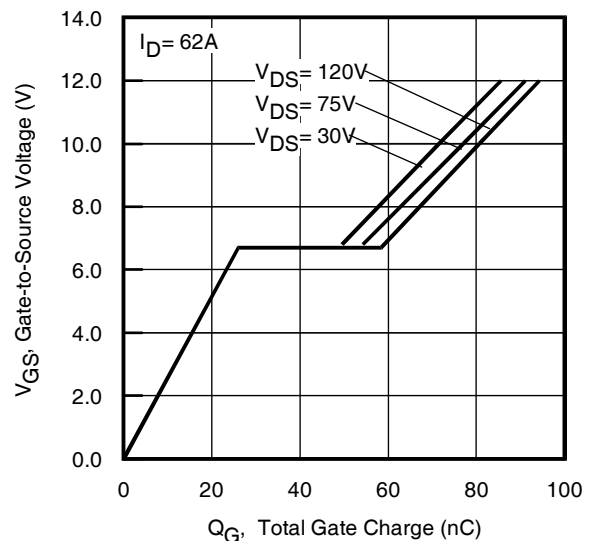
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	97	—	—	S	$V_{DS} = 50V, I_D = 62A$
Q_g	Total Gate Charge	—	77	120	nC	$I_D = 62A$
Q_{gs}	Gate-to-Source Charge	—	28	—		$V_{DS} = 75V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	26	—		$V_{GS} = 10V$ ④
Q_{sync}	Total Gate Charge Sync. ($Q_g - Q_{gd}$)	—	51	—		$I_D = 62A, V_{DS} = 0V, V_{GS} = 10V$
$t_{d(on)}$	Turn-On Delay Time	—	18	—	ns	$V_{DD} = 98V$
t_r	Rise Time	—	73	—		$I_D = 62A$
$t_{d(off)}$	Turn-Off Delay Time	—	41	—		$R_G = 2.2\Omega$
t_f	Fall Time	—	39	—		$V_{GS} = 10V$ ④
C_{iss}	Input Capacitance	—	5270	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	490	—		$V_{DS} = 50V$
C_{riss}	Reverse Transfer Capacitance	—	105	—		$f = 1.0\text{ MHz}$, See Fig. 5
$C_{oss\text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)	—	460	—		$V_{GS} = 0V, V_{DS} = 0V$ to $120V$ ⑥, See Fig. 11
$C_{oss\text{ eff. (TR)}}$	Effective Output Capacitance (Time Related)	—	530	—		$V_{GS} = 0V, V_{DS} = 0V$ to $120V$ ⑥

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	104	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ②	—	—	420	A	
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 62A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	86	—	ns	$T_J = 25^\circ\text{C}$ $V_R = 130V,$
		—	110	—		$T_J = 125^\circ\text{C}$ $I_F = 62A$
Q_{rr}	Reverse Recovery Charge	—	300	—	nC	$T_J = 25^\circ\text{C}$ $di/dt = 100A/\mu s$ ④
		—	450	—		$T_J = 125^\circ\text{C}$
I_{RRM}	Reverse Recovery Current	—	6.5	—	A	$T_J = 25^\circ\text{C}$
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Recommended max EAS limit, starting $T_J = 25^\circ\text{C}$, $L = 0.17\text{mH}, R_G = 25\Omega, I_{AS} = 100A, V_{GS} = 15V$.
- ③ $I_{SD} \leq 62A, di/dt \leq 1040A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 175^\circ\text{C}$.
- ④ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ⑤ $C_{oss\text{ eff. (TR)}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑥ $C_{oss\text{ eff. (ER)}}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑧ R_{θ} is measured at T_J approximately 90°C .


Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance vs. Temperature

Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

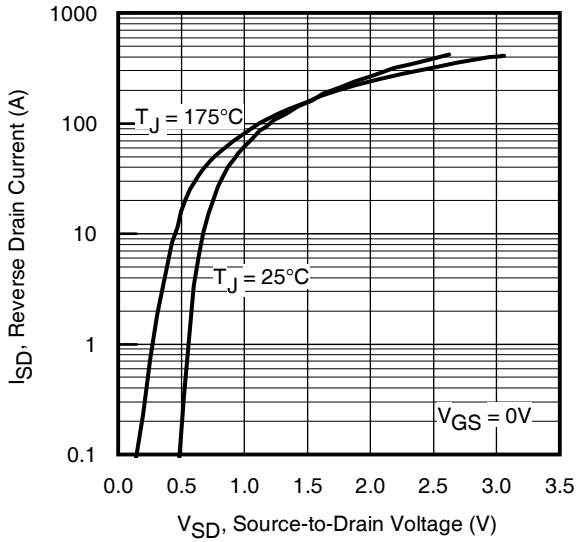


Fig 7. Typical Source-Drain Diode Forward Voltage

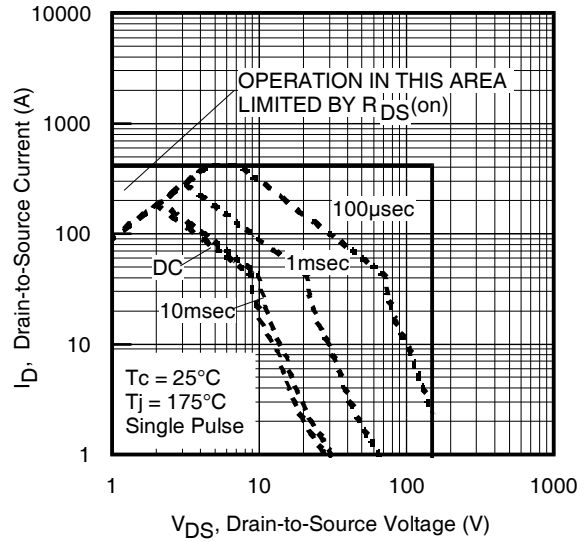


Fig 8. Maximum Safe Operating Area

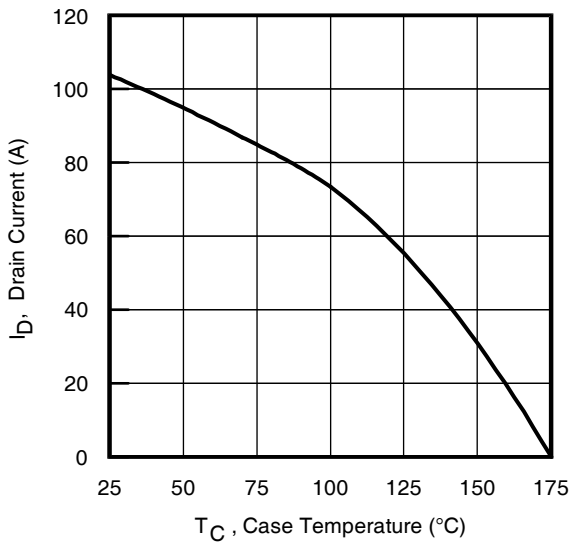


Fig 9. Maximum Drain Current vs. Case Temperature

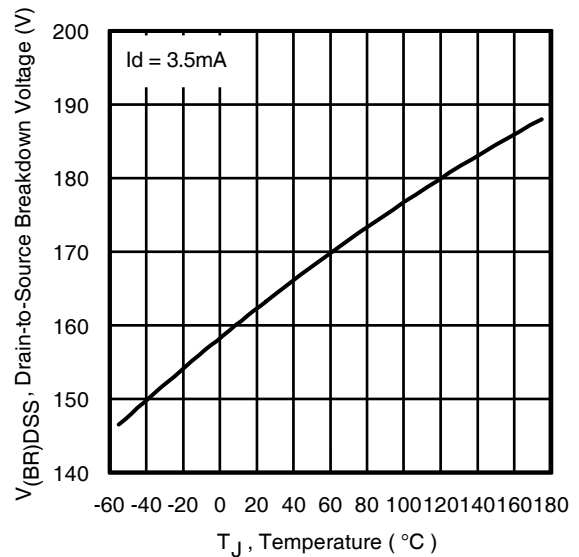


Fig 10. Drain-to-Source Breakdown Voltage

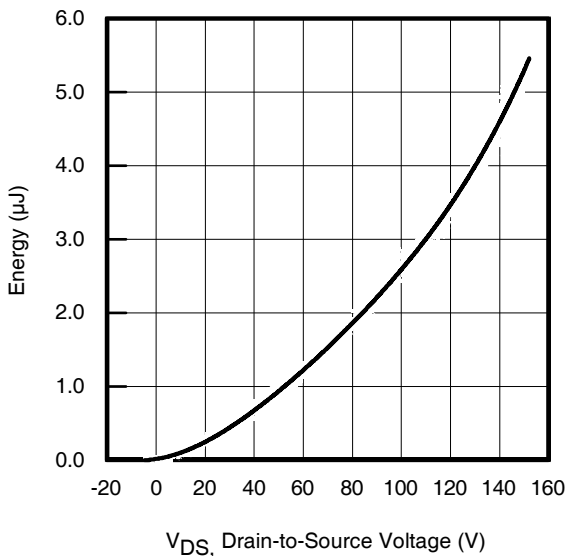


Fig 11. Typical C_{OSS} Stored Energy

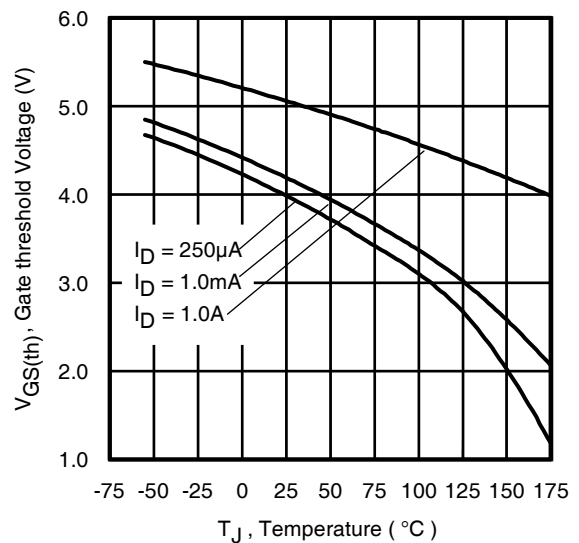


Fig 12. Threshold Voltage vs. Temperature

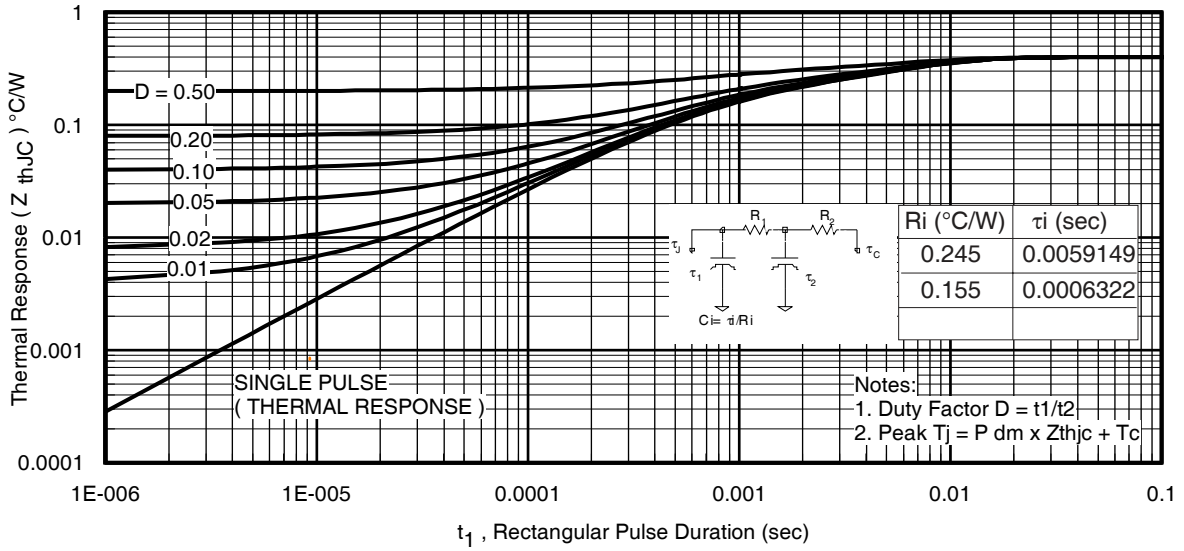


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

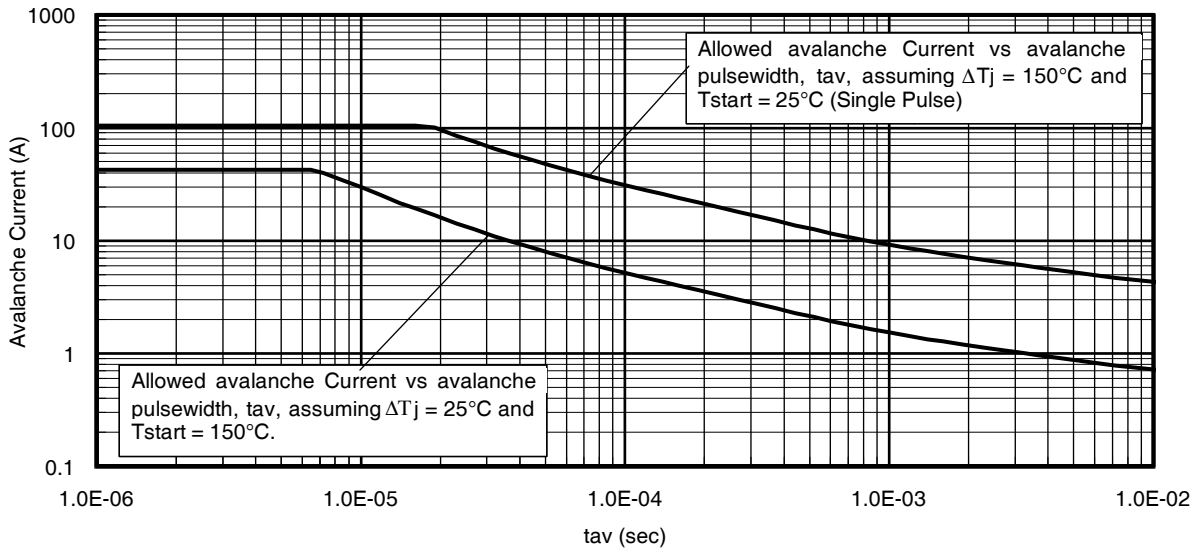


Fig 14. Typical Avalanche Current vs.Pulsewidth

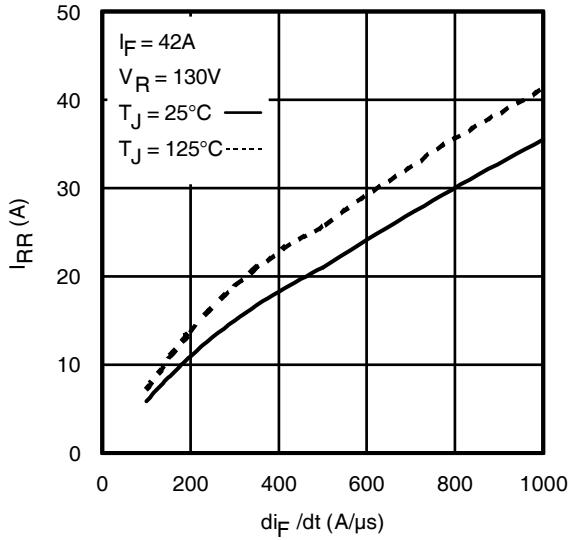


Fig 15. - Typical Recovery Current vs. di_f/dt

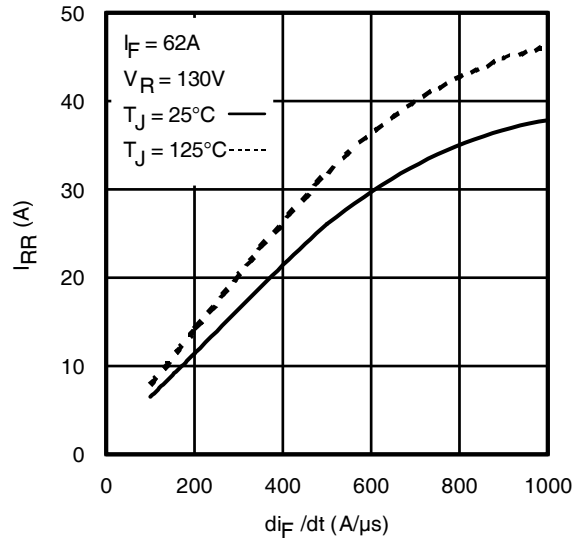


Fig 16. - Typical Recovery Current vs. di_f/dt

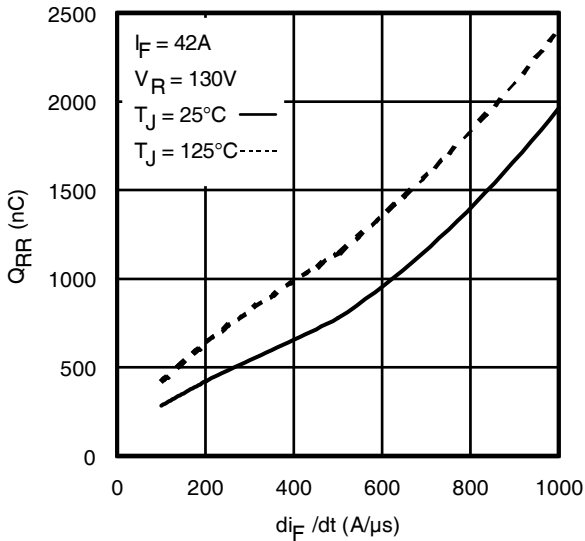


Fig 17. - Typical Stored Charge vs. di_f/dt

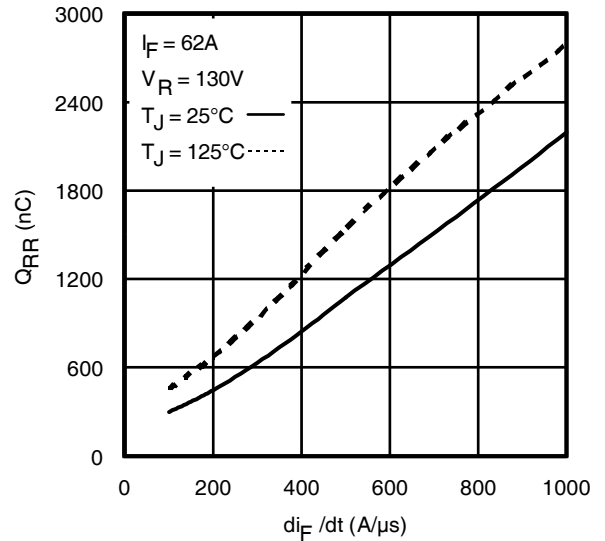
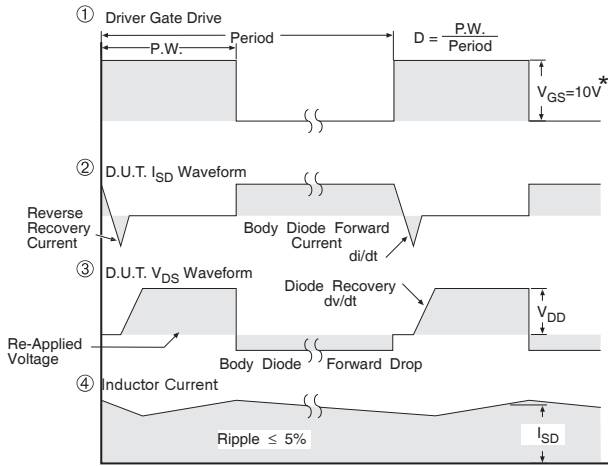
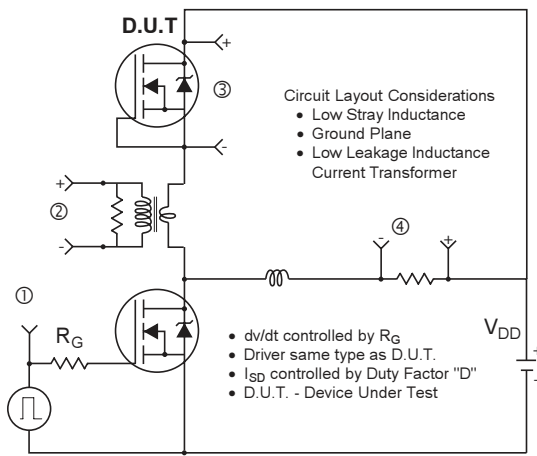


Fig 18. - Typical Stored Charge vs. di_f/dt



* $V_{GS} = 5V$ for Logic Level Devices

Fig 19. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

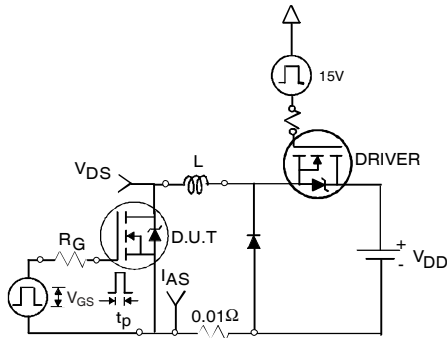


Fig 20a. Unclamped Inductive Test Circuit

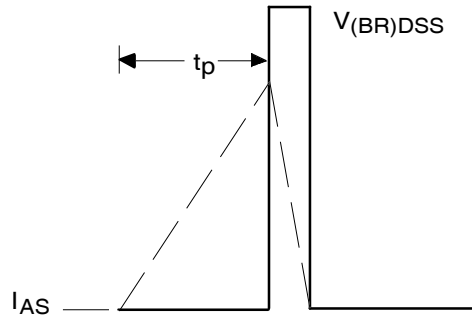


Fig 20b. Unclamped Inductive Waveforms

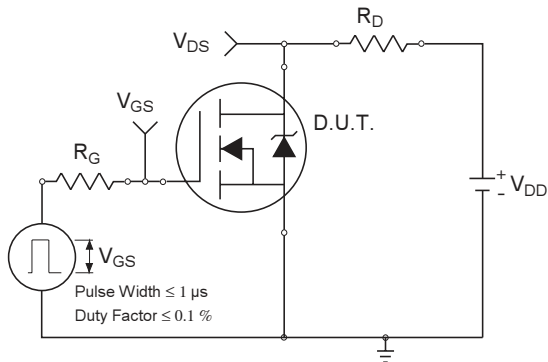


Fig 21a. Switching Time Test Circuit

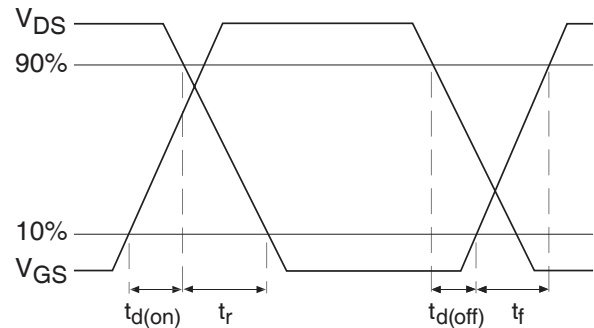


Fig 21b. Switching Time Waveforms

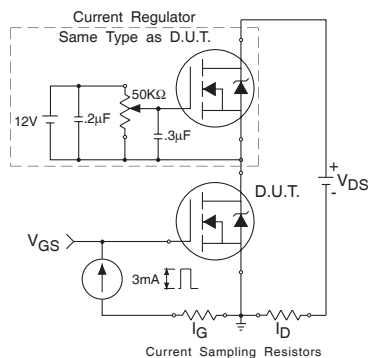


Fig 22a. Gate Charge Test Circuit

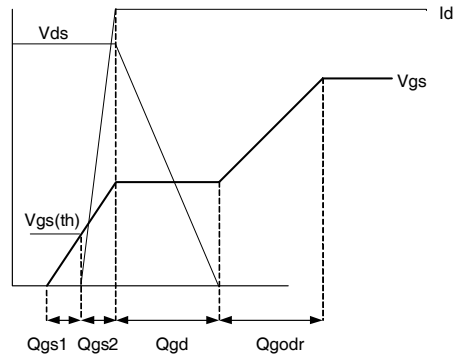
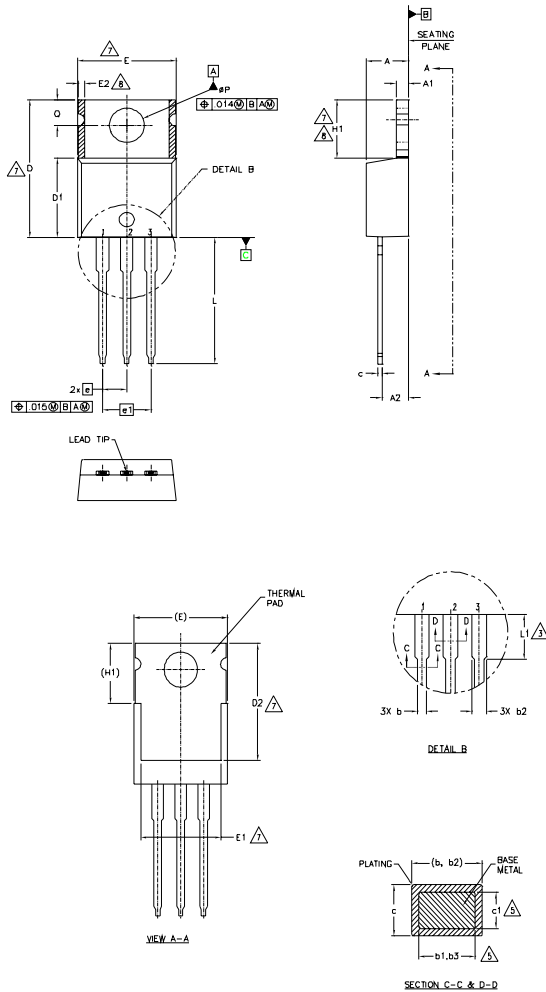


Fig 22b. Gate Charge Waveform

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



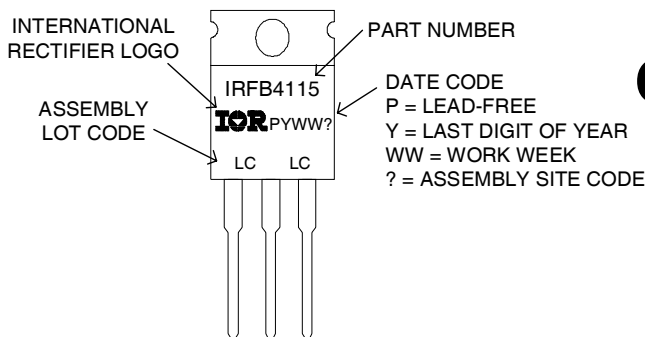
NOTES:

- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
- 6.- CONTROLLING DIMENSION : INCHES.
- 7.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
- 8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
- 9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

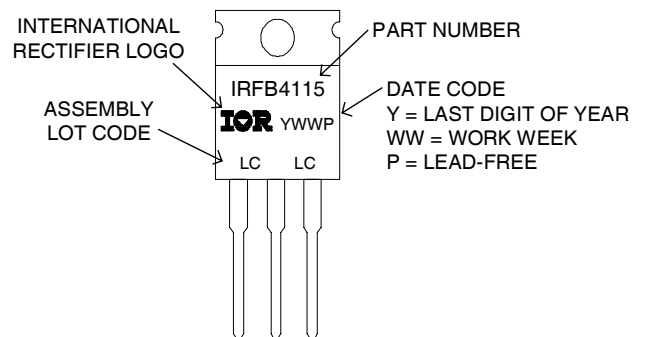
SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	1.14	1.40	.045	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	-	0.76	-	.030	8
e	2.54 BSC		.100 BSC		
e1	5.08 BSC		.200 BSC		
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
phi P	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

- LEAD ASSIGNMENTS**
- HEXFET**
- 1.- GATE
 - 2.- DRAIN
 - 3.- SOURCE
- IGBTs, CoPACK**
- 1.- GATE
 - 2.- COLLECTOR
 - 3.- EMITTER
- DIODES**
- 1.- ANODE
 - 2.- CATHODE
 - 3.- ANODE

TO-220AB Part Marking Information



OR



TO-220AB packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

Qualification information[†]

Qualification level	Industrial [†]	
	(per JEDEC JESD47F ^{††} guidelines)	
Moisture Sensitivity Level	TO-220	N/A
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>

†† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comment
4/28/2014	<ul style="list-style-type: none"> Updated data sheet with new IR corporate template. Updated package outline & part marking on page 7. Added bullet point in the Benefits "RoHS Compliant, Halogen -Free" on page 1. Updated typo on the Fig.16 and Fig.17, unit of Y-axis from "A" to "nC" on page 5.
11/6/2014	<ul style="list-style-type: none"> Added Fig 14 - Typical Avalanche Current vs Pulsewidth on page 5.

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