**HARRIS**
SEMICONDUCTOR

# HGTP12N60C3R, HGT1S12N60C3R, HGT1S12N60C3RS

December 1997

## 24A, 600V, Rugged, UFS Series N-Channel IGBTs

### Features

- **24A, 600V at $T_C = 25^oC$**
- **600V Switching SOA Capability**
- **Typical Fall Time at $T_J = 150^oC$ . . . . . . . . . . . . . . 250ns**
- **Short Circuit Rating at $T_J = 150^oC$ . . . . . . . . . . . . . 10µs**
- **Low Conduction Loss**
- **Related Literature**
  - **TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"**

### Ordering Information

| PART NUMBER | PACKAGE | BRAND |
|---|---|---|
| HGTP12N60C3R | TO-220AB | 12N60C3R |
| HGT1S12N60C3R | TO-262AA | 12N60C3R |
| HGT1S12N60C3RS | TO263AB | 12N60C3R |

NOTE: When ordering, use the entire part number.

### Description

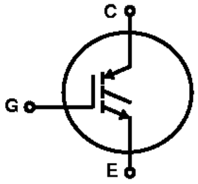
This family of IGBTs was designed for optimum performance in the demanding world of motor control operation as well as other high voltage switching applications. These devices demonstrate RUGGED performance capability when subjected to harsh SHORT CIRCUIT WITHSTAND TIME (SCWT) conditions. The parts have ULTRAFAST (UFS) switching speed while the on-state conduction losses have been kept at a low level.

The electrical specifications include typical Turn-On and Turn-Off dv/dt ratings. These ratings and the Turn-On ratings include the effect of the diode in the test circuit (Figure 15). The data was obtained with the diode at the same $T_J$ as the IGBT under test.

Formerly developmental type TA49118.

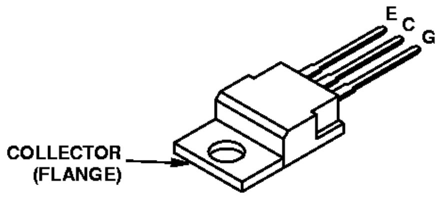
### Terminal Diagram

**N-CHANNEL ENHANCEMENT MODE**

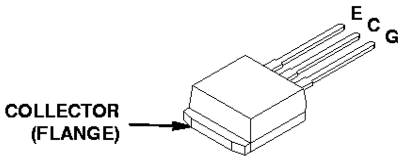


### Packaging

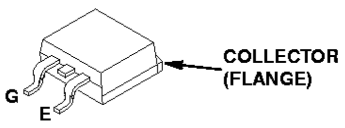
**JEDEC TO-220AB**



**JEDEC TO-262AA**



**JEDEC TO-263AB**



**HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:**

4,364,073 4,417,385 4,430,792 4,443,931 4,466,176 4,516,143 4,532,534 4,567,641
4,587,713 4,598,461 4,605,948 4,618,872 4,620,211 4,631,564 4,639,754 4,639,762
4,641,162 4,644,637 4,682,195 4,684,413 4,694,313 4,717,679 4,743,952 4,783,690
4,794,432 4,801,986 4,803,533 4,809,045 4,809,047 4,810,665 4,823,176 4,837,606
4,860,080 4,883,767 4,888,627 4,890,143 4,901,127 4,904,609 4,933,740 4,963,951
4,969,027

## Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

| | | HGTP12N60C3R,<br>HGT1S12N60C3R,<br>HGT1S12N60C3RS | UNITS |
|---|---|---|---|
| Collector to Emitter Voltage | $BV_{CES}$ | 600 | V |
| Continuous Collector Current | $I_{C25}$ | 24 | A |
| At $T_C = 110^oC$ | $I_{C110}$ | 12 | A |
| Collector Current Pulsed (Note 1) | $I_{CM}$ | 48 | A |
| Gate to Emitter Voltage Continuous | $V_{GES}$ | ±20 | V |
| Gate to Emitter Voltage Pulsed | $V_{GEM}$ | ±30 | V |
| Switching Safe Operating Area at $T_C = 150^oC$ | SSOA | 48A at 600V | |
| Maximum Power Dissipation | $P_D$ | 104 | W |
| Linear Derating Factor | | 0.83 | W/$^o$C |
| Operating and Storage Temperature | $T_J$, $T_{STG}$ | -55 to 150 | $^o$C |
| Maximum Temperature for Soldering | | | |
| Leads at 0.063in (1.6mm) from Case for 10s | $T_L$ | 300 | $^o$C |
| Package Body for 10s, See Techbrief 334 | $T_{pkg}$ | 260 | $^o$C |
| Reverse Voltage Avalanche Energy | $E_{ARV}$ | 100 | mJ |
| Short Circuit Withstand Time (Note 2) at $V_{GE} = 15V$ | $t_{SC}$ | 10 | µs |

*CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $V_{CE} = 440V$, $T_J = 150^oC$, $R_{GE} = 25\Omega$.

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## Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Collector to Emitter Breakdown Voltage | $BV_{CES}$ | $I_C = 250\mu A$, $V_{GE} = 0V$ | | 600 | - | - | V |
| Emitter to Collector Breakdown Voltage | $BV_{ECS}$ | $I_C = 10mA$, $V_{GE} = 0V$ | | 20 | 23 | - | V |
| Collector to Emitter Leakage Current | $I_{CES}$ | $V_{CE} = BV_{CES}$ | $T_C = 25^oC$ | - | - | 250 | µA |
| | | | $T_C = 150^oC$ | - | - | 1.0 | mA |
| Collector to Emitter Saturation Voltage | $V_{CE(SAT)}$ | $I_C = I_{C110}$,<br>$V_{GE} = 15V$ | $T_C = 25^oC$ | - | 1.9 | 2.2 | V |
| | | | $T_C = 150^oC$ | - | 2.0 | 2.5 | V |
| Gate to Emitter Threshold Voltage | $V_{GE(TH)}$ | $I_C = 250\mu A$, $V_{CE} = V_{GE}$ | | 4.5 | 6.1 | 7.5 | V |
| Gate to Emitter Leakage Current | $I_{GES}$ | $V_{GE} = \pm 20V$ | | - | - | ±100 | nA |
| Switching SOA (See Figure 2) | SSOA | $T_J = 150^oC$, $R_G = 25\Omega$, $V_{GE} = 15V$,<br>$V_{CE} = 600V$, $L = 100\mu H$ | | 48 | - | - | A |
| Gate to Emitter Plateau Voltage | $V_{GEP}$ | $I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$ | | - | 9.7 | - | V |
| On-State Gate Charge | $Q_{g(ON)}$ | $I_C = I_{C110}$,<br>$V_{CE} = 0.5\ BV_{ES}$ | $V_{GE} = 15V$ | - | 50 | 70 | nC |
| | | | $V_{GE} = 20V$ | - | 71 | 90 | nC |
| Current Turn-On Delay Time | $t_{d(ON)I}$ | $T_J = 25^oC$, $I_{CE} = I_{C110}$,<br>$V_{CE} = 0.8\ BV_{CES}$,<br>$V_{GE} = 15V$, $R_G = 25\Omega$,<br>$L = 1mH$<br>Diode Used in Test Circuit<br>RURP1560 at $25^oC$ | | - | 37 | - | ns |
| Current Rise Time | $t_{rI}$ | | | - | 37 | - | ns |
| Current Turn-Off Delay Time | $t_{d(OFF)I}$ | | | - | 120 | 240 | ns |
| Current Fall Time | $t_{fI}$ | | | - | 110 | 160 | ns |
| Turn-On Energy (Note 4) | $E_{ON}$ | | | - | 400 | 750 | µJ |
| Turn-Off Energy (Note 5) | $E_{OFF}$ | | | - | 340 | 750 | µJ |

**Electrical Specifications** $T_C = 25^oC$, Unless Otherwise Specified **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Current Turn-On Delay Time | $t_{d(ON)I}$ | $T_J = 150^oC$<br>$I_{CE} = I_{C110}$<br>$V_{CE} = 0.8\ BV_{CES}$<br>$V_{GE} = 15V$<br>$R_G = 25\Omega$<br>$L = 1mH$<br>Diode Used in Test Circuit RURP1560 at 150°C | - | 36 | - | ns |
| Current Rise Time | $t_{rI}$ | | - | 38 | - | ns |
| Current Turn-Off Delay Time | $t_{d(OFF)I}$ | | - | 290 | 500 | ns |
| Current Fall Time | $t_{fI}$ | | - | 250 | 400 | ns |
| Turn-Off Voltage dv/dt (Note 3) | $dV_{CE}/dt$ | | - | 2 | - | V/ns |
| Turn-On Voltage dv/dt (Note 3) | $dV_{CE}/dt$ | | - | 10 | - | V/ns |
| Turn-On Energy (Note 4) | $E_{ON}$ | | - | 0.83 | - | mJ |
| Turn-Off Energy (Note 5) | $E_{OFF}$ | | - | 1.20 | - | mJ |
| Thermal Resistance Junction to Case | $R_{\theta JC}$ | | - | - | 1.2 | °C/W |

NOTES:

3. $dV_{CE}/dt$ depends on the diode used and the temperature of the diode.
4. Turn-On Energy Loss ($E_{ON}$) includes losses due to the diode recovery and is defined as the integral of the instantaneous power loss starting at the leading edge of the input pulse and ending at the point where the collector voltage equals $V_{CE}(ON)$. This value of $E_{ON}$ was obtained with a RURP1560 diode at $T_J = 150^oC$. A different diode or temperature will result in a different $E_{ON}$. For example with diode at $T_J = 25^oC$, $E_{ON}$ is about one half the value of $E_{ON}$ with diode at $T_J = 150^oC$.
5. Turn-Off Energy Loss ($E_{OFF}$) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$). All devices were tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss.

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## *Typical Performance Curves*

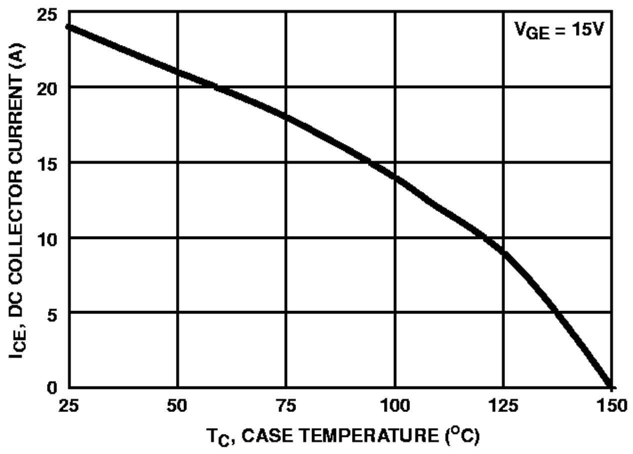

FIGURE 1. DC COLLECTOR CURRENT vs CASE TEMPERATURE

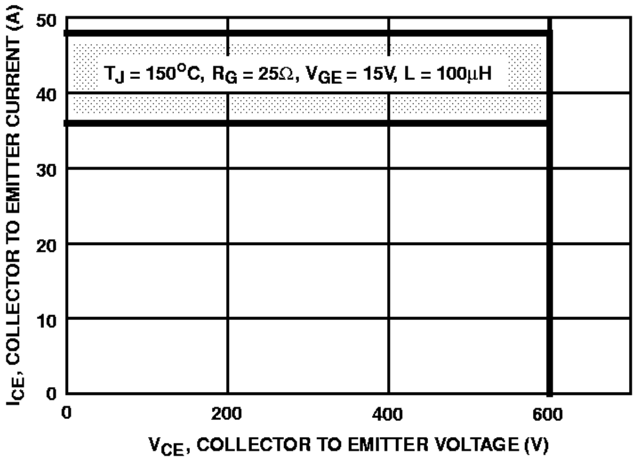

FIGURE 2. SWITCHING SAFE OPERATING AREAS

## *Typical Performance Curves* (Continued)

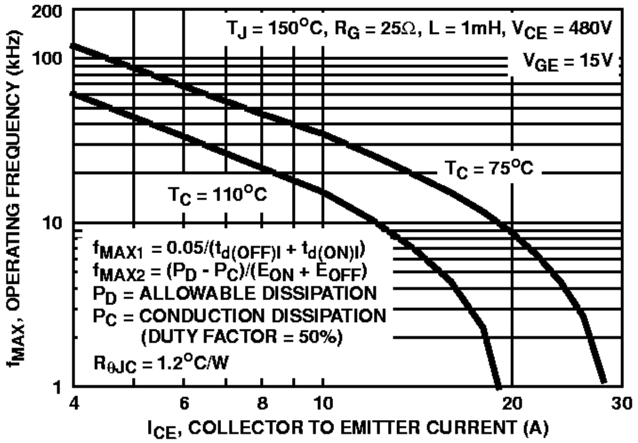

FIGURE 3. OPERATING FREQUENCY vs COLLECTOR TO EMITTER CURRENT

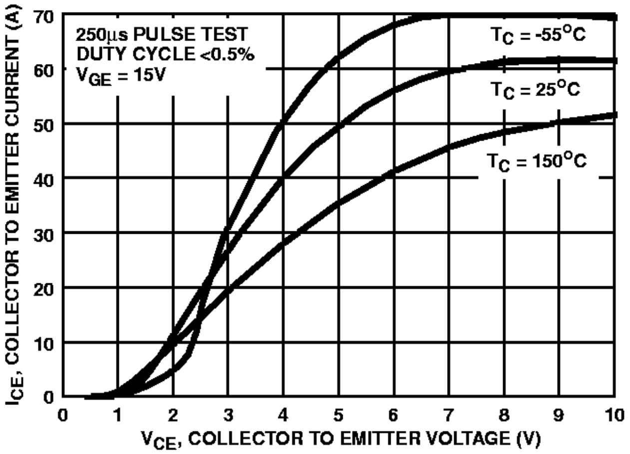

FIGURE 4. COLLECTOR TO EMITTER ON STATE VOLTAGE

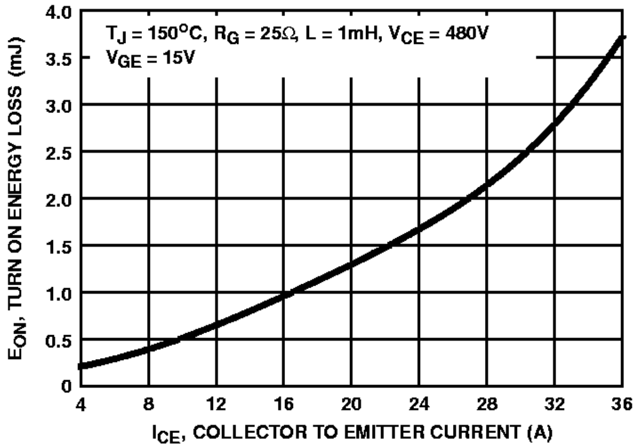

FIGURE 5. TURN ON ENERGY LOSS vs COLLECTOR TO EMITTER CURRENT

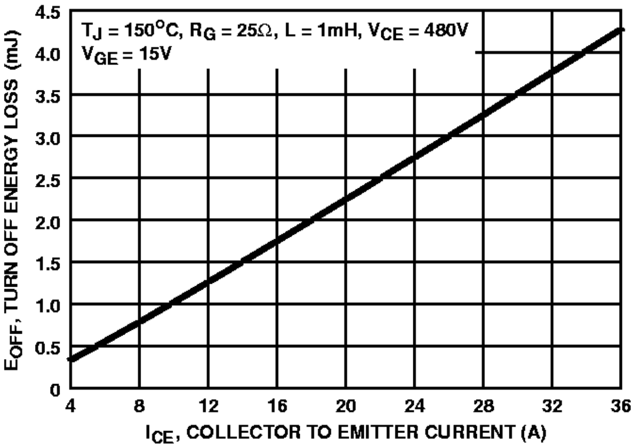

FIGURE 6. TURN OFF ENERGY LOSS vs COLLECTOR TO EMITTER CURRENT

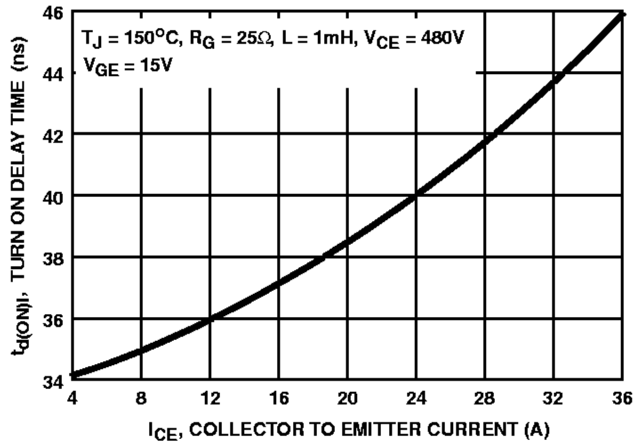

FIGURE 7. TURN ON DELAY TIME vs COLLECTOR TO EMITTER CURRENT

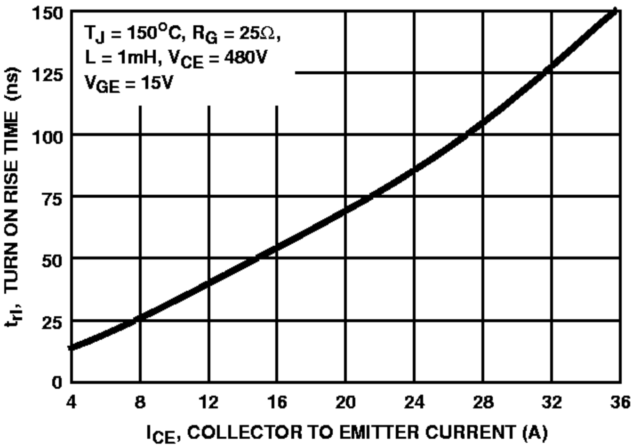

FIGURE 8. TURN ON RISE TIME vs COLLECTOR TO EMITTER CURRENT

## Typical Performance Curves (Continued)

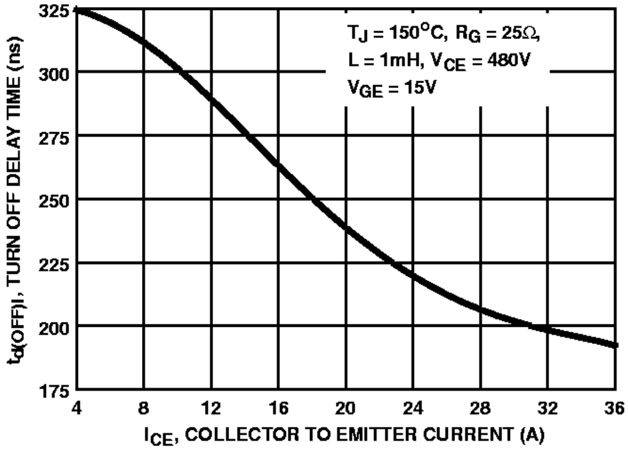

FIGURE 9. TURN OFF DELAY TIME vs COLLECTOR TO EMITTER CURRENT

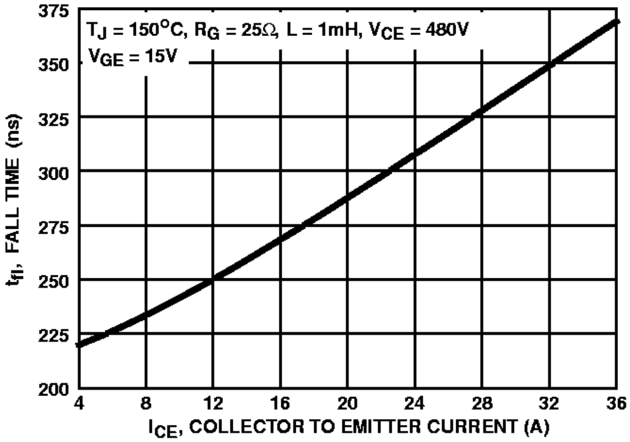

FIGURE 10. TURN OFF FALL TIME vs COLLECTOR TO EMITTER CURRENT

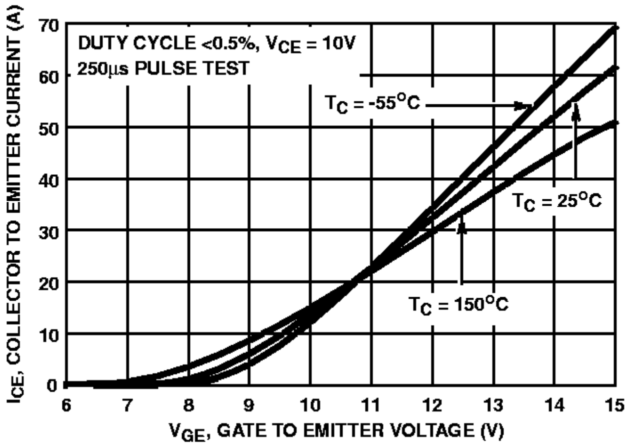

FIGURE 11. TRANSFER CHARACTERISTICS

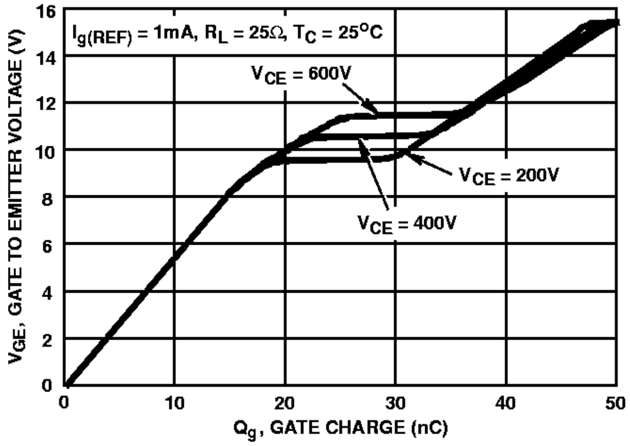

FIGURE 12. GATE CHARGE WAVEFORMS

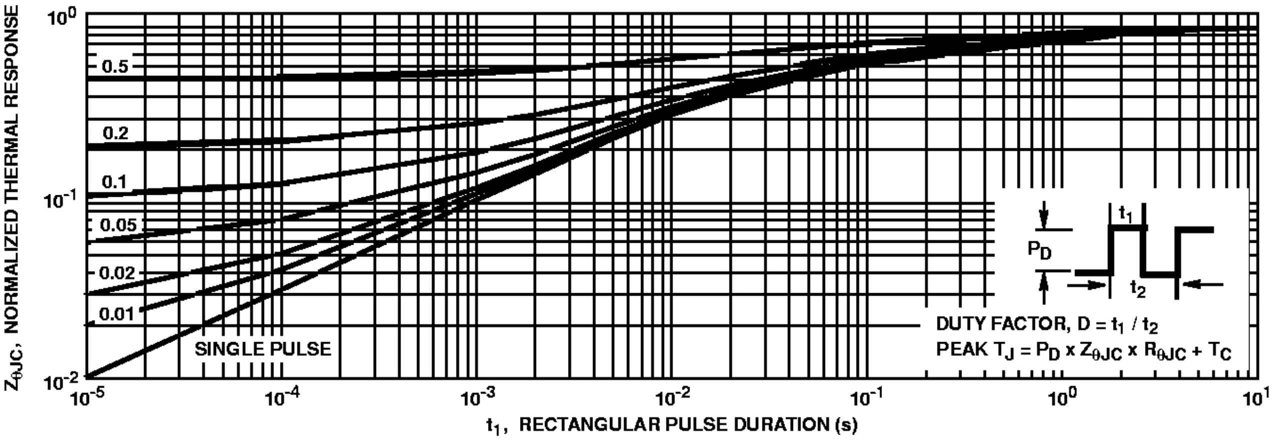

FIGURE 13. IGBT NORMALIZED TRANSIENT THERMAL RESPONSE, JUNCTION TO CASE

## *Typical Performance Curves* (Continued)

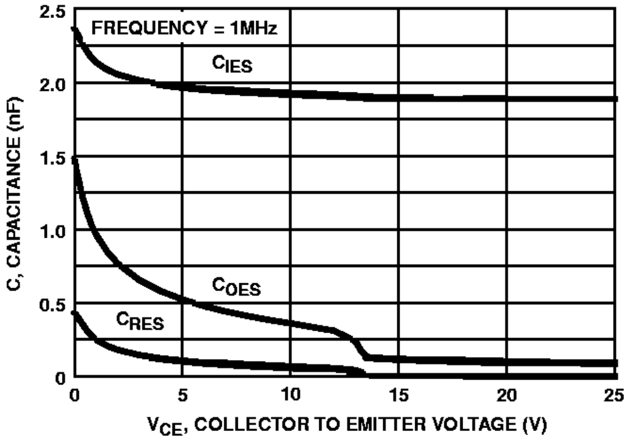

FIGURE 14. CAPACITANCE vs COLLECTOR TO EMITTER VOLTAGE

## *Test Circuit and Waveforms*

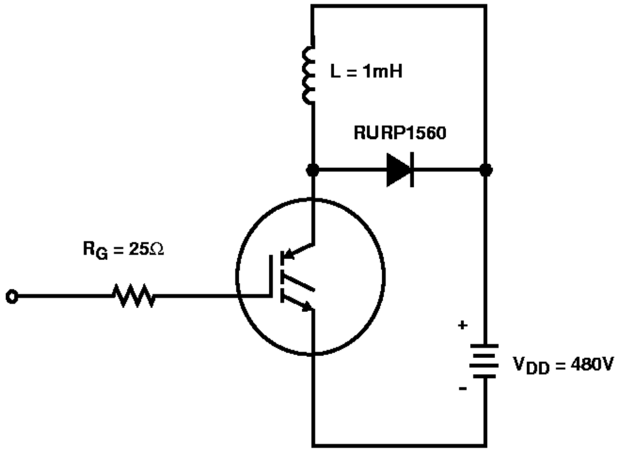

FIGURE 15. INDUCTIVE SWITCHING TEST CIRCUIT

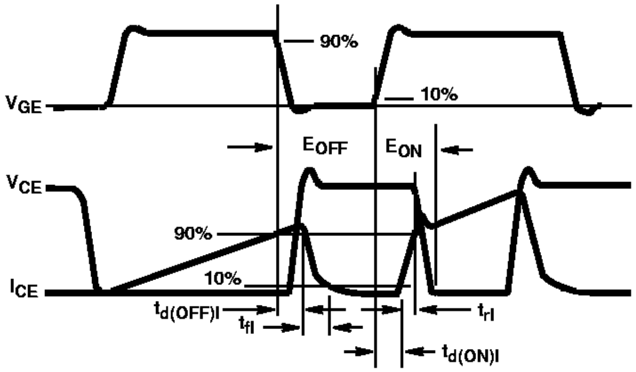

FIGURE 16. SWITCHING TEST WAVEFORMS

## Handling Precautions for IGBTs

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBTs are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBTs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "ECCOSORBD™ LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of $V_{GEM}$. Exceeding the rated $V_{GE}$ can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic zener diode from gate to emitter. If gate protection is required an external zener is recommended.

## Operating Frequency Information

Operating frequency information for a typical device (Figure 3) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current ($I_{CE}$) plots are possible using the information shown for a typical unit in Figures 4, 5, 6, 7 and 9. The operating frequency plot (Figure 3) of a typical device shows $f_{MAX1}$ or $f_{MAX2}$ whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

$f_{MAX1}$ is defined by $f_{MAX1} = 0.05/(t_{D(OFF)I} + t_{D(ON)I})$. Deadtime (the denominator) has been arbitrarily held to 10% of the on- state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ and $t_{D(ON)I}$ are defined in Figure 16. Device turn-off delay can establish an additional frequency limiting condition for an application other than $T_{JMAX}$. $t_{D(OFF)}$ is important when controlling output ripple under a lightly loaded condition.

$f_{MAX2}$ is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON})$. The allowable dissipation ($P_D$) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed $P_D$. A 50% duty factor was used (Figure 3) and the conduction losses ($P_C$) are approximated by $P_C = (V_{CE} \times I_{CE})/2$.

$E_{ON}$ and $E_{OFF}$ are defined in the switching waveforms shown in Figure 16. $E_{ON}$ is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-on and $E_{OFF}$ is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-off. All tail losses are included in the calculation for $E_{OFF}$; i.e. the collector current equals zero ($I_{CE} = 0$).

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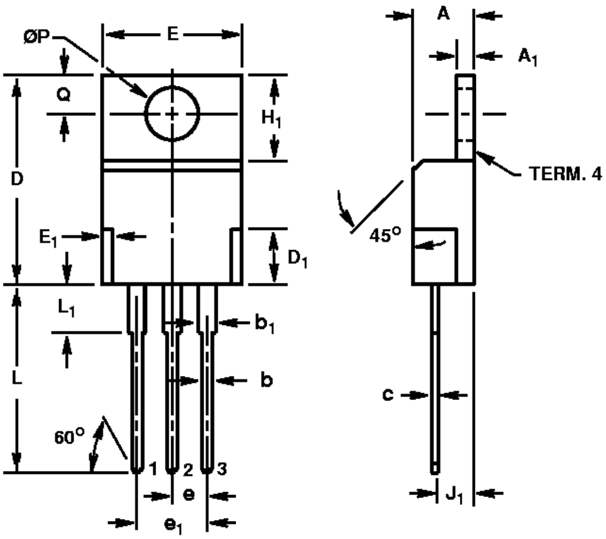
## *TO-220AB*

**3 LEAD JEDEC TO-220AB PLASTIC PACKAGE**



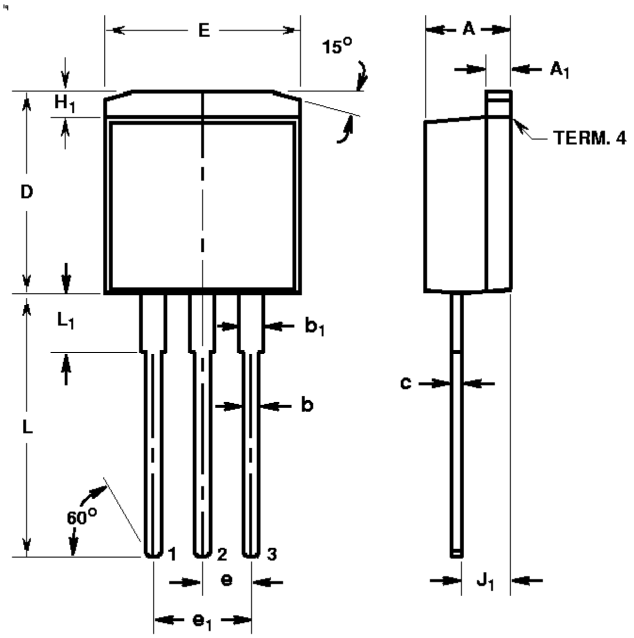
**LEAD 1 - GATE**
**LEAD 2 - COLLECTOR**
**LEAD 3 - EMITTER**
**TERM. 4 - COLLECTOR**

| **SYMBOL** | **INCHES** | | **MILLIMETERS** | | **NOTES** |
|---|---|---|---|---|---|
| | **MIN** | **MAX** | **MIN** | **MAX** | |
| A | 0.170 | 0.180 | 4.32 | 4.57 | - |
| $A_1$ | 0.048 | 0.052 | 1.22 | 1.32 | - |
| b | 0.030 | 0.034 | 0.77 | 0.86 | 3, 4 |
| $b_1$ | 0.045 | 0.055 | 1.15 | 1.39 | 2, 3 |
| c | 0.014 | 0.019 | 0.36 | 0.48 | 2, 3, 4 |
| D | 0.590 | 0.610 | 14.99 | 15.49 | - |
| $D_1$ | - | 0.160 | - | 4.06 | - |
| E | 0.395 | 0.410 | 10.04 | 10.41 | - |
| $E_1$ | - | 0.030 | - | 0.76 | - |
| e | 0.100 TYP | | 2.54 TYP | | 5 |
| $e_1$ | 0.200 BSC | | 5.08 BSC | | 5 |
| $H_1$ | 0.235 | 0.255 | 5.97 | 6.47 | - |
| $J_1$ | 0.100 | 0.110 | 2.54 | 2.79 | 6 |
| L | 0.530 | 0.550 | 13.47 | 13.97 | - |
| $L_1$ | 0.130 | 0.150 | 3.31 | 3.81 | 2 |
| ØP | 0.149 | 0.153 | 3.79 | 3.88 | - |
| Q | 0.102 | 0.112 | 2.60 | 2.84 | - |

NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Lead dimension and finish uncontrolled in $L_1$.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 2 dated 7-97.

## *TO-262AA* 3 LEAD JEDEC TO-262AA PLASTIC PACKAGE



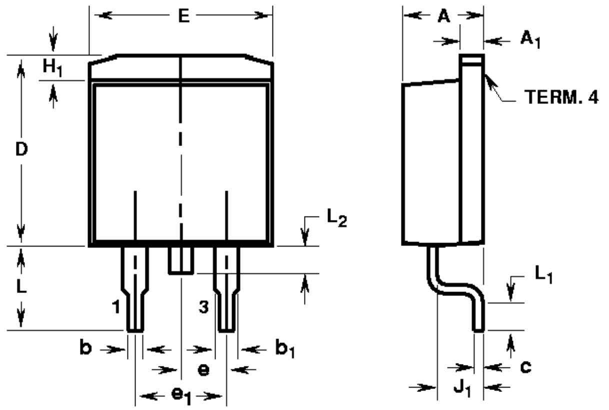
**LEAD 1 - GATE**
**LEAD 2 - COLLECTOR**
**LEAD 3 - EMITTER**
**TERM. 4 - COLLECTOR**

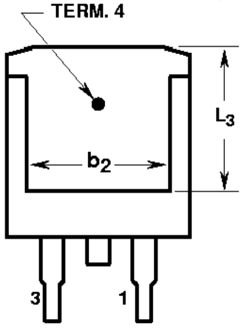
| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | 0.170 | 0.180 | 4.32 | 4.57 | - |
| $A_1$ | 0.048 | 0.052 | 1.22 | 1.32 | 3, 4 |
| b | 0.030 | 0.034 | 0.77 | 0.86 | 3, 4 |
| $b_1$ | 0.045 | 0.055 | 1.15 | 1.39 | 3, 4 |
| c | 0.018 | 0.022 | 0.46 | 0.55 | 3, 4 |
| D | 0.405 | 0.425 | 10.29 | 10.79 | - |
| E | 0.395 | 0.405 | 10.04 | 10.28 | - |
| e | 0.100 TYP | | 2.54 TYP | | 5 |
| $e_1$ | 0.200 BSC | | 5.08 BSC | | 5 |
| $H_1$ | 0.045 | 0.055 | 1.15 | 1.39 | - |
| $J_1$ | 0.095 | 0.105 | 2.42 | 2.66 | 6 |
| L | 0.530 | 0.550 | 13.47 | 13.97 | - |
| $L_1$ | 0.110 | 0.130 | 2.80 | 3.30 | 2 |

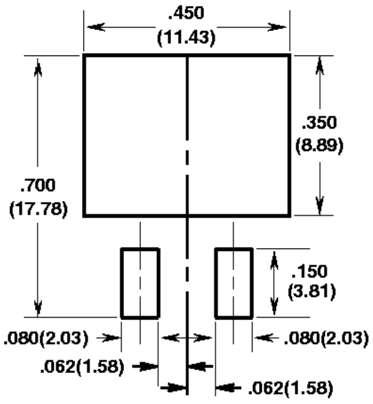
NOTES:

1. These dimensions are within allowable dimensions of Rev. A of JEDEC TO-262AA outline dated 6-90.
2. Solder finish uncontrolled in this area.
3. Dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder plating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 5 dated 7-97.

## *TO-263AB* SURFACE MOUNT JEDEC TO-263AB PLASTIC PACKAGE







**MINIMUM PAD SIZE RECOMMENDED FOR SURFACE-MOUNTED APPLICATIONS**

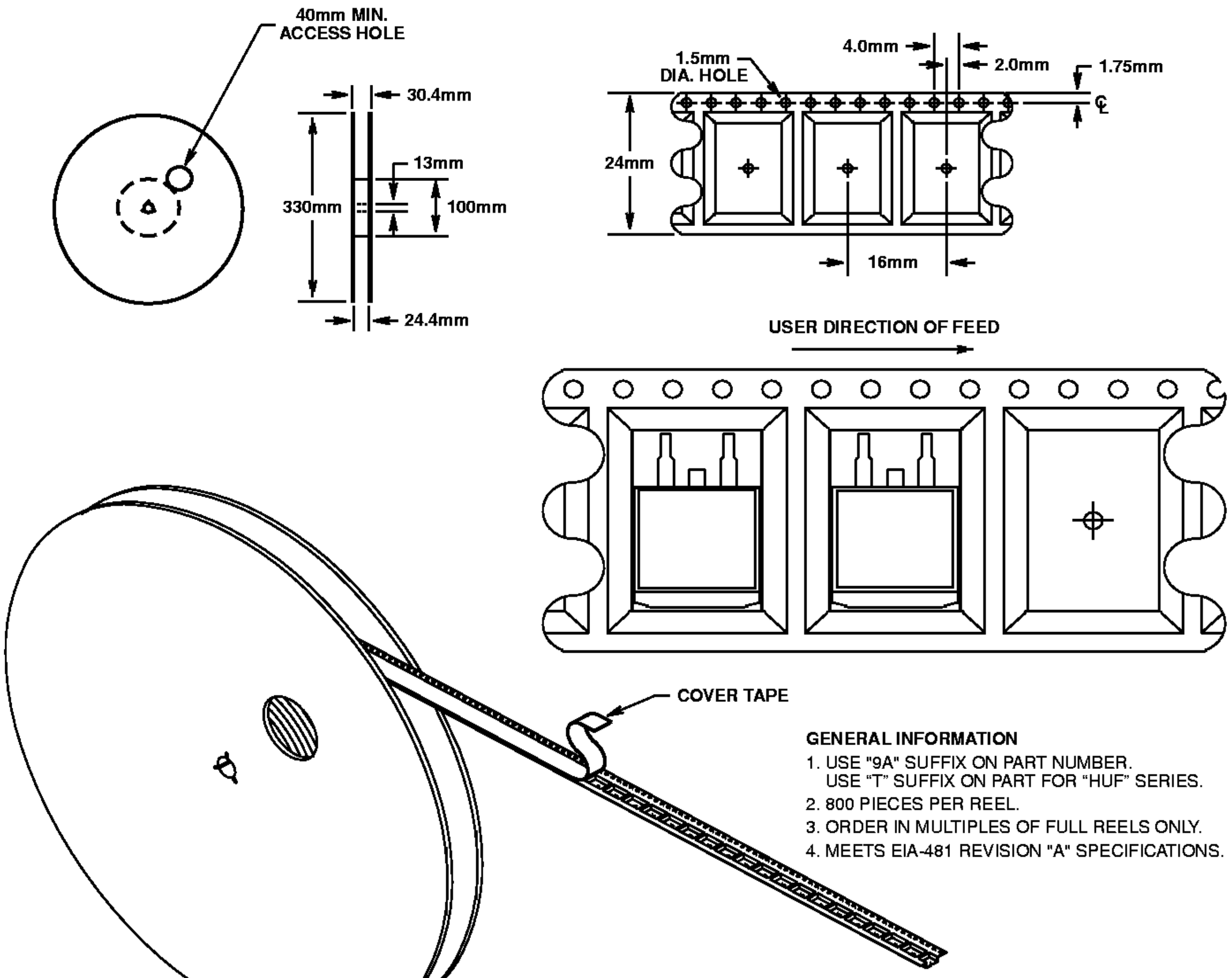
| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | 0.170 | 0.180 | 4.32 | 4.57 | - |
| $A_1$ | 0.048 | 0.052 | 1.22 | 1.32 | 4, 5 |
| b | 0.030 | 0.034 | 0.77 | 0.86 | 4, 5 |
| $b_1$ | 0.045 | 0.055 | 1.15 | 1.39 | 4, 5 |
| $b_2$ | 0.310 | - | 7.88 | - | 2 |
| c | 0.018 | 0.022 | 0.46 | 0.55 | 4, 5 |
| D | 0.405 | 0.425 | 10.29 | 10.79 | - |
| E | 0.395 | 0.405 | 10.04 | 10.28 | - |
| e | 0.100 TYP | | 2.54 TYP | | 7 |
| $e_1$ | 0.200 BSC | | 5.08 BSC | | 7 |
| $H_1$ | 0.045 | 0.055 | 1.15 | 1.39 | - |
| $J_1$ | 0.095 | 0.105 | 2.42 | 2.66 | - |
| L | 0.175 | 0.195 | 4.45 | 4.95 | - |
| $L_1$ | 0.090 | 0.110 | 2.29 | 2.79 | 4, 6 |
| $L_2$ | 0.050 | 0.070 | 1.27 | 1.77 | 3 |
| $L_3$ | 0.315 | - | 8.01 | - | 2 |

NOTES:

1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-263AB outline dated 2-92.
2. $L_3$ and $b_2$ dimensions established a minimum mounting surface for terminal 4.
3. Solder finish uncontrolled in this area.
4. Dimension (without solder).
5. Add typically 0.002 inches (0.05mm) for solder plating.
6. $L_1$ is the terminal length for soldering.
7. Position of lead to be measured 0.120 inches (3.05mm) from bottom of dimension D.
8. Controlling dimension: Inch.
9. Revision 8 dated 7-97.

## *TO-263AB*

**24mm TAPE AND REEL**



**GENERAL INFORMATION**

1. USE "9A" SUFFIX ON PART NUMBER.
   USE "T" SUFFIX ON PART FOR "HUF" SERIES.
2. 800 PIECES PER REEL.
3. ORDER IN MULTIPLES OF FULL REELS ONLY.
4. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

Revision 8 dated 7-97

All Harris Semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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