FAIRCHILD SEMICONDUCTOR TM

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Si4463DY

P-Channel 2.5V Specified PowerTrench® MOSFET

General Description

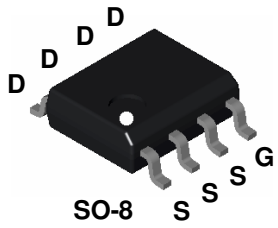
This P-Channel 2.5V specified MOSFET uses a rugged gate PowerTrench process. It has been optimized for power management applications with a wide range of gate drive voltage (2.5V – 12V).

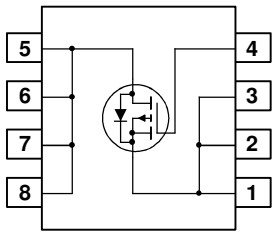
Applications

- Power management
- Load switch
- Battery protection

Features

- –11.5 A, –20 V. $R_{DS(ON)}$ = 12 mΩ @ V_{GS} = –4.5 V
  $R_{DS(ON)}$ = 17.5 mΩ @ V_{GS} = –2.5 V
- Fast switching speed.
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		–20	V
V_{GSS}	Gate-Source Voltage		± 12	V
I_D	Drain Current – Continuous	(Note 1a)	–11.5	A
	– Pulsed		–50	
P_D	Power Dissipation for Single Operation	(Note 1a)	2.5	W
		(Note 1b)	1.2	
		(Note 1c)	1.0	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	25	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
4463	Si4463DY	13''	12mm	2500 units

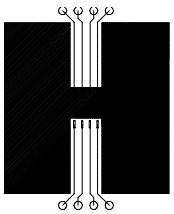
Electrical Characteristics

T_A = 25°C unless otherwise noted

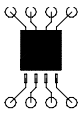
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = –250 µA	–20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = –250 µA, Referenced to 25°C		–12		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –16 V, V_{GS} = 0 V			–1	µA
I_{GSSF}	Gate–Body Leakage, Forward	V_{GS} = 12 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate–Body Leakage, Reverse	V_{GS} = –12 V, V_{DS} = 0 V			–100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = –250 µA	–0.6	–0.8	–1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = –250 µA, Referenced to 25°C		3		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = –4.5 V, I_D = –11.5 A V_{GS} = –2.5 V, I_D = –9.5 A V_{GS}= –4.5 V, I_D = –11.5A, T_J=125°C		10 14 13	12 17.5 18	mΩ
$I_{D(on)}$	On–State Drain Current	V_{GS} = –4.5 V, V_{DS} = –5 V	–50			A
g_{FS}	Forward Transconductance	V_{DS} = –10 V, I_D = –10 A		49		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = –10 V, V_{GS} = 0 V, f = 1.0 MHz		4481		pF
C_{oss}	Output Capacitance			1532		pF
C_{rss}	Reverse Transfer Capacitance			540		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = –5 V, I_D = –1 A, V_{GS} = –4.5 V, R_{GEN} = 6 Ω		15	30	ns
t_r	Turn–On Rise Time			15	30	ns
$t_{d(off)}$	Turn–Off Delay Time			120	240	ns
t_f	Turn–Off Fall Time			60	120	ns
Q_g	Total Gate Charge	V_{DS} = –10 V, I_D = –11.5 A, V_{GS} = –4.5 V		41	60	nC
Q_{gs}	Gate–Source Charge			6.4		nC
Q_{gd}	Gate–Drain Charge			11.8		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				–2.1	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = –1.5 A (Note 2)		–0.65	–1.2	V

Notes:

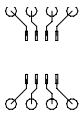
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50°/W when mounted on a 1in^2 pad of 2 oz copper



b) 105°/W when mounted on a .04 in^2 pad of 2 oz copper



c) 125°/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

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