

## 74F283 4-Bit Binary Full Adder with Fast Carry

### General Description

The 'F283 high-speed 4-bit binary full adder with internal carry lookahead accepts two 4-bit binary words ( $A_0$ – $A_3$ ,  $B_0$ – $B_3$ ) and a Carry input ( $C_0$ ). It generates the binary Sum outputs ( $S_0$ – $S_3$ ) and the Carry output ( $C_4$ ) from the most significant bit. The 'F283 will operate with either active HIGH or active LOW operands (positive or negative logic).

### Features

- Guaranteed 4000V minimum ESD protection

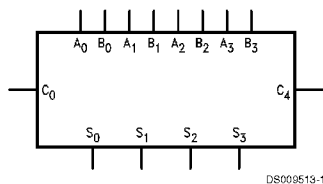
### Ordering Code:

Commercial	Military	Package Number	Package Description
74F283PC		N16E	16-Lead (0.300" Wide) Molded Dual-In-Line
	54F283DM (Note 2)	J16A	16-Lead Ceramic Dual-In-Line
74F283SC (Note 1)		M16A	16-Lead (0.150" Wide) Molded Small Outline, JEDEC
74F283SJ (Note 1)		M16D	16-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F283FM (Note 2)	W16A	16-Lead Cerpack
	54F283LL (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

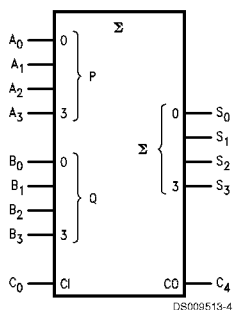
**Note 1:** Devices also available in 13" reel. Use suffix = SCX and SJX.

**Note 2:** Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

### Logic Symbols

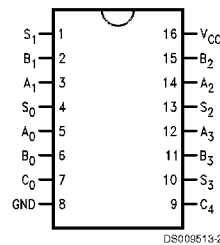


#### IEEE/IEC

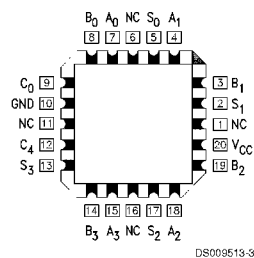


### Connection Diagrams

#### Pin Assignment for DIP, SOIC and Flatpak



#### Pin Assignment for LCC



## Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L.	Input I <sub>H</sub> /I <sub>IL</sub>
		HIGH/LOW	Output I <sub>OH</sub> /I <sub>OL</sub>
A <sub>0</sub> -A <sub>3</sub>	A Operand Inputs	1.0/2.0	20 μA/-1.2 mA
B <sub>0</sub> -B <sub>3</sub>	B Operand Inputs	1.0/2.0	20 μA/-1.2 mA
C <sub>0</sub>	Carry Input	1.0/1.0	20 μA/-0.6 mA
S <sub>0</sub> -S <sub>3</sub>	Sum Outputs	50/33.3	-1 mA/20 mA
C <sub>4</sub>	Carry Output	50/33.3	-1 mA/20 mA

## Functional Description

The 'F283 adds two 4-bit binary words (A plus B) plus the incoming Carry (C<sub>0</sub>). The binary sum appears on the Sum (S<sub>0</sub>-S<sub>3</sub>) and outgoing carry (C<sub>4</sub>) outputs. The binary weight of the various inputs and outputs is indicated by the subscript numbers, representing powers of two.

$$2^0 (A_0 + B_0 + C_0) + 2^1 (A_1 + B_1) + 2^2 (A_2 + B_2) + 2^3 (A_3 + B_3) = S_0 + 2S_1 + 4S_2 + 8S_3 + 16C_4$$

Where (+) = plus

Interchanging inputs of equal weight does not affect the operation. Thus C<sub>0</sub>, A<sub>0</sub>, B<sub>0</sub> can be arbitrarily assigned to pins 5, 6 and 7 for DIPs, and 7, 8 and 9 for chip carrier packages. Due to the symmetry of the binary add function, the 'F283 can be used either with all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). See Figure 1. Note that if C<sub>0</sub> is not used it must be tied LOW for active HIGH logic or tied HIGH for active LOW logic.

Due to pin limitations, the intermediate carries of the 'F283 are not brought out for use as inputs or outputs. However,

other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage. Figure 2 shows how to make a 3-bit adder. Tying the operand inputs of the fourth adder (A<sub>3</sub>, B<sub>3</sub>) LOW makes S<sub>3</sub> dependent only on, and equal to, the carry from the third adder. Using somewhat the same principle, Figure 3 shows a way of dividing the 'F283 into a 2-bit and a 1-bit adder. The third stage adder (A<sub>2</sub>, B<sub>2</sub>, S<sub>2</sub>) is used merely as a means of getting a carry (C<sub>10</sub>) signal into the fourth stage (via A<sub>2</sub> and B<sub>2</sub>) and bringing out the carry from the second stage on S<sub>2</sub>. Note that as long as A<sub>2</sub> and B<sub>2</sub> are the same, whether HIGH or LOW, they do not influence S<sub>2</sub>. Similarly, when A<sub>2</sub> and B<sub>2</sub> are the same the carry into the third stage does not influence the carry out of the third stage. Figure 4 shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs S<sub>0</sub>, S<sub>1</sub> and S<sub>2</sub> present a binary number equal to the number of inputs I<sub>1</sub>-I<sub>5</sub> that are true. Figure 5 shows one method of implementing a 5-input majority gate. When three or more of the inputs I<sub>1</sub>-I<sub>5</sub> are true, the output M<sub>5</sub> is true.

	C <sub>0</sub>	A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	B <sub>0</sub>	B <sub>1</sub>	B <sub>2</sub>	B <sub>3</sub>	S <sub>0</sub>	S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	C <sub>4</sub>
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

Active HIGH: 0 + 10 + 9 = 3 + 16    Active LOW: 1 + 5 + 6 = 12 + 0

FIGURE 1. Active HIGH versus Active LOW Interpretation

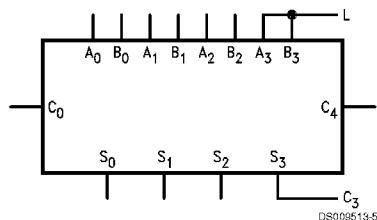


FIGURE 2. 3-Bit Adder

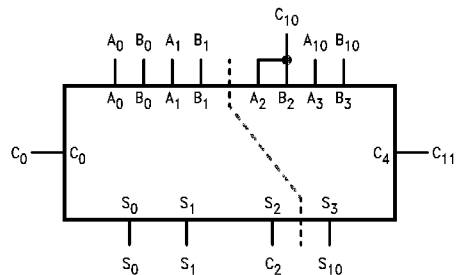
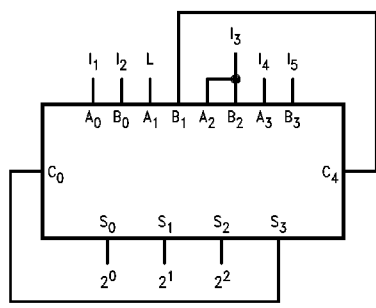


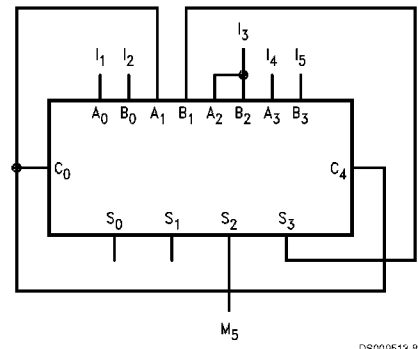
FIGURE 3. 2-Bit and 1-Bit Adders

**Functional Description** (Continued)



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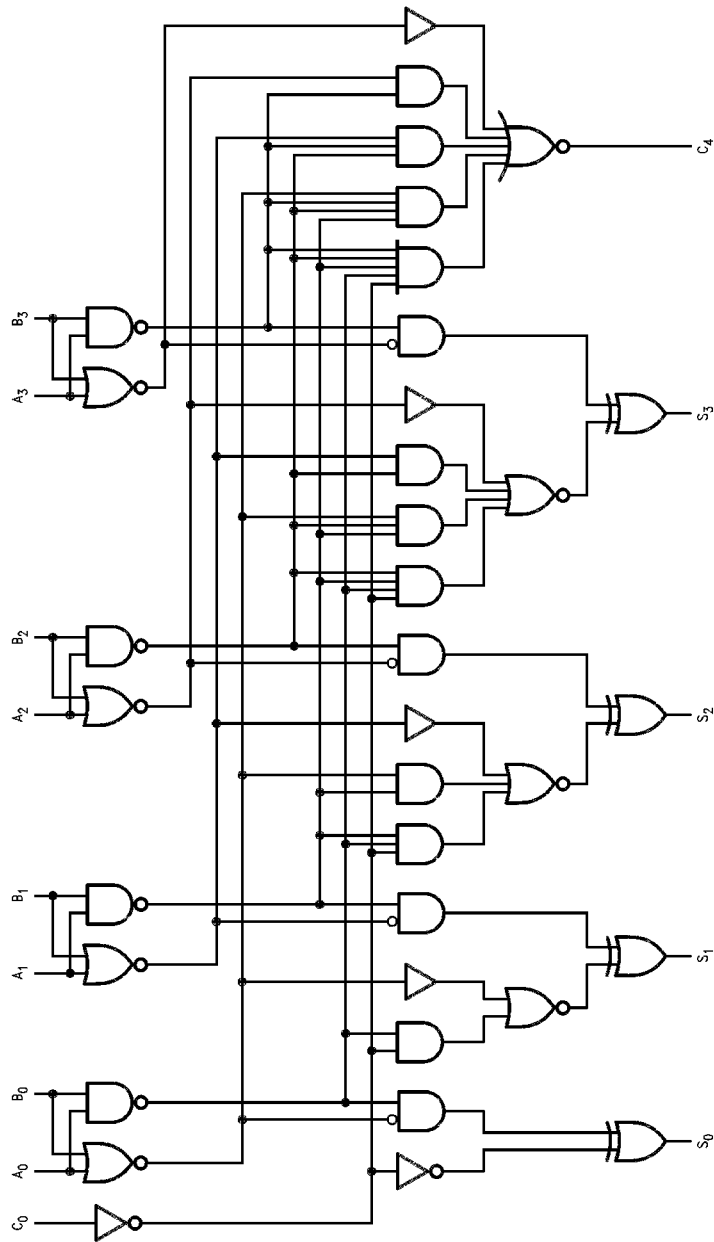
**FIGURE 4. 5-Input Encoder**



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**FIGURE 5. 5-Input Majority Gate**

# Logic Diagram



DS000513-9

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 3)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 4)	-0.5V to +7.0V
Input Current (Note 4)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

ESD Last Passing Voltage (Min)

4000V

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**Note 3:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 4:** Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

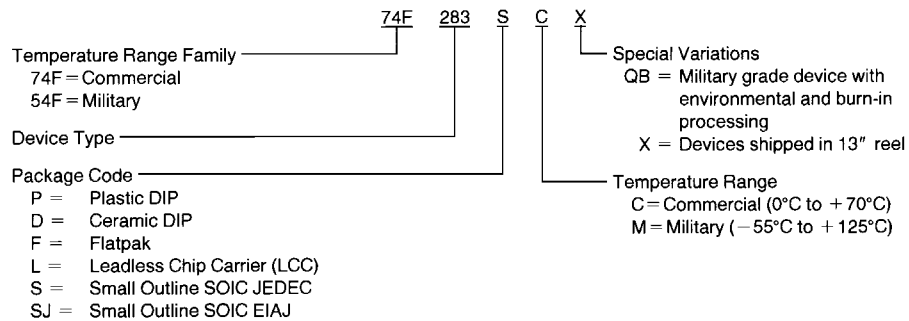
Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions	
		Min	Typ	Max				
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal	
V <sub>IL</sub>	Input LOW Voltage	0.8			V		Recognized as a LOW Signal	
V <sub>CD</sub>	Input Clamp Diode Voltage	-1.2			V	Min	I <sub>IN</sub> = -18 mA	
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA	
		74F 10% V <sub>CC</sub>	2.5					
		74F 5% V <sub>CC</sub>	2.7					
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>	0.5		V	Min	I <sub>OL</sub> = 20 mA	
		74F 10% V <sub>CC</sub>	0.5					
I <sub>IH</sub>	Input HIGH Current	54F	20.0		μA	Max	V <sub>IN</sub> = 2.7V	
		74F	5.0					
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F	100		μA	Max	V <sub>IN</sub> = 7.0V	
		74F	7.0					
I <sub>CEX</sub>	Output HIGH Leakage Current	54F	250		μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>	
		74F	50					
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded	
I <sub>OD</sub>	Output Leakage Circuit Current	74F	3.75		μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded	
I <sub>IL</sub>	Input LOW Current	-0.6			mA	Max	V <sub>IN</sub> = 0.5V (C <sub>O</sub> ) V <sub>IN</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> )	
		-1.2						
I <sub>OS</sub>	Output Short-Circuit Current	-60			-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current	36			55	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current	36			55	mA	Max	V <sub>O</sub> = LOW

## AC Electrical Characteristics:

Symbol	Parameter	74F			54F		74F		Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	Min	Max	
$t_{PLH}$	Propagation Delay	3.5	7.0	9.5	3.5	14.0	3.5	11.0	ns
$t_{PHL}$	$C_0$ to $S_n$	3.0	7.0	9.5	3.0	14.0	3.0	11.0	
$t_{PLH}$	Propagation Delay	3.0	7.0	9.5	3.0	17.0	3.0	13.0	ns
$t_{PHL}$	$A_n$ or $B_n$ to $S_n$	3.0	7.0	9.5	3.0	14.0	3.0	11.5	
$t_{PLH}$	Propagation Delay	3.0	5.7	7.5	3.0	10.5	3.0	8.5	ns
$t_{PHL}$	$C_0$ to $C_4$	3.0	5.4	7.0	2.5	10.0	3.0	8.0	
$t_{PLH}$	Propagation Delay	3.0	5.7	7.5	3.0	10.5	3.0	8.5	ns
$t_{PHL}$	$A_n$ or $B_n$ to $C_4$	2.5	5.3	7.0	2.5	10.0	2.5	8.0	

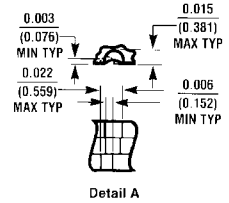
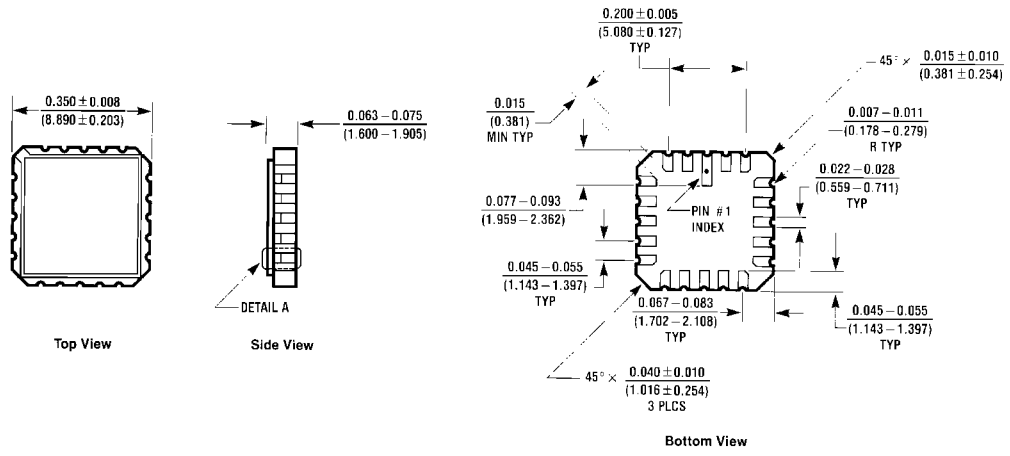
## Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



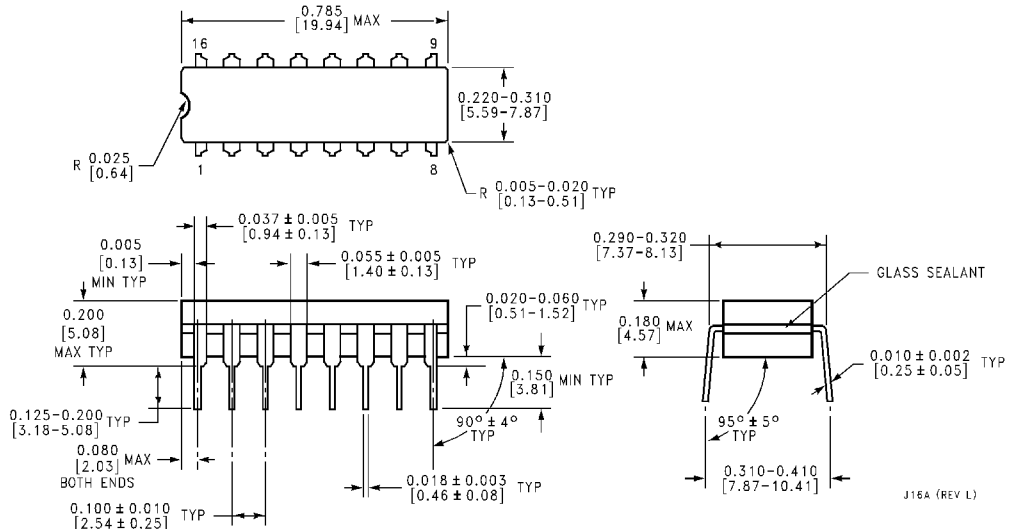
DS009513-10

**Physical Dimensions** inches (millimeters) unless otherwise noted



**20-Lead Ceramic Leadless Chip Carrier (L)  
 Package Number E20A**

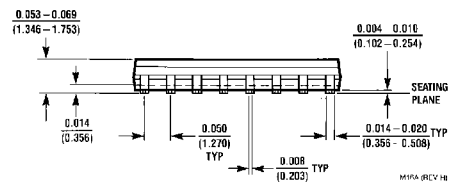
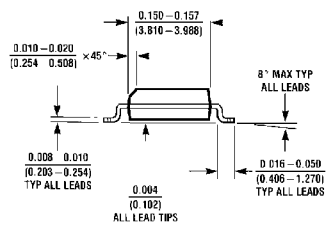
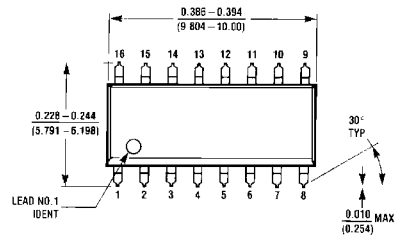
E20A (REV D)



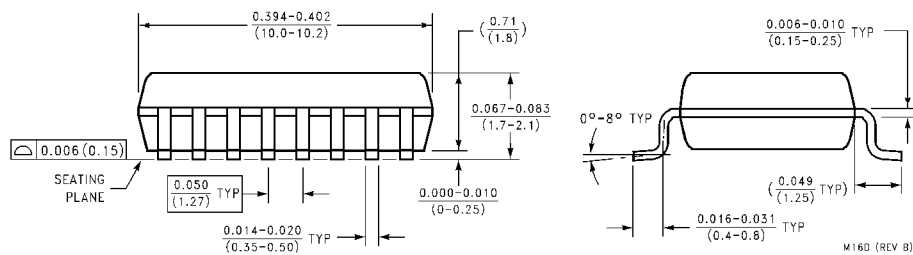
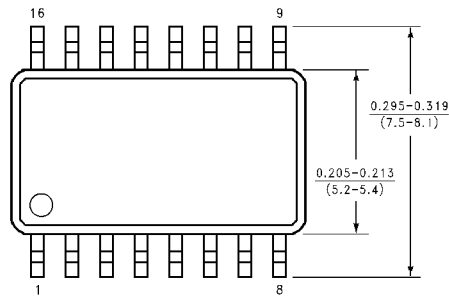
**16-Lead Ceramic Dual-In-Line Package (D)  
 Package Number J16A**

J16A (REV L)

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



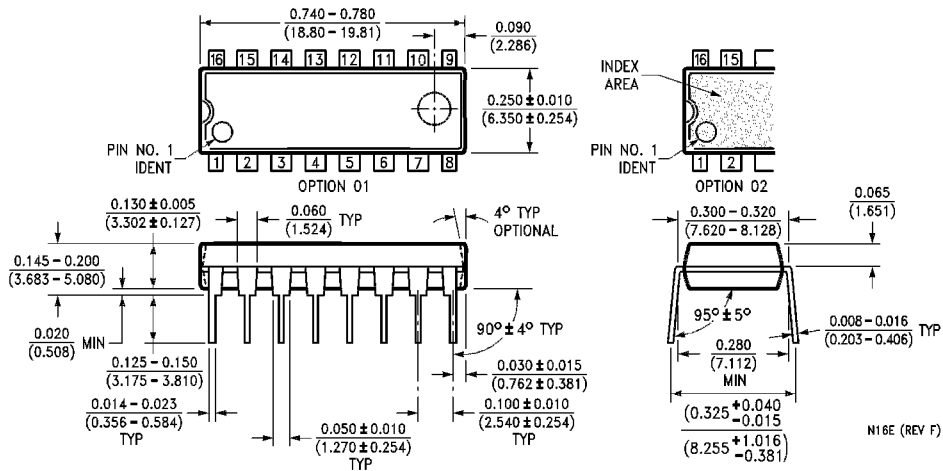
**16-Lead (0.150" Wide) Molded Small Outline Package, JEDEC (S)  
Package Number M16A**



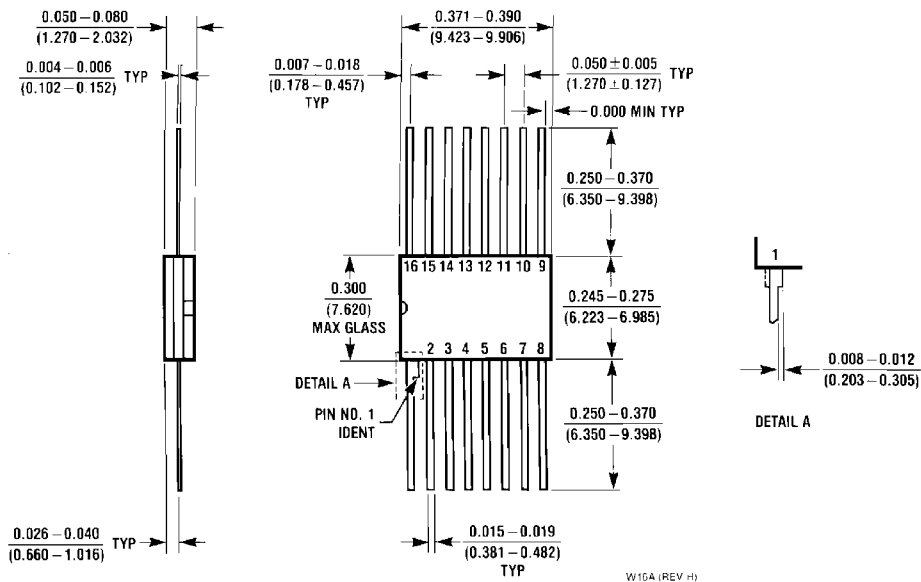
**16-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)  
Package Number M16D**



**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead (0.300" Wide) Molded Dual-In-Line Package (P)**  
Package Number N16E



**16-Lead Ceramic Flatpak (F)**  
Package Number W16A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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