STCF04

High power white LED SuperCap™ driver with I²C interface

Datasheet — production data

Features

- Buck-boost converter with 1.5 A peak current limiting and synchronous rectification
- Burst mode operation when output is charged
- Input voltage range 2.5 V to 5.5 V
- Programmable output charging voltage up to 5.5 V
- Full I²C control
- Operation modes:
  - Shutdown mode
  - Monitoring mode with NTC and SuperCap monitoring
  - Idle mode
  - Flash mode
  - Torch mode: up to 320 mA
- Controlled LED current in all modes
- Soft and hard triggering of Flash, Torch and Picture light modes
- Torch dimming in 12 exponential steps
- Flash dimming in 8 steps
- Active balancing of SuperCap voltage
- SuperCap status flag
- Internally or externally timed flash operation
- Digitally programmable safety timeout in Flash mode
- Torch mode safety timeout
- LED overtemperature detection and protection with external NTC resistor
- Shorted LED failure detection and protection
- Chip overtemperature detection and protection

TFBGA25 (3 x 3 mm)

Applications

- Cell phones and smartphones
- Camera flashes/strobe
- PDAs and digital still cameras

Description

The STCF04 is a dedicated and space optimized high efficiency solution for driving a flash LED module in cameras, phones, PDAs and other handheld devices using the SuperCap technology. It is based on a DC-DC buck-boost converter, which ensures a proper and efficient charging control and monitoring of the SuperCap in the whole battery voltage range. The output current control ensures a good current regulation over the forward voltage spread characteristics of the flash LEDs in Torch and Flash mode operation. The SuperCap charging current is limited to a defined value which avoids overload of the battery. The SuperCap discharge current flows through the LEDs and the external MOSFET which must be chosen according to the desired flash current.

Table 1. Device summary

Order code	Package	Packaging
STCF04TBR	TFBGA25 (3 x 3 mm)	3000 parts per reel

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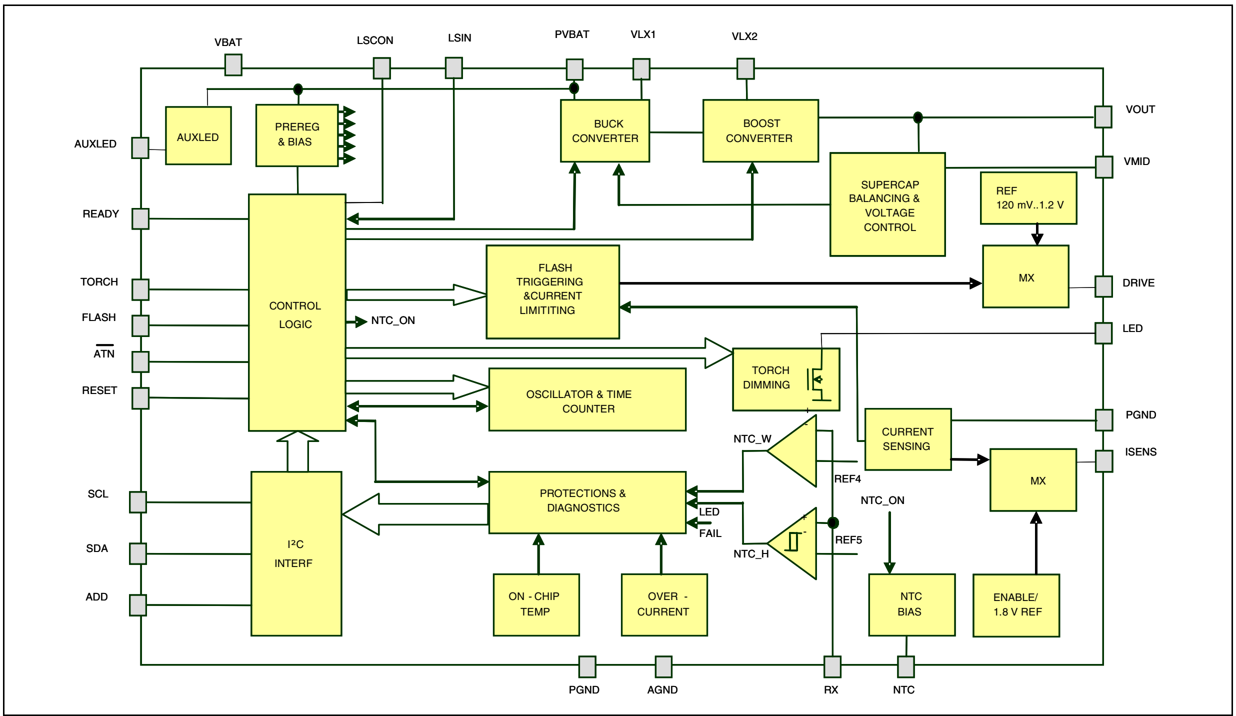
1 Description (continued)

All the functions of the device are controlled through the I^2C bus which reduces the number of logic pins of the package and saves PCB tracks on the application board. Hard and soft-triggering of flash and torch are both supported. The device includes many functions to protect the chip and the power LEDs. These include a soft-start control, chip overtemperature detection and protection, and shorted LED detection and protection. In addition, a digital programmable timeout function protects the LEDs in case of a wrong command issued by the microprocessor. An optional external NTC is supported to protect the LEDs against overheating. It is possible to separately program the current intensity in Flash and Torch mode through I^2C. In order to guarantee the proper function of Flash mode, the SuperCap voltage should be monitored by the microprocessor using the READY pin feature. In case of insufficient power from the SuperCap, a warning is generated. The device is packaged in BGA 3 x 3 mm with 1 mm height.

2 Diagram

Figure 1. Block diagram



3 Pin configuration

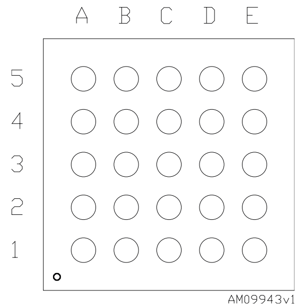


Figure 2. Pin connection (top view)

Table 2. Pin description

Pin	Symbol	Description
A1	VLX1	Inductor connection 1
E1	VLX2	Inductor connection 2
D5	R_X	R_X resistor connection
D1	VOUT	SuperCap connection
C1	VMID	SuperCap middle pin connection
E5	NTC	NTC resistor connection
A3	READY	SuperCap status flag pin
B3	SCL	I^2C clock signal
A4	FLASH	Flash trigger input
E2	AGND	Signal ground
B5	TORCH	Torch trigger input
B4	RESET	External reset input
D4	ISENS	Flash regulator sensing connection
C3	ADD	I^2C address selection
E4	LED	Diode module cathode connection
C4	ATN	Attention (open drain output, active LOW)
B1	PVBAT	Supply voltage
A5	SDA	I^2C data
E3	AUXLED	Auxiliary red LED connection
B2	LSCON	Light sensor capacitor connection
D3	VBAT	Signal supply voltage
A2	LSIN	Light sensor input
C5	DRIVE	MOSFET driver output
C2, D2	PGND	Power ground + die back connection

4 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VBAT, PVBAT	Signal supply voltage	- 0.3 to 6	V
VLX	Inductor connection	- 0.3 to 6	V
VOUT	SuperCap connection	- 0.3 to 6	V
VDCDC	DC-DC converter output	- 0.3 to 6	V
VMID	SuperCap middle pin connection	- 0.3 to 6	V
AUXLED	AUXLED connection	- 0.3 to 6	V
LED	LED connection	- 0.3 to 6	V
SCL, SDA, ATN, ADD, READY, TORCH, FLASH, RESET	Logic pins	- 0.3 to V_{BAT} + 0.3	V
PVBAT	Power supply voltage	- 0.3 to V_{BAT} + 0.3	V
DRIVE	External MOSFET drive	- 0.3 to 6	V
LSIN	Light sensor input	- 0.3 to 6	V
LSCON	Light sensor capacitor connection	- 0.3 to 6	V
R_X	Connection for reference resistor	- 0.3 to 3	V
NTC	Connection for LED temperature sensing	- 0.3 to 3	V
ISENS	Flash regulator sensing connection	- 0.3 to 3	V
ESD	Human body model	± 2	kV
P_{TOT}	Continuous power dissipation (at T_A=70 °C)	1	W
T_{OP}	Operating junction temperature range	- 40 to 85	°C
T_J	Junction temperature	- 40 to 150	°C
T_{STG}	Storage temperature range	- 65 to 150	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

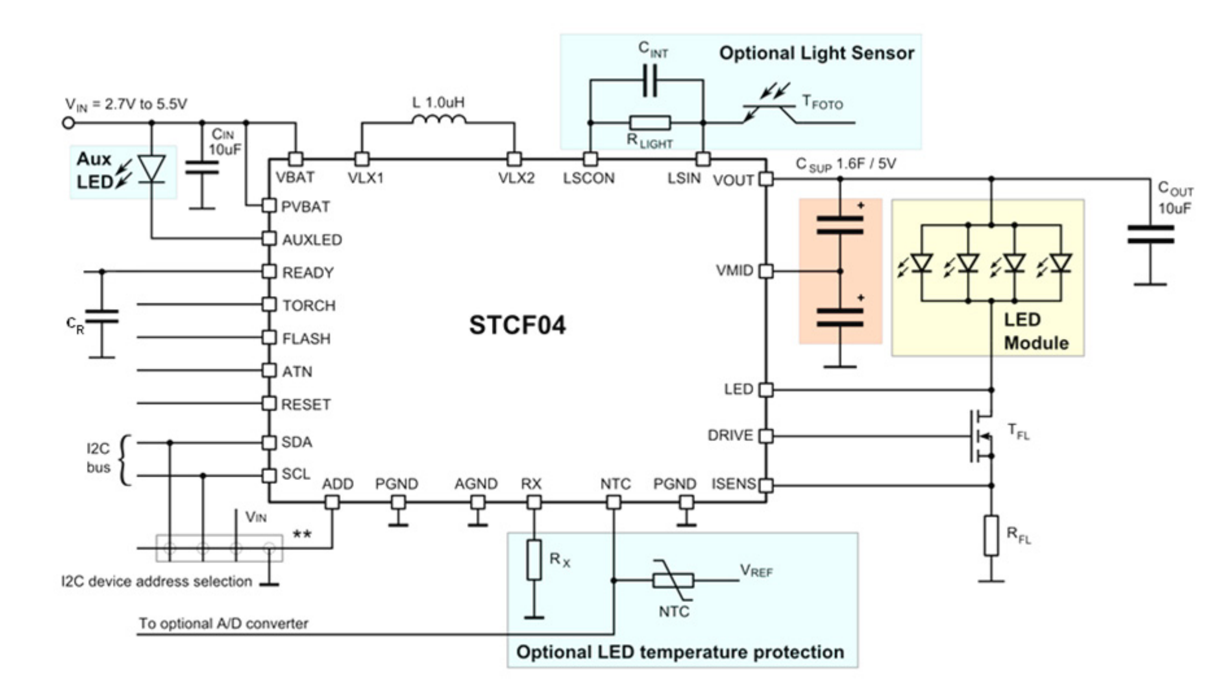
Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient (1)	56	°C/W

1. This parameter corresponds to the PCB board, 8 layers with 1 inch² of cooling area.

5 Application

Figure 3. Application schematic



Note: ***: connect to V_I, or GND or SDA or SCL to choose one of the 4 different I²C slave addresses. Optional components to support auxiliary functions are highlighted with blue rectangles.*

Note: *The anode of the AuxLED should be also connected to the V_{OUT}.*

Table 5. List of external components

Component	Manufacturer	Part number	Value	Size
L	Murata	LQM2HPN1R0MJC	1 µH / 1.5 A	2.5 x 2.0 x 1.1 mm
	TDK	VLS252012T-1R0N1R7	1 µH / 1.7 A	2.5 x 2.0 x 1.2 mm
CIN, COUT	TDK	C1608X5R0J106MT	10 µF / 6.3 V	0603
Rx	Rohm	MCR01MZPJ15K	15 kΩ	0402
NTC	Murata	NCP21WF104J03RA	100 kΩ	0805
CSUP	Murata	DME2W5R5K404M	400 mF / 5.5 V	20.5 x 18.5 x 3 mm
	TDK	EDLC152344	550 mF / 5.5 V	44 x 23 x 1.5 mm
		EDLC272020	500 mF / 5.5 V	20 x 20 x 2.7 mm
	CAP-xx	GS 2 19F	1.6 F / 5 V	40 x 17 mm
LED MODULE	Luxeon	4x LXCL-PWF4	White LED	0805
T_{FL}	STMicroelectronics	STL8NH3LL	8 A / 12 mΩ	3.3 x 3.3 x 0.9 mm
R_{FL}	Tyco	TL2BR01FTE	0R01	1206
C_{INT} [(1)]	TDK		10 µF / 6.3 V	0402
R_{LIGHT}*	Tyco			0402
T_{FOTO}*	Vishay	TEMT6000		4 x 2 x 1 mm
AUXLED			Red LED	0603
C_R			100 nF	0402

1. Optional components for the auxiliary light sensor feature.

Note: The components listed above refer to a typical application. However, STCF04 operation is not limited to the choice of these external components.

6 Electrical characteristics

T_A = 25 °C, V_{IN} = 3.6 V connected to V_{BAT} and P_{VBAT}, C_{IN} = 10 µF, C_{SUP} = 1.6F/5 V L = 1 µH, R_X = 15 kΩ, V_{FLED} = 4.2 V/10 A. Unless otherwise specified, typical values are at 25 °C.

Table 6. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input supply voltage		2.5		5.5	V
$V_{PW\_ON RESET}$	Power-ON reset threshold	V_{IN} rising		2.3		V
I_O	Output current adjustment range I_{TORCH}	Torch mode V_{IN}=2.7 V to 5.5 V	15		320	mA
	Auxiliary LED output current adjustment range I_{AUXLED}	Idle mode, V_I or V_O=3.3 V to 5.5 V	0		100	
V_{ISENS}	Current sensing input	V_{IN}=2.7 V to 5.5 V, I_{LED} = 12 A R_{FL} = 10 mΩ	108	120	132	mV
I_{PEAK}	Switch peak current limit	V_{IN}=2.7 V to 5.5 V, IDC0=0		1.45		A
		V_{IN}=2.7 V to 5.5 V, IDC0=1		1.80		
V_{OUT}	Regulated voltage range optimized for Flash mode	V_{IN}=2.7 V to 5.5 V	4.5		5.5	V
	Regulated voltage range optimized for Torch mode	V_{IN}=2.7 V to 5.5 V		V_{FLED}+ 0.25		V
	V_{OUT} tolerance	Percentage with respect to programmed voltage	-5		+5	%
I_{MID}	Active balancing output	V_{IN}=2.7 V to 5.5 V	-400		400	mA
ΔI_O	Output current variation	Torch mode I_{LED} = 300 mA	-10		10	%
I_Q	Quiescent current in Shutdown mode	V_{IN}=2.7 to 5.5 V, NTC_ON=0			1	µA
	Quiescent current in Shutdown mode	V_{IN}=2.7 to 5.5 V, NTC_ON=1		2		
	Quiescent current in Monitoring mode	NTC_ON=0, SuperCap monitoring=1		45		
	Quiescent current in Idle mode	NTC_ON, CHRG=0			1	mA
f_s	Switching frequency	V_{IN}=2.7 V		1.8		MHz

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
ν	Efficiency of the converter	V_{IN}=3.7 V, VDC_0,1=1, IDC0=1		85		%
	Efficiency in Torch mode operation	V_{IN}=2.7 V to 4.2 V, IDC_0=1, TCHV_H=1 I_{TORCH}=320 mA		50		
		V_{IN}=2.7 V to 4.2 V, IDC_0=1, TCHV_H=0 I_{TORCH}=320 mA		70		
$V_{SUPHYST}$	SuperCap regulated voltage hysteresis	V_{SUPMAX}=5.5 V, V_{SUPMIN}=5.5 V-$V_{SUPHYST,}$ TCHV_H=1 or FLASH_ON=1		1.3		V
		V_{SUPMAX}=5.0 V, V_{SUPMIN}=5.0 V-$V_{SUPHYST,}$ TCHV_H=1 or FLASH_ON=1		0.8		
		V_{SUPMAX}=4.5 V, V_{SUPMIN}=4.5 V-$V_{SUPHYST}$, TCHV_H=1 or FLASH_ON=1		0.3		
		V_{SUPMAX}=4.2 V, V_{SUPMIN}=4.2 V-$V_{SUPHYST}$, TCHV_H=0		0.2		
$V_{MONIREADY}$	SuperCap voltage ready hysteresis	PWR_ON=0, VDC_0 or/and VDC_1=1		0.2		V
OTP	Overtemperature protection	V_{IN}=5.5 V		140		C
OTHYST	Overtemperature hysteresis	V_{IN}=5.5 V		20		C
V_NTCW	NTC threshold warning	Idle mode, I_{NTC}=2 mA max.		0.56		V
V_NTCH	NTC threshold hot	Idle mode, I_{NTC}=2 mA max.		1.2		V
VOL	Output logic signal level low ATN, READY	$I_{ATN,\ READY}$=+10 mA			0.3	V
I_{OZ}	Output logic leakage current ATN, READY	$V_{ATN,\ READY}$ =3.3 V			1	mA
V_{IL}	Input logic signal level SCL, SDA, TEST, RESET, SCHRG, FLASH, TORCH, ADD	V_{IN}=2.7 V to 5.5 V	0		0.4	V
V_{IH}			1.4		3.0	
I_{LSCON}	Input reset current	V_{IN}=2.7 V to 5.5 V, V_{REF}=1.6 V			10	mA
V_{LSIN}	Analog input signal range	V_{IN}=2.7 V to 5.5 V	0.1		1.6	V
V_{DRIVE}	MOSFET driver output	Source: I_{DRIVE} = -8 mA		4.27		V
		Sink: I_{DRIVE} = +8 mA		1.05		V
	Reference voltage range	EXT_REG=1 (1)	0.12		1.2	V
T_{ON}	LED current rise time I_{LED}=0 to I_{LED}=max.	Flash triggered by external trig			0.3	ms

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{RESMIN}	Minimum RESET time	V_{IN}=2.7 V to 5.5 V	1			µs
$T_{LSCAPRES}$	Reset time of the light sensor capacitor		200			µs

7 Introduction

The STCF04 is a high efficiency buck-boost converter with input current limitation dedicated to managing the power for Flash/Torch mode operations using the SuperCap technology and to control the high current white LEDs in cell phone cameras and portable applications in general.

The device operates in Free-running mode with a coil peak current limiter. It charges and stores the energy on the SuperCap from a single cell lithium-Ion battery (2.5 V to 4.2 V). The device contains an active balancer circuit able to regulate the middle pin of the SuperCap, therefore guaranteeing the reliability of the SuperCap component. The device operation and diagnostic are controlled by the I²C bus. Torch current is adjustable from 15 mA to 320 mA. The maximum flash current is set by choosing the R_{FL} resistor and it can be adjusted by I²C using a dedicated register. The device operates as a standalone flash SuperCap controller able to drive one external MOSFET.

The device has two modes of managing the energy in the SuperCap during Torch mode operation, both adjustable by I²C:

1. Torch mode 1: in this case the output current in Torch mode is regulated from $V_{OUT,}$ which is set by V_{DC} bits in the feature register (R4). This mode is optimized to give the possibility of triggering the flash without any delay caused by a recharging of the SuperCap.
2. Torch mode 2: in this case the output current in Torch mode is regulated from V_{OUT} = V_{FLED} + 0.25 V. This mode is optimized for maximum efficiency in Torch mode. The SuperCap must be recharged after the end of Torch mode operation.

The device uses an external NTC resistor to sense the temperature of the white LEDs and light sensor management to optimize the flash duration in Flash mode. These last two functions are optional so they may not be needed in all applications, and, in such cases, the relevant external components can be omitted. In Monitoring mode, when the voltage Monitoring mode of the SuperCap is active, the device is working with low consumption. When the READY pin goes HIGH, meaning that the SuperCap has been self-discharged, the P should initiate a re-charge of the SuperCap, for example, by entering Charge mode.

8 Detailed description

8.1 Logic pins

8.1.1 SCL, SDA pins

These are the standard CLOCK and DATA pins as defined in the I²C bus specifications. External pull-ups are required according to I²C bus specifications.

8.1.2 FLASH pin

This input pin is internally AND-ed with the FLASH_ON bit to generate the internal signal that activates the flash operation. This gives the user the possibility to accurately control the flash duration using a dedicated pin, avoiding the I²C bus latencies (hard-triggering). Neither internal pull-up nor pull-down is provided.

8.1.3 TORCH pin

This input pin is internally AND-ed with the TCH_ON bit to generate the internal signal that activates the torch operation. Neither internal pull-up nor pull-down is provided.

8.1.4 RESET pin

This pin works as an external reset input. The microprocessor can use this pin to reset the STCF04 at any time. Neither internal pull-up nor pull-down is provided. This pin is active LOW.

8.1.5 ATN pin

This output pin (open drain, active LOW) is provided to better manage the information transfer from the STCF04 to the microprocessor. Because of the limitations of a single master I²C bus configuration, the microprocessor should regularly communicate with the STCF04 to verify if certain operations have been completed, or to check diagnostic information. Alternatively, the microprocessor can use the ATN pin to be advised that a new data is available in the STAT_REG register, therefore avoiding continuous communication. The information may then be read in the STAT_REG by a read operation via I²C which also automatically resets the ATN pin to HIGH. The STAT_REG is also reset to 0. No internal pull-up is provided.

8.1.6 ADD pin

This pin offers the opportunity of selecting one of the 4 possible I²C slave addresses. Neither internal pull-up nor pull-down is provided. The pin must be connected to GND, VBAT, SCL or SDA to select the desired I²C slave address (see *Table 7*). This pin cannot be left floating.

Table 7. I²C address table

ADD pin	A7	A6	A5	A4	A3	A2	A1	A0
GND	0	1	1	0	0	0	0	R/W
VBAT	0	1	1	0	0	0	1	R/W
SDA	0	1	1	0	0	1	0	R/W
SCL	0	1	1	0	0	1	1	R/W

8.1.7 READY pin

This pin can be used to monitor the voltage on the SuperCap by the microprocessor. The status of this pin has different meanings according to the current mode of operation of the STCF04.

- Idle, Monitoring, Torch mode with TCHV_H=1:

The READY pin goes LOW when the SuperCap voltage reaches the threshold voltage set by the V_{DC} register, otherwise the READY pin is HIGH when $V_{SuperCap}$ goes below V_{DC} voltage - 0.2 V of hysteresis. When READY is HIGH it means that it is necessary to recharge the SuperCap in order to be able to make a flash.

- Torch mode with TCHV_H=0:

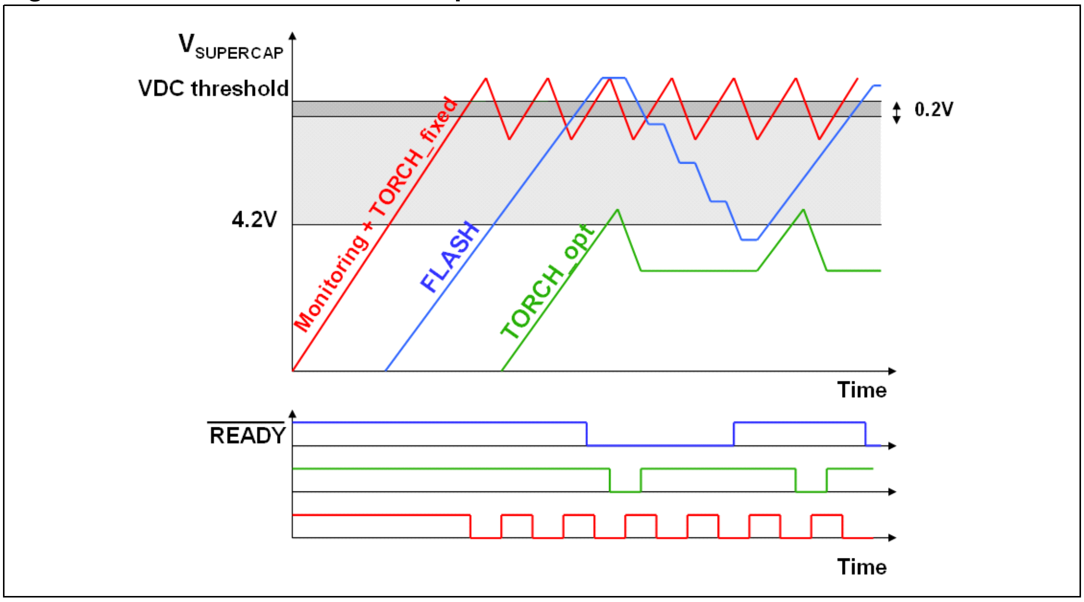
The READY pin goes LOW when the SuperCap reaches 4.2 V and is HIGH when the SuperCap is below 4.2 V and Torch mode is not active.

- FLASH:

The READY pin goes LOW as soon as the SuperCap voltage reaches the threshold voltage set by the V_{DC} register. It stays LOW until the SuperCap voltage decreases below 4.2 V and Flash mode is not active. This feature allows the user to perform multiple flashes.

See *Figure 4* below for details.

Figure 4. Behavior of the READY pin in different modes

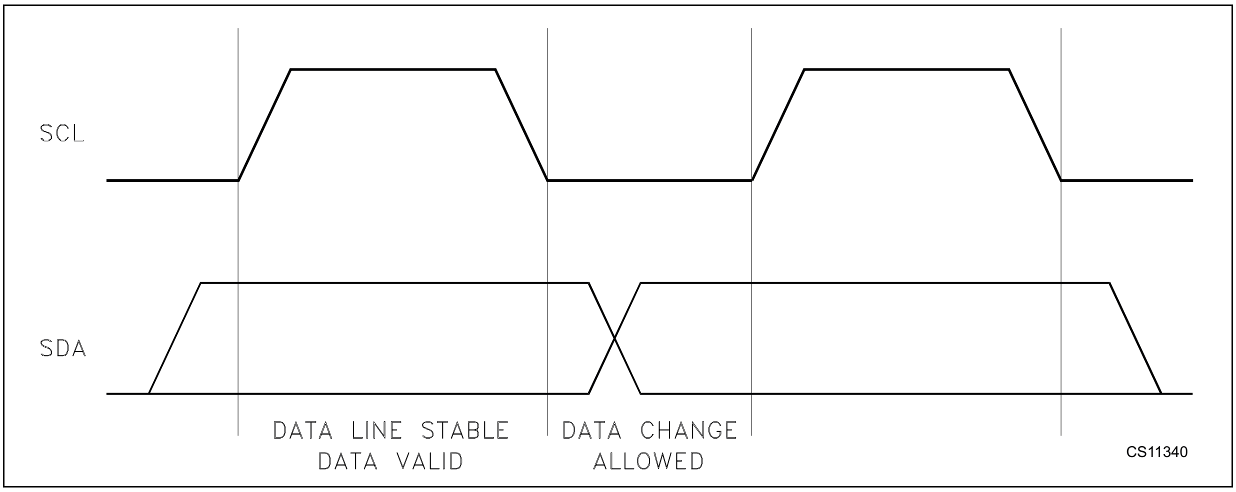


Data transmission from the main microprocessor to the STCF04 and vice versa takes place through the 2 I²C bus interface wires, consisting of the two lines SDA and SCL (pull-up resistors to a positive supply voltage must be externally connected).

8.1.8 Data validity

As shown in *Figure 5*, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

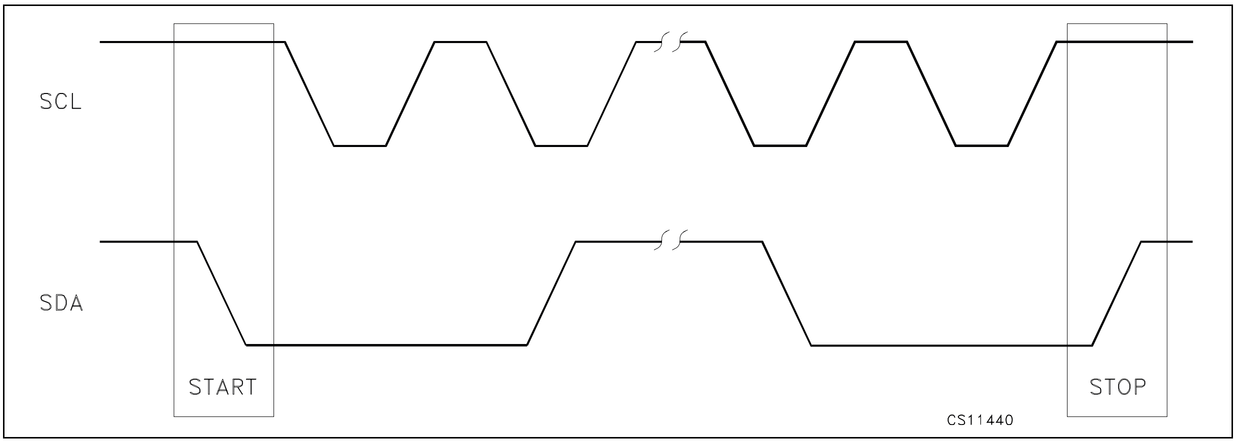
Figure 5. Data validity on the I²C bus



8.1.9 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. As shown in *Figure 6*, a START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The STOP condition is a LOW to HIGH transition of the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition.

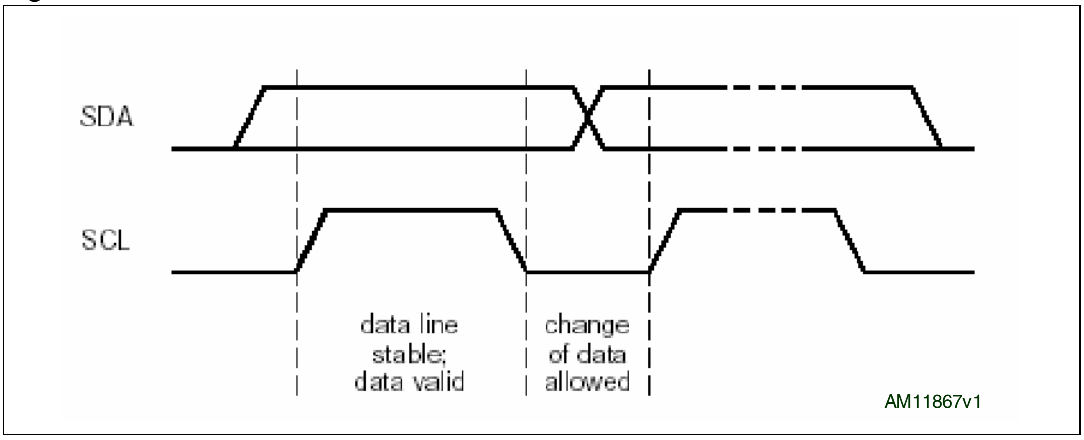
Figure 6. Timing diagram on I²C bus



8.1.10 Byte format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first. One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse. Any change in the SDA line at this time is interpreted as a control signal.

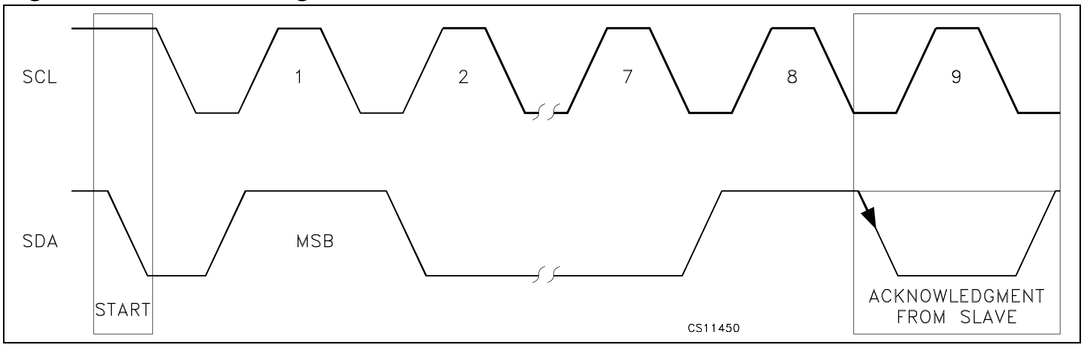
Figure 7. Bit transfer



8.1.11 Acknowledge

The master (microprocessor) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see *Figure 8*). The peripheral (STCF04) that acknowledges must pull down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse. The peripheral which has been addressed must generate an acknowledge pulse after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse duration. In this case, the master transmitter can generate the STOP information in order to abort the transfer. The STCF04 does not generate the acknowledge bit if the V_I supply is below 2.7 V.

Figure 8. Acknowledge on I²C bus



8.1.12 Interface protocol

The interface protocol is composed of (*Table 8*):

- A START condition (START)

- A device address + R/W bit (read =1 / write =0)

- A register address byte

- A sequence of data n* (1 byte + acknowledge)

- A STOP condition (STOP)

The register address byte determines the first register in which the read or write operation takes place. When the read or write operation is finished, the register address is automatically incremented.

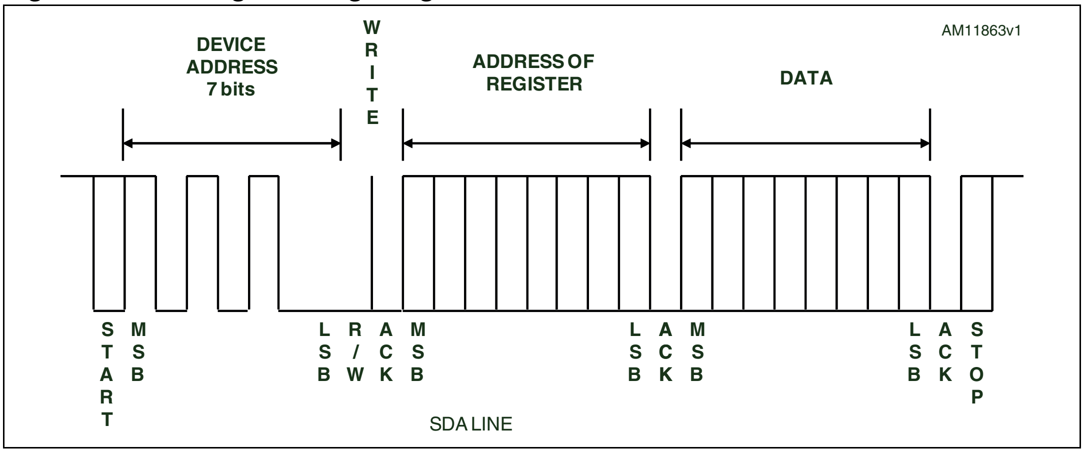
Table 8. Interface protocol

	Device address + R/W bit									Register address									Data									
	7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0		
START	MSB						LSB	RW	ACK	MSB							LSB	ACK	MSB							LSB	ACK	STOP

8.1.13 Writing to a single register

Writing to a single register starts with a START bit followed by the 7-bit device address of the STCF04. The 8th bit is the R/W bit, which is 0 in this case. R/W = 1 means a reading operation. The master then waits for an acknowledgement from the STCF04. The 8-bit register address is then sent to the STCF04. It is also followed by an acknowledge pulse. The last transmitted byte is the data to be written to the register. It is again followed by an acknowledge pulse from the STCF04. The master then generates a STOP bit and the communication is over. See *Figure 9* below.

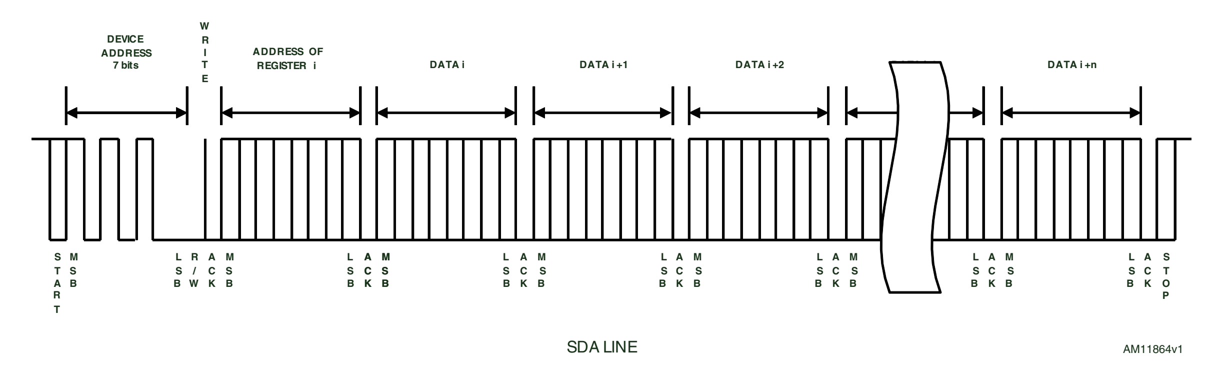
Figure 9. Writing to a single register



8.1.14 Writing to multiple registers with incremental addressing

It would be impractical to send the device address and the address of the register when writing to multiple registers several times. The STCF04 supports writing to multiple registers with incremental addressing. When data is written to a register, the address register is automatically incremented, so the next data can be sent without sending the device address and the register address again. See *Figure 10* below.

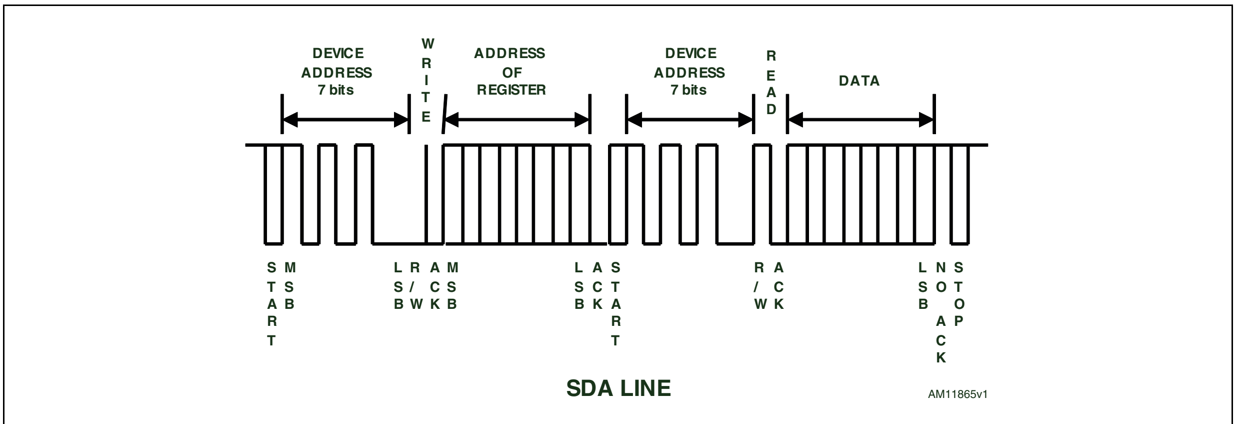
Figure 10. Writing to multiple registers with incremental addressing



8.1.15 Reading from a single register

The reading operation starts with a START bit followed by the 7-bit device address of the STCF04. The 8th bit is the R/W bit, which is 0 in this case. The STCF04 confirms receipt of the address + R/W bit by an acknowledge pulse. The address of the register that should be read is sent afterwards and confirmed again by an acknowledge pulse of the STCF04 again. Then the master generates a START bit again and sends the device address followed by the R/W bit, which is now 1. The STCF04 confirms receipt of the address + R/W bit by an acknowledge pulse and starts to send the data to the master. No acknowledge pulse from the master is required after receiving the data. Then the master generates a STOP bit to terminate the communication. See *Figure 11*.

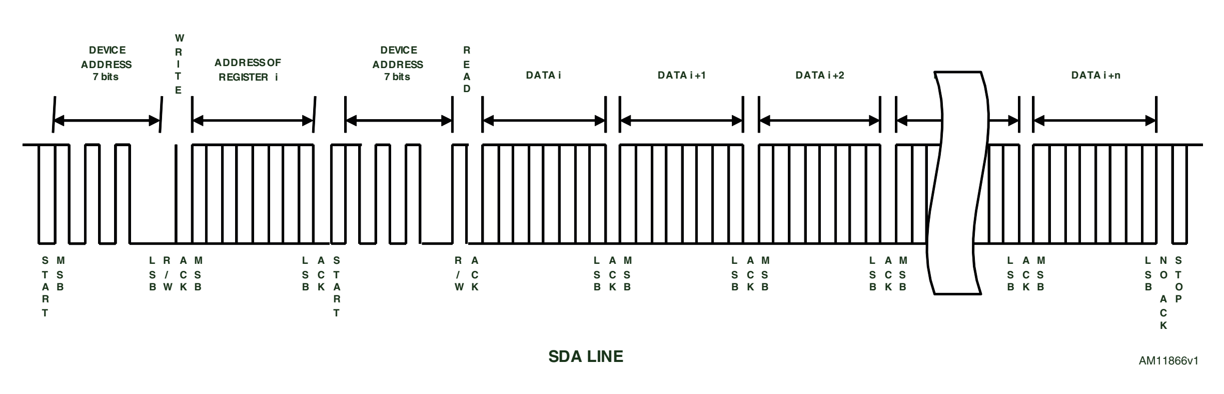
Figure 11. Reading from a single register



8.1.16 Reading from multiple registers with incremental addressing

Reading from multiple registers starts in the same way as reading from a single register. As soon as the first register is read, the register address is automatically incremented. If the master generates an acknowledge pulse after receiving the data from the first register, then reading of the next register can start immediately without sending the device address and the register address again. The last acknowledge pulse before the STOP bit is not required. See *Figure 12*.

Figure 12. Reading from multiple registers



9 Description of the internal registers

Table 9. I²C register mapping

Register name	SUB address (hex)	Operation	Description
CMD_REG	00	R / W	Commands
FL_REG	01	R / W	Flash register
AUX_REG	02	R / W	Auxiliary LED
STAT_REG	03	R only	Status register
FTR_REG	04	R / W	Features
TRCH_REG	05	R / W	Torch register

Note: All the registers can be read only when the PWR_ON bit is 1. Reading any register when PWR_ON = 0, gives 0 regardless of the real value of the register. This concerns command and feature registers in Monitoring mode and Shutdown + NTC mode.

9.1 Commands (CMD_REG) 00(hex)

Table 10. Command register

CMD_REG (Write mode)	MSB							LSB
SUB ADD=00	PWR_ON	FLASH_ON	TCH_ON	NTC_ON	TCHV_H	CHRG	MONTR	N/A
Power-ON RESET value	0	0	0	0	0	0	0	0

9.1.1 PWR_ON

When set, it activates all analog and power internal blocks including the NTC supporting circuit, and the device is ready to operate (Idle mode). As long as PWR_ON=0, only the I²C interface is active, minimizing Shutdown mode power consumption.

9.1.2 FLASH_ON

This bit is AND-ed with the FLASH pin to generate the internal signal FL_ON that activates Flash mode. In this way, both soft-triggering and hard-triggering of the flash are possible. If soft-triggering (through I²C) is chosen, the FLASH pin is not used and must be kept HIGH (tied to VBAT). If hard-triggering is chosen, then the FLASH pin must be connected to a microprocessor I/O devoted to flash timing control, and the FLASH_ON bit must be set in advance. Both triggering modes can benefit from the internal flash time counter, which uses the FLASH_ON bit and can work either as a safety shutdown timer or as a flash duration timer. Flash mode can start only if PWR_ON=1. The LED current is controlled by the value set by the FDIM_0~2 of the DIM_REG.

9.1.3 TCH_ON

Torch on: when set to 1 from Idle mode, the STCF04 enters Torch mode. The LED current is controlled by the value set by the TDIM_0~3 of the TORCH_REG.

9.1.4 NTC_ON

This bit activates the comparators that monitor the LED temperature. NTC-related blocks are always active regardless of this bit in Torch mode and Flash mode.

9.1.5 TCHV_H

Torch voltage HIGH: when set to 1, the SuperCap voltage is maintained to the value set by the feature register (VDC_0~1) during Torch mode. If this bit is set to 0, voltage on the SuperCap is regulated to maintain the desired torch current and optimize the efficiency in Torch mode.

9.1.6 CHRG

This bit enables the charging of the SuperCap, when set to 1, the device starts to charge the SuperCap by the limited current from the PVBAT. During this operation the active balancing circuit is enabled.

9.1.7 MONTR

When this bit is set and the VDC voltage in the feature register is set to a non-zero value at the same time, the device enters Monitoring mode.

9.2 Flash register (FL_REG) 01(hex)

Table 11. Flash register

CL_REG (Write mode)	MSB							LSB
SUB ADD=01	FTIM_4	FTIM_3	FTIM_2	FTIM_1	FTIM_0	FDIM_2	FDIM_1	FDIM_0
Power-ON, Shutdown mode RESET value	0	0	0	0	0	0	0	0

FDIM_0~2: these 3 bits define the LED current in Flash mode with 8 values.

FTIM_0~4: these 5 bits define the flash duration timer value in Flash mode with 32 values.

Table 12. Flash mode dimming registers settings (EXT_REG = 0)

F_DIM (hex)	0	1	2	3	4	5	6	7
DRIVE voltage [mV]**	12	48	60	72	84	96	108	120
LED current [A]*	0.012 V / R_{FL}	0.048 V / R_{FL}	0.060 V / R_{FL}	0.072 V / R_{FL}	0.084 V / R_{FL}	0.096 V / R_{FL}	0.108 V / R_{FL}	0.120 V / R_{FL}
Example LED current (A) for R_{FL} = 10 mΩ	1.2	4.8	6	7.2	8.4	9.6	10.8	12

Note: R_{FL} is the external sensing resistor, external MOS transistor connected, see Figure 3.

FTIM_0~4: these 5 bits define the maximum flash duration. It is intended to limit the energy dissipated by the LED to a maximum safe value or to leave the control of the flash duration to the STCF04 during normal operation. Values from 0~31 correspond to 0~410 ms (according to *Table 13*). The timing accuracy is related to the internal oscillator frequency that clocks the flash time counter (+/- 20%). Entering Flash mode (either by soft or hard triggering) activates the flash time counter, which begins counting down from the value loaded in the F_TIM register. When the counter reaches zero, Flash mode is stopped by resetting the TRIG_EN bit, and simultaneously, the ATN pin is set to true (LOW) to alert the microprocessor that the maximum time has been reached. The FTIM value remains unaltered at the end of the count.

Table 13. Flash time dimming register settings

FTIM_DIM(hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Flash length[ms]	0	5	10	15	20	25	30	35	40	45	50	55	60	65	70	90
FTIM_DIM(hex)	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
Flash length[ms]	110	130	150	170	190	210	230	250	270	290	310	330	350	370	390	410

9.3 AUX LED (AUX_REG) 02(hex)

Table 14. AUX LED register

AUX_REG (Write mode)	**MSB**							**LSB**
SUB ADD = 02	AUXI_3	AUXI_2	AUXI_1	AUXI_0	AUXT_3	AUXT_2	AUXT_1	AUXT_0
Power-ON, Shutdown mode RESET value	0	0	0	0	0	0	0	0

AUXI_0~3: this 4-bit register defines the AUX LED current from 0 to 100 mA. See *Table 15* AUX LED dimming for reference. Loading any value between 1 and 11 also starts the AUX LED current source timer, if enabled. The AUX LED current source is active only in Idle mode, and is deactivated in any other mode.

AUXT_0~3: this 4-bit register controls the timer that defines the ON-time of the AUX LED current source. ON-time starts when the AUXI register is loaded with any value other than zero, and stops after the time defined in the AUXT register. Values from 0 to 14 of the AUXT register correspond to an ON-time of the AUX LED ranging from 100 to 1500 ms in 100 ms steps. The value 15 puts the AUX LED into the continuous light mode. The activation/deactivation of the AUX LED current source is controlled using only the AUXI register.

Table 15. Auxiliary LED dimming table

AUXI (hex)	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**A**	**B**
AUX LED current [mA]	0	6	10	15	20	25	33	40	53	67	80	100

Table 16. Auxiliary LED timing table

AUXT (hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
AUX LED time [s]	0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1	1.1	1.2	1.3	1.4	∞

9.4 Status (STAT_REG) 03(hex)

Table 17. Status register

STAT_REG (Read mode)	MSB							LSB
SUB ADD=03	N/A	F_RUN	FL_R	NTC_W	NTC_H	OT_F	FL_OVR	LTH
Power-ON, Shutdown mode RESET value	0	0	0	0	0	0	0	0

F_RUN: this bit is kept HIGH by the STCF04 during Flash mode. By checking this bit, the microprocessor can verify if the Flash mode is running or has been terminated by the time counter.

FL_R: (FLASH ready) this bit is set to 0 if the SuperCap voltage is not high enough to make a flash.

NTC_W: this bit is set HIGH by the STCF04 and the ATN pin is pulled down, when the voltage seen on the pin R_X exceeds V_{REF4} = 0.56 V. This threshold corresponds to a warning temperature value at the LED measured by the NTC. The device is still operating, but a warning is sent to the microprocessor. This bit stays high until the temperature goes below the threshold.

NTC_H: this bit is set HIGH by the STCF04 and the ATN pin is pulled down, when the voltage seen on the pin R_X exceeds V_{REF5} = 1.2 V. This threshold corresponds to an excess temperature value at the LED measured by the NTC. The device is put into Idle mode to avoid damaging the LED. This bit is reset by the STCF04 following a read operation of the STAT_REG.

OT_F: this bit is set HIGH by the STCF04 and the ATN pin is pulled down, when the chip overtemperature protection (~140 °C) has put the device into Idle mode. This bit is reset by the STCF04 following a read operation of the STAT_REG.

FL_OVR: this bit is set HIGH, if the flash operation is terminated by the light sensor.

LTH: this bit is set HIGH when the local temperature protection for the SuperCap charging circuit is activated.

Table 18. Status register details

Bit name	F_RUN (STAT_REG)	FL_R	NTC_W (STAT_REG)	NTC_H (STAT_REG)	OT_F (STAT_REG)	FL_OVR	LTH
Default value	0	0	0	0	0	0	0
Latched (1)	NO	NO	YES	YES	YES	NO	NO
Forces Idle mode when set	NO	NO	NO	YES	YES	NO	NO
Sets ATN LOW when set	NO	YES	YES	YES	YES	YES	NO

1. YES means that the bit is set by internal signals and is reset to default by an I²C read operation of STAT_REG. NO means that the bit is set and reset by internal signals in real-time.

9.5 Feature (FTR_REG) 04(hex)

Table 19. Feature register

LS_REG (Write mode)	MSB						LSB
SUB ADD=04	IDC_0	N/A	VDC_1	VDC_0	EN_LS	LS_2	LS_1	LS_0
Power-ON, Shutdown mode RESET value	0	0	0	0	0	0	0	0

LS_0~2: these 3 bits define the value of the internal reference voltage for the light sensor comparator. The EN_LS bit must be set to 1 to activate the internal reference for the light sensor comparator.

EN_LS: this bit enables the light sensor function when set HIGH.

Table 20. Light sensor reference dimming register settings

LS_DIM(hex)	0	1	2	3	4	5	6	7
LSREF[mV]	200	400	600	800	1000	1200	1400	1600

VDC_0~1: these 2 bits define the output voltage of the DC-DC converter.

Table 21. DC-DC converter output voltages (V_{OUT})

VDC_1	VDC_0	V_{OUT}
0	0	4.5 V
0	1	5.0 V
1	0	5.5 V

Note: See Section 10.4.

IDC_0: this bit defines the peak current limit value of the DC-DC converter.

Table 22. DC-DC converter coil peak current limit values

IDC_0	$I_{COIL\ (PEAK)}$
0	1.45 A
1	1.80 A

9.6 Torch register (TRCH_REG) 05(hex)

Table 23. Torch register

VRID_REG (Read mode)	MSB							LSB
SUB ADD=05	TTRCH1	TTRCH0	TDIM_3	TDIM_2	TDIM_1	TDIM_0	N/A	N/A
Power-ON, Shutdown mode RESET value	0	0	0	0	0	0	0	0

TTRCH_0~1: these bits define the Torch mode time.

TDIM_0~3: these 4 bits define the LED current in Torch mode with 12 values.

Table 24. Torch mode dimming registers settings

TDIM (hex)	0	1	2	3	4	5	6	7	8	9	A	B
LED current [mA]	15	20	30	45	60	75	100	120	160	200	240	320
Internal step	1	2	3	4	5	6	7	8	9	10	11	12

Table 25. The safety timeout for Torch mode

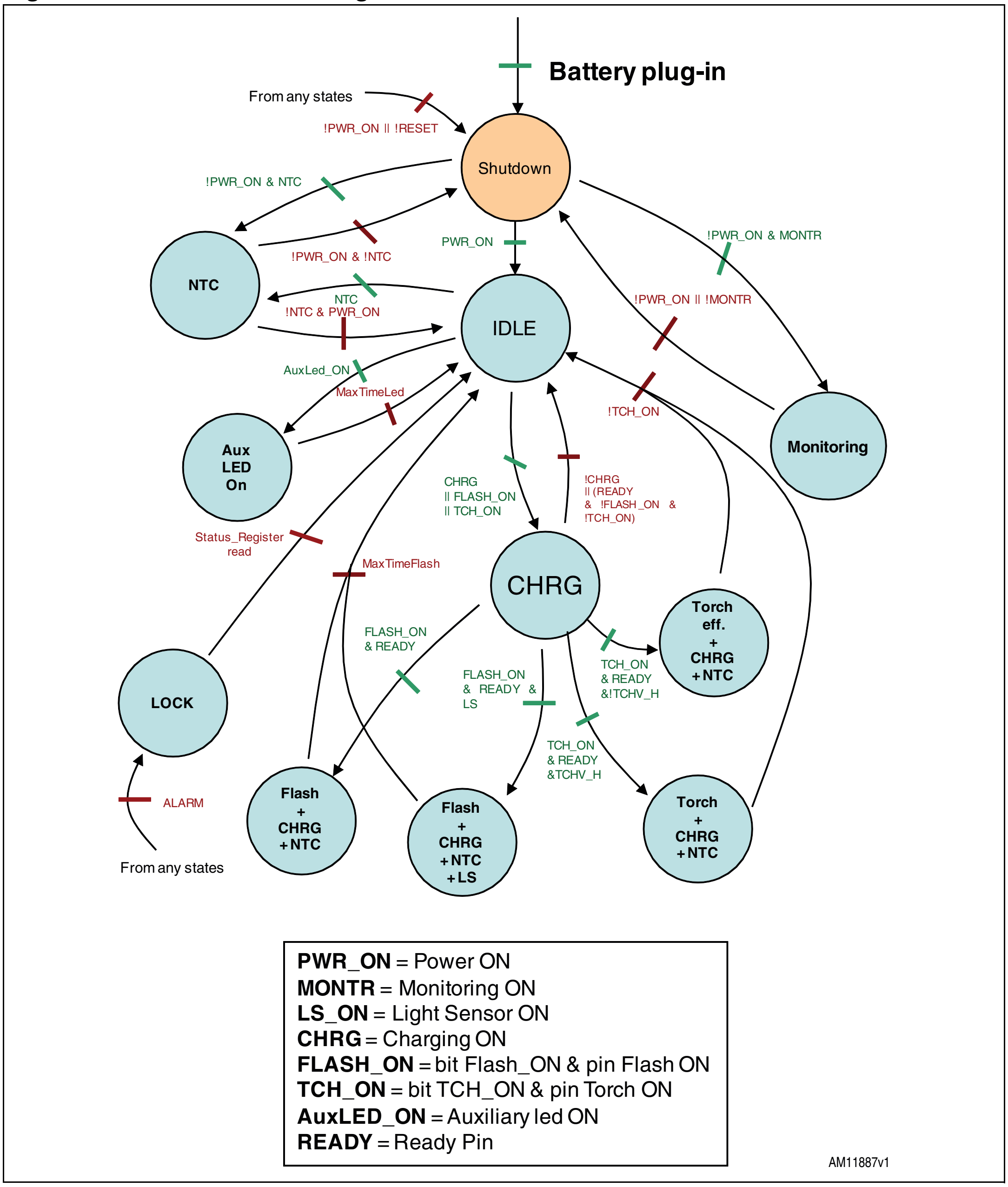
TTRCH1	TTRCH0	Torch time
0	0	Infinity
0	1	5s
1	0	10s
1	1	15s

10 Theory of operation

10.1 The state machine diagram

The state machine diagram of the device describes the overall function of the logic part of the device. It helps with the understanding of all the working modes of the complex and efficient management of the stored energy.

Figure 13. State machine diagram of the STCF04



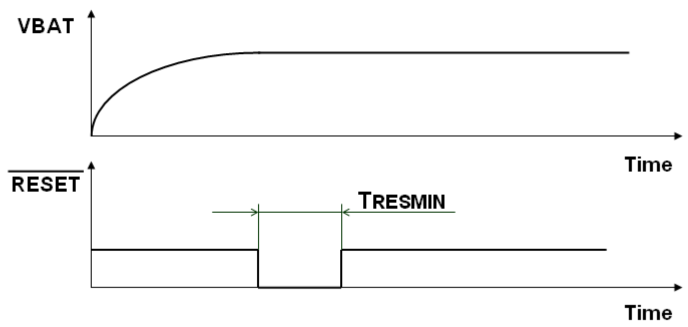
10.2 Power-ON reset

This mode is initiated by applying a supply voltage above the $V_{PW\_ON\ RESET}$ threshold value. An internal timing (~1 µs) defines the duration of this status. The logic blocks are powered, but the device doesn't respond to any input. The registers are reset to their default values, the ATN and SDA pins are in high-Z, and the I²C slave address is internally set by reading the ADD pin configuration. After the internally defined time has elapsed, the STCF04 automatically enters Shutdown mode. For the additional reset of the device, it is also possible to use the RESET pin.

10.2.1 RESET pin function

The device is put into Reset mode when the logic level on the RESET pin is 0. The logic blocks are powered, but the device doesn't respond to any input. The registers are reset to their default values; the ATN and SDA pins are in high-Z. The RESET pin must stay in LOW level for T_{RESMIN} time (1 µs) at least to guarantee correct resetting of the device. When the reset function driven by the RESET pin is not needed, the RESET pin must be connected to the $V_{BAT} = V_{IN}$.

Figure 14. Reset timing



10.3 Shutdown mode and NTC mode

In Shutdown mode only the I²C interface is live, accepting I²C commands and register settings. The device enters this mode automatically after reset or by resetting the PWR_ON bit from other operation modes. Power consumption is at the minimum (1 µA typ.), if NTC is not activated (NTC_ON = 0). If the NTC_ON is set, the µP can measure the LED temperature through an A/D converter connected to the NTC pin. When NTC circuits are active and the $V_{REF-EXT}$ is present, the typical current consumption is increased to 2 µA. It is recommended to not leave the STCF04 in this status if battery drain must be minimized.

10.4 Monitoring mode

When the VDC voltage set by the FTR_REG is not 0, the comparator of the SuperCap voltage is live. This comparator checks the voltage on the SuperCap continuously. If it is higher than the V_{SUPMAX} threshold, then the READY pin is pulled low and stays low until the voltage on the SuperCap is higher than V_{SUPMAX} - 200 mV.

10.5 Idle mode

In this mode all internal blocks are turned ON. The DC-DC converter can be enabled by setting the CHRG bit to 1. If it is enabled, the SuperCap is automatically charged. The NTC circuit can be activated to monitor the temperature of the LED and I^2C commands and register settings are allowed to be executed immediately. The device enters this mode:

- from Monitoring when setting the PWR_ON bit
- from flash operation by resetting the FLASH pin or the FLASH_ON bit, or automatically from flash operation when the time counter reaches zero
- from torch operation by resetting the TCH_ON bit.

The device automatically enters this mode also when an overload or an abnormal condition has been detected during flash or torch operation (see *Table 17*).

10.6 AUX LED

The STCF04 is capable of driving an auxiliary LED. Its cathode is always connected to the AUXLED pin, while its anode can be connected either to the V_{BAT} or V_{OUT} pin. Connecting it to the V_{OUT} pin is particularly advantageous in case of high AUXLED currents. The maximum values of AUXLED currents are guaranteed only for anode voltages higher than 3.3 V, but V_{BAT} may range from 2.7 V to 5.5 V, so in some cases it may not be possible to use maximum currents.

10.7 Single or multiple flash using external (microprocessor) temporization

To avoid the I^2C bus time latency, it is recommended to use the dedicated FLASH pin to define the flash duration (hard-triggering). The FLASH_ON bit of CMD_REG should be set before starting each flash operation, because it may have been reset automatically in the previous flash operation.

The flash duration is determined by the pulse length that drives the FLASH pin. As soon as the flash is activated, the system needs typically 0.3 ms to ramp up the output current on the power LED. The internal time counter times out flash operation and keeps the LED dissipated energy within safe limits in case of software deadlock; the FTIM register must be set first.

Multiple flashes are possible by strobing the FLASH pin. The timeout counter cumulates every flash ON-time until the defined timeout is reached unless it is reloaded by updating the CMD_REG. The number of the flashes depends on V_{FLED}, when the SuperCap is discharged down to 4.2 V, the device goes automatically into Idle mode. After a flash operation is timed out, the device automatically enters Idle mode by resetting the FLASH_ON bit, and it also resets the F_RUN bit. The ATN pin is pulled down to inform the microprocessor that the STAT_REG has been updated. Multiple flash is possible to trigger as long as the READY pin is LOW.

10.8 External (microprocessor) temporization using the FLASH_ON bit

Even though it is possible, it is not recommended to use the FLASH_ON bit to start and stop the flash operation, because of I²C bus latencies: this may result in inaccurate flash timing. Nevertheless, if this operation mode is chosen, the FLASH pin must be kept HIGH (logic level or wired to V_{BAT}), leaving the whole flash control to the I²C bus. Also in this operation mode the time counter times out flash operation and keeps the energy dissipated by the LED within safe limits in case of software deadlock.

10.9 Single flash using internal temporization

Flash triggering can be obtained either by the FLASH pin (hard-triggering) or by I²C commands (soft-triggering). The first solution is recommended for an accurate start time, while the second is less accurate because of the I²C bus time latency. Stop time is defined by the STCF04 internal temporization and its accuracy is determined by the internal oscillator. For hard-triggering, it is necessary to set the FLASH_ON bit in advance. For soft-triggering, the FLASH pin must be kept High (logic level or wired to V_{BAT}) and the flash can be started by setting the FTIM and the TRIG_EN through I²C (both are located in the CMD REG). There is a delay time between the moment the flash is triggered and when it appears. This delay is caused by the time necessary to charge up the output capacitor, which depends on battery voltage. Once triggered, the flash operation is stopped when the time counter reaches zero. As soon as the flash is finished, the F_RUN bit is reset, the ATN pin is pulled down for 11 µs to inform the microprocessor that the STAT_REG has been updated and the device goes back to Idle mode.

10.10 Light sensor feature

This function works as an optional feature, which is able to optimize the length of the flash according to the light conditions in the flashed area. It uses an external capacitor C_{INT}, which is charged by a current coming from the external voltage reference, which is limited by the light sensor (generally made by a phototransistor). Before the start of the flash operation, the C_{INT} capacitor is discharged by the internal switch to the zero voltage during 200 µs. During the flash operation the C_{INT} capacitor integrates the charging current according to the light conditions in the flashed area. When the voltage level on the C_{INT} capacitor reaches the internal reference voltage, which is set by the light sensor register (R4, LS_0~2), the STCF04 stops the operation of the flash and discharges the C_{INT} capacitor through an internal switch.

11 Typical performance characteristics

Figure 15. Flash current vs. input voltage

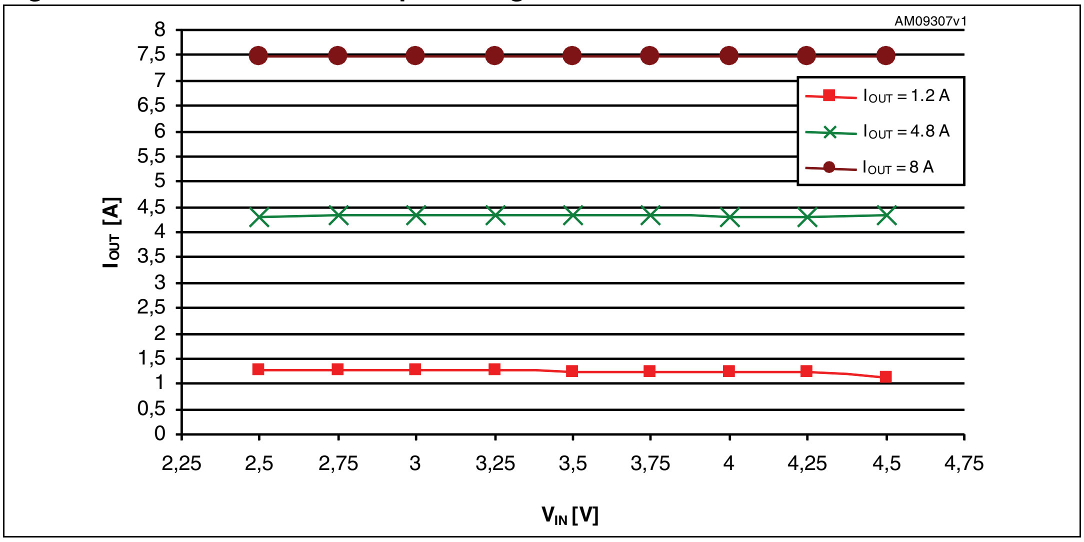


Figure 16. Torch current vs. input voltage

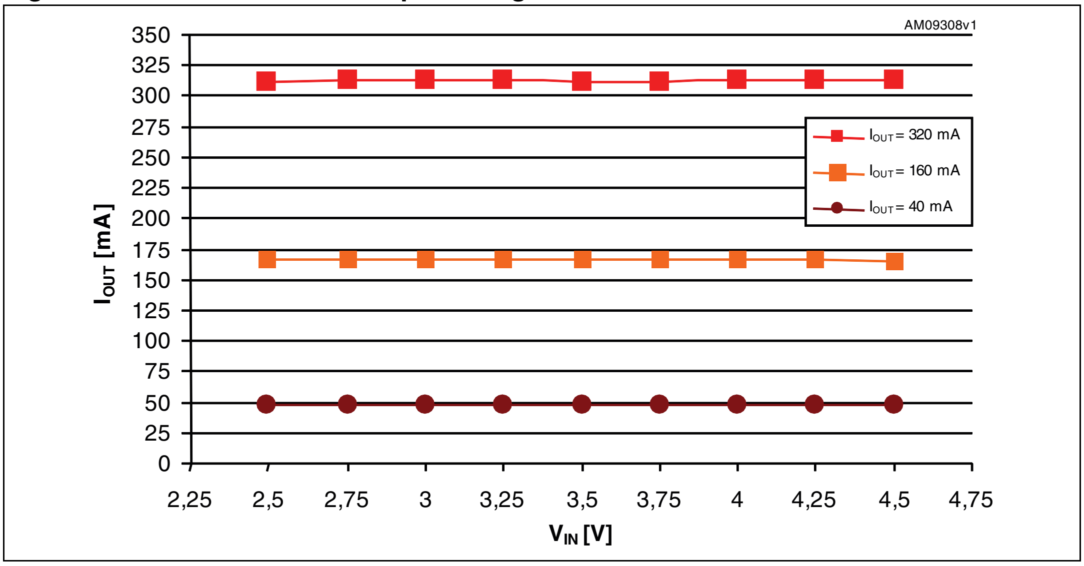


Figure 17. Aux LED current vs. input voltage

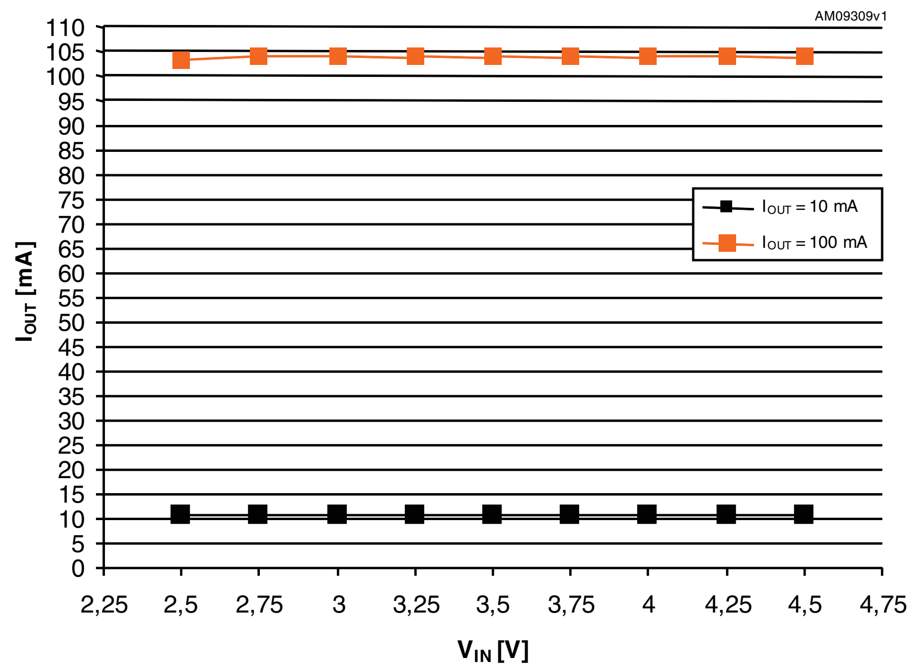


Figure 18. Charging efficiency vs. V_{OUT} voltage (V_{IN} = 3.6 V)

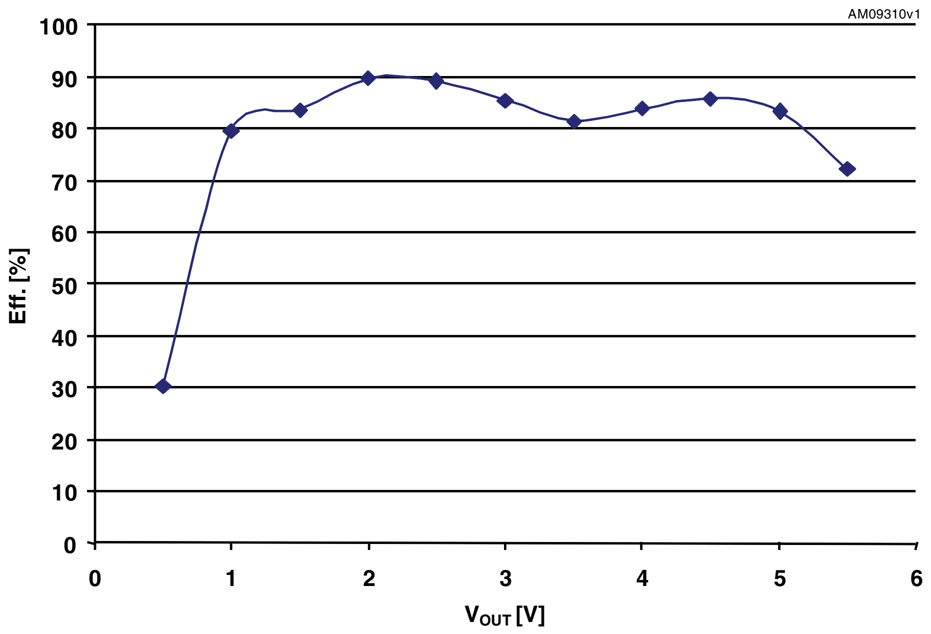


Figure 19. Torch time - settings compared to real values

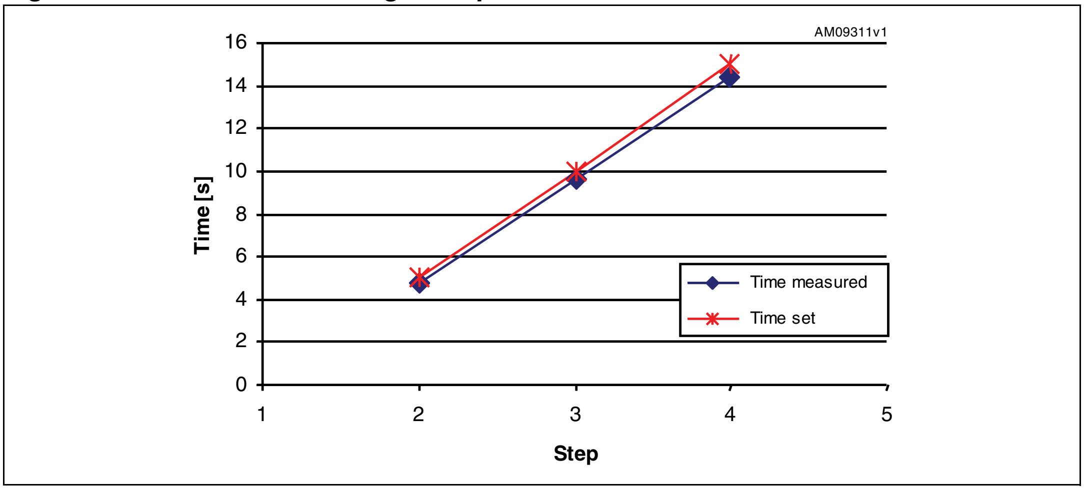


Figure 20. Torch current - settings compared to real values

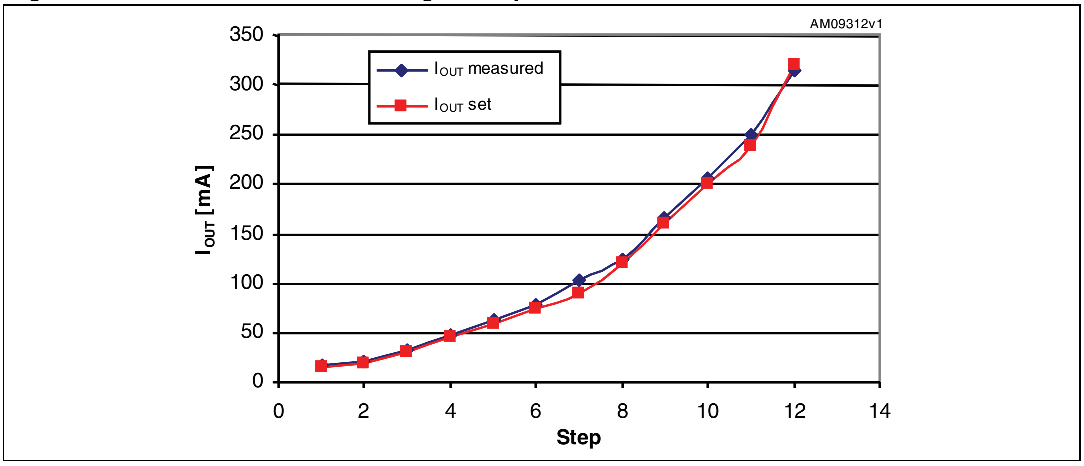


Figure 21. Flash time - settings compared to real values

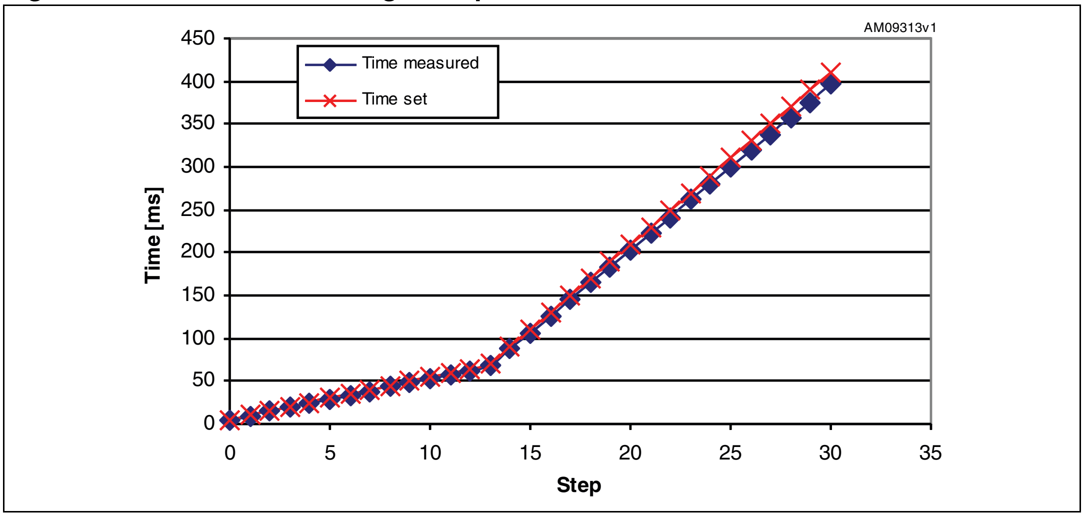


Figure 22. Flash current - settings compared to real values

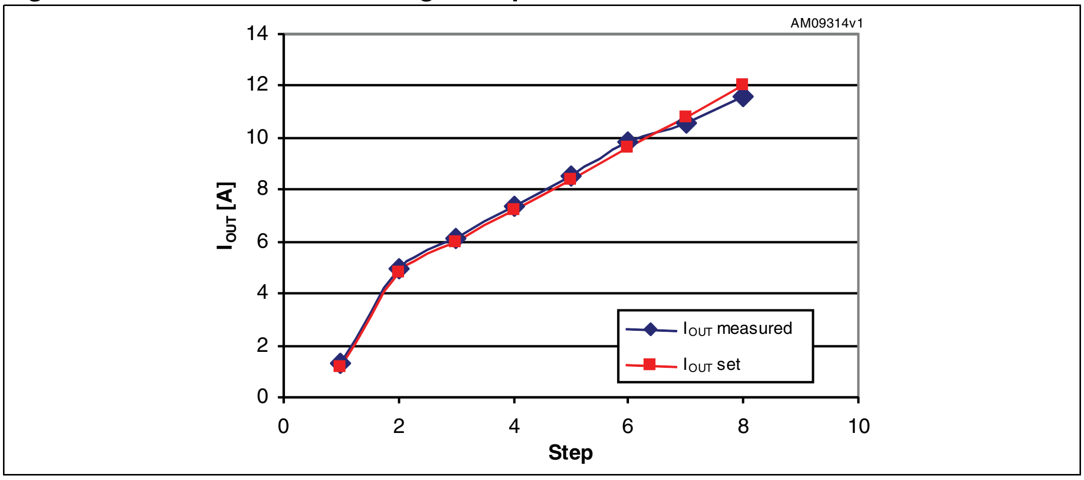


Figure 23. Aux LED time - settings compared to real values

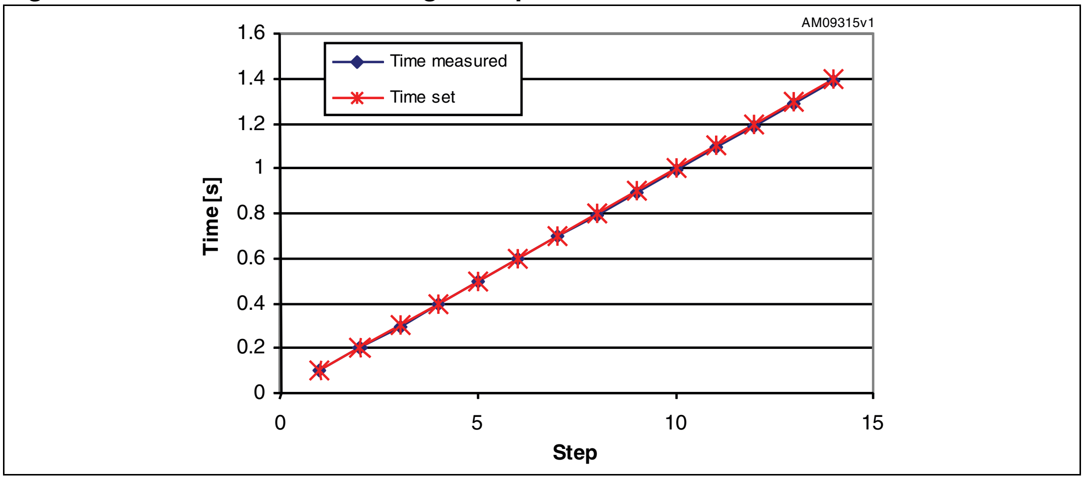


Figure 24. Aux LED current- settings compared to real values

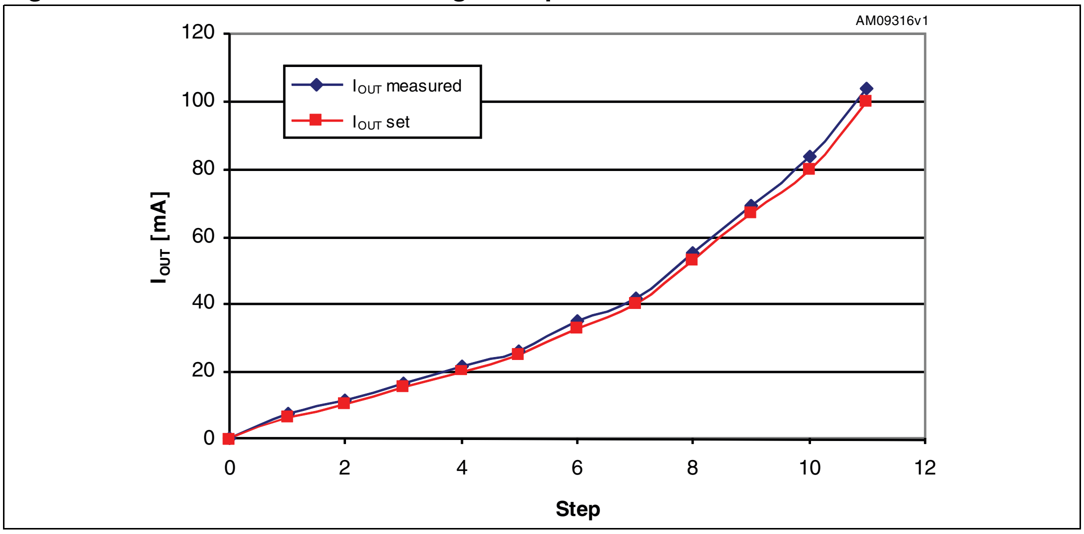
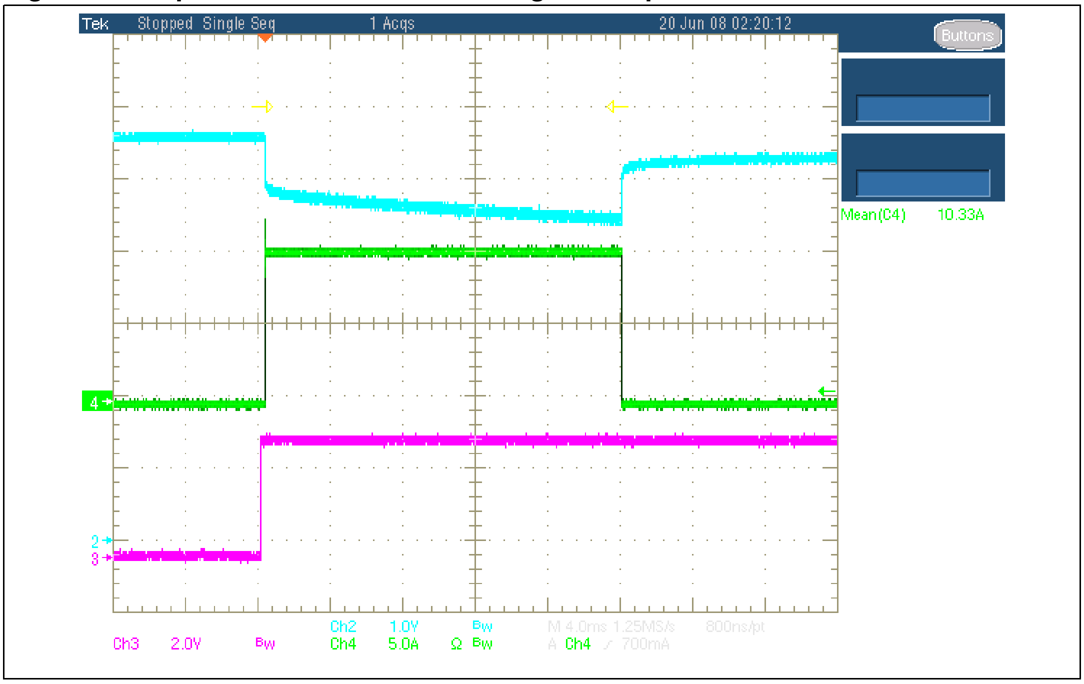
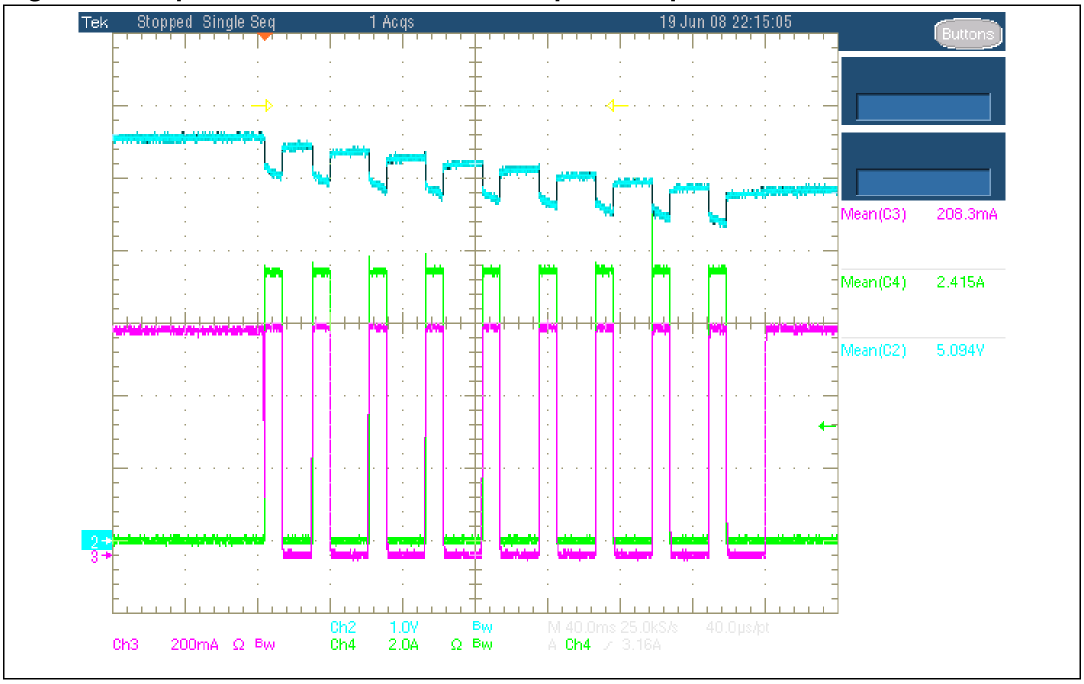


Figure 25. Operation in Flash mode - single flash pulse



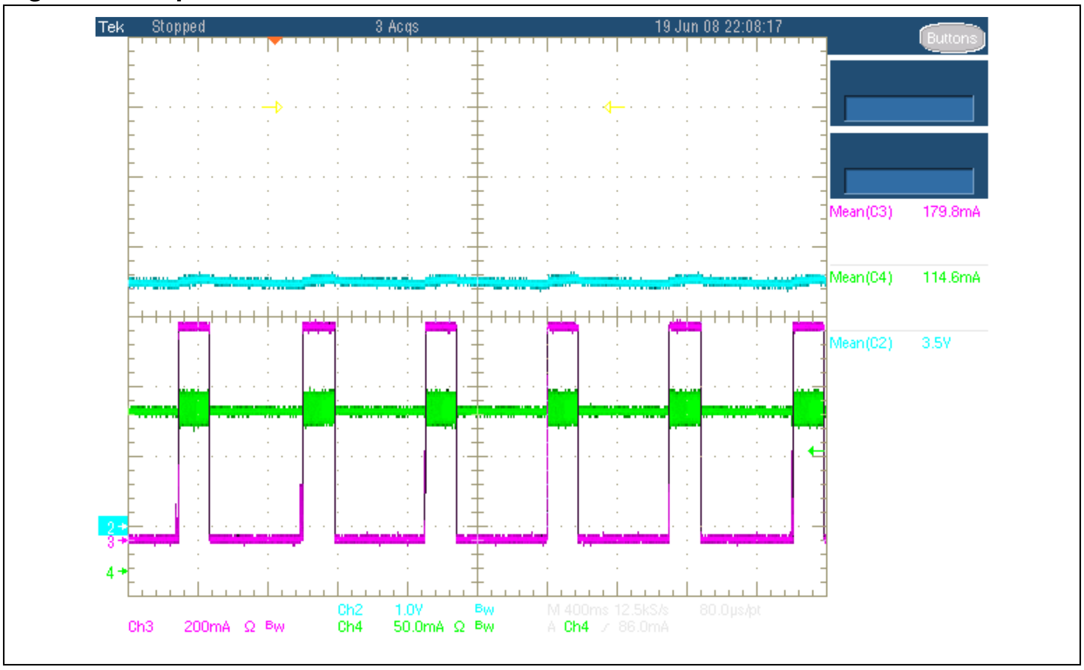
Blue - SuperCap voltage; Green - LED current; Magenta - FLASH pin;

Figure 26. Operation in Flash mode - multiple flash pulses



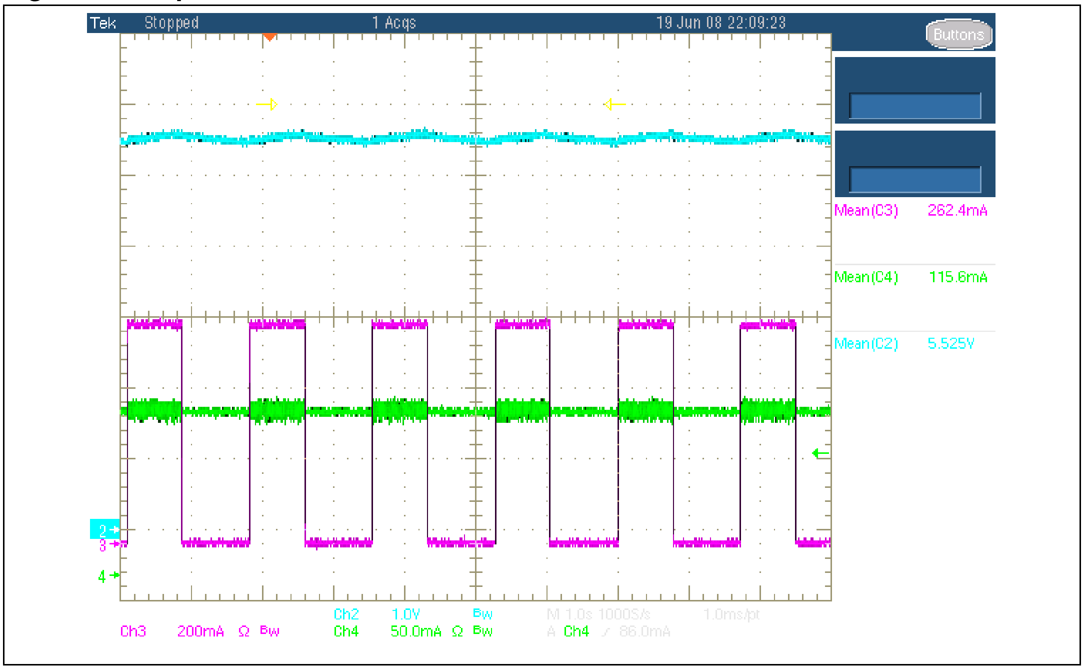
Blue - SuperCap voltage; Green - LED current; Magenta - Battery current;

Figure 27. Operation in Torch mode with TCHV_H bit = 0



Blue - SuperCap voltage; Green - LED current; Magenta - Battery current;

Figure 28. Operation in Torch mode with TCHV_H bit = 1



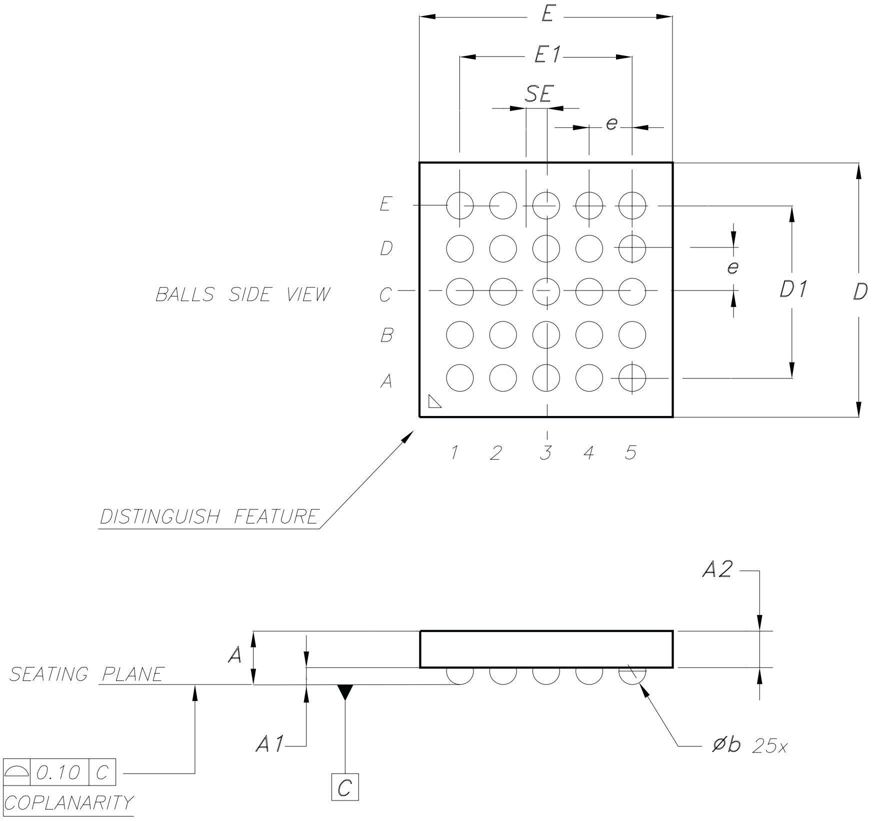
Blue - SuperCap voltage; Green - LED current; Magenta - Battery current.

12 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

TFBGA25 mechanical data

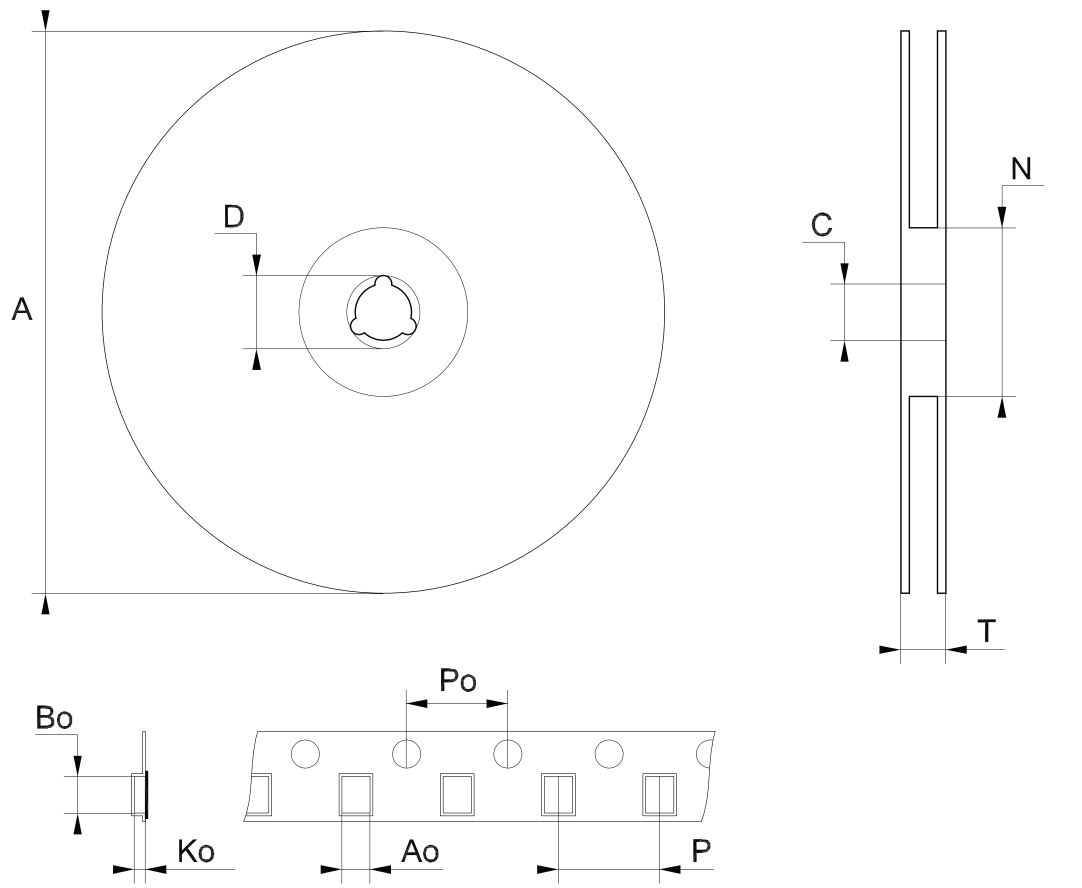
Dim.	mm.			mils.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.0	1.1	1.16	39.4	43.3	45.7
A1			0.25			9.8
A2	0.78		0.86	30.7		33.9
b	0.25	0.30	0.35	9.8	11.8	13.8
D	2.9	3.0	3.1	114.2	118.1	122.0
D1		2			78.8	
E	2.9	3.0	3.1	114.2	118.1	122.0
E1		2			78.8	
e		0.5			19.7	
SE		0.25			9.8	



7539979/A

Tape & reel TFBGA25 mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao		3.3			0.130	
Bo		3.3			0.130	
Ko		1.60			0.063	
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



Note: Drawing not in scale

13 Revision history

Table 26. Document revision history

Date	Revision	Changes
14-Mar-2012	1	Initial release.
16-May-2012	2	Document status promoted from preliminary data to production data.
13-Sep-2012	3	Modified: T_{FL} value 12 mΩ *Table 5 on page 11*.

Please Read Carefully: