



HARRIS

IRFF9130, IRFF9131 IRFF9132, IRFF9133

Avalanche Energy Rated
P-Channel Power MOSFETs

January 1994

Features

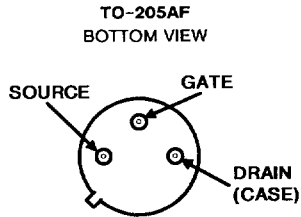
- -5.5A and -6.5A, -80V and -100V
- $r_{DS(ON)} = 0.30\Omega$ and 0.40Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Description

The IRFF9130, IRFF9131, IRFF9132 and IRFF9133 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

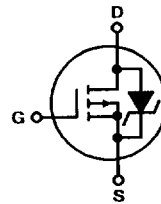
The IRFF types are supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

Package



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^\circ\text{C}$) Unless Otherwise Specified

	IRFF9130	IRFF9131	IRFF9132	IRFF9133	UNITS
Drain-Source Voltage (1)	V_{DS} -100	-80	-100	-80	V
Drain-Gate Voltage ($R_{GS} = 20k\Omega$) (1)	V_{DGR} -100	-80	-100	-80	V
Continuous Drain Current					
$T_C = 25^\circ\text{C}$	I_D -6.5	-6.5	-5.5	-5.5	A
Pulsed Drain Current (3)	I_{DM} -26	-26	-22	-22	A
Gate-Source Voltage	V_{GS} ± 20	± 20	± 20	± 20	V
Maximum Power Dissipation	P_D 25	25	25	25	W
(See Figure 14)					
Linear Derating Factor	0.2	0.2	0.2	0.2	W/ $^\circ\text{C}$
(See Figure 14)					
Single Pulse Avalanche Energy Rating (4)	E_{as} 500	500	500	500	mJ
Operating and Storage Junction	T_J, T_{STG} -55 to +150	-55 to +150	-55 to +150	-55 to +150	$^\circ\text{C}$
Temperature Range					
Maximum Lead Temperature for Soldering	T_L 300	300	300	300	$^\circ\text{C}$
(0.063" (1.6mm) from case for 10s)					

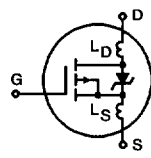
NOTES:

1. $T_J = +25^\circ\text{C}$ to $+150^\circ\text{C}$
2. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. $V_{DD} = 25\text{V}$, Start $T_J = +25^\circ\text{C}$, $L = 17.75\text{mH}$, $R_G = 25\Omega$, Peak $I_L = 6.5\text{A}$ (See Figures 15 and 16)

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POWER MOSFETs

Specifications IRFF9130, IRFF9131, IRFF9132, IRFF9133

Electrical Characteristics $T_C = +25^\circ\text{C}$, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Drain-Source Breakdown Voltage IRFF9130, IRFF9132 IRFF9131, IRFF9133	BV_{DSS}	$V_{GS} = 0V, I_D = -250\mu A$	-100	-	-	V
			-80	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	$V_{GS} = -20V$	-	-	-100	nA
Gate-Source Leakage Reverse	I_{GSS}	$V_{GS} = 20V$	-	-	100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = \text{Max Rating}, V_{GS} = 0V$	-	-	-250	μA
		$V_{DS} = \text{Max Rating} \times 0.8, V_{GS} = 0V, T_C = +125^\circ\text{C}$	-	-	-1000	μA
On-State Drain Current (Note 2) IRFF9130, IRFF9131 IRFF9132, IRFF9133	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)} \text{ Max}, V_{GS} = -10V$	-6.5	-	-	A
			-5.5	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFF9130, IRFF9131 IRFF9132, IRFF9133	$r_{DS(ON)}$	$V_{GS} = -10V, I_D = -3A$	-	0.25	0.3	Ω
			-	0.3	0.4	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq I_{D(ON)} \times r_{DS(ON)} \text{ Max}, I_D = -3A$	2.5	3.5	-	S(V)
Input Capacitance	C_{ISS}	$V_{GS} = 0V, V_{DS} = -25V, f = 1.0\text{MHz}$	-	500	-	pF
Output Capacitance	C_{OSS}	See Figure 10	-	300	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	100	-	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 0.5 BV_{DSS}, I_D = -6.5A, R_G = 9.1\Omega$ See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	30	60	ns
Rise Time	t_r		-	70	140	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	70	140	ns
Fall Time	t_f		-	70	140	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	$V_{GS} = -10V, I_D = -6.5A, V_{DS} = 0.8 \text{ Max Rating}$. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	25	45	nC
Gate-Source Charge	Q_{gs}		-	13	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	12	-	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 5mm (0.2") from header to center of die.	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 5mm (0.2") from header to source bonding pad.	-	15	-	nH
						
Junction-to-Case	$R_{\theta JC}$		-	-	5.0	$^\circ\text{C/W}$
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	175	$^\circ\text{C/W}$

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.	-	-	-6.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-26	A
Diode Forward Voltage (Note 2)	V_{SD}	$T_C = +25^\circ\text{C}, I_S = -6.5A, V_{GS} = 0V$	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	$T_J = +150^\circ\text{C}, I_F = -6.5A, dI_F/dt = 100A/\mu s$	-	300	-	ns
Reverse Recovered Charge	Q_{RR}	$T_J = +150^\circ\text{C}, I_F = -6.5A, dI_F/dt = 100A/\mu s$	-	1.8	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.	-	-	-	-

NOTES: 1. $T_J = +25^\circ\text{C}$ to $+150^\circ\text{C}$

2. Pulse Test: Pulse width $\leq 300\mu s$,
Duty Cycle $\leq 2\%$

3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)

4. $V_{DD} = 25V$, Start $T_J = +25^\circ\text{C}$, $L = 17.75\text{mH}$,
 $R_G = 25\Omega$, Peak $I_L = 6.5A$ (See Figures 15 and 16)

IRFF9130, IRFF9131, IRFF9132, IRFF9133

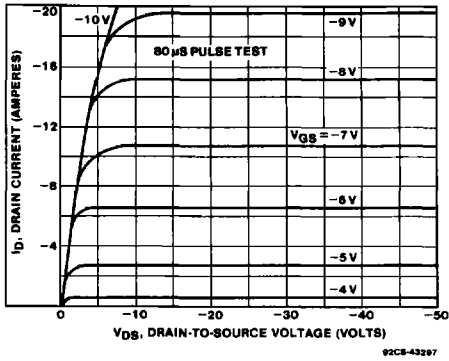


Fig. 1 - Typical Output Characteristics

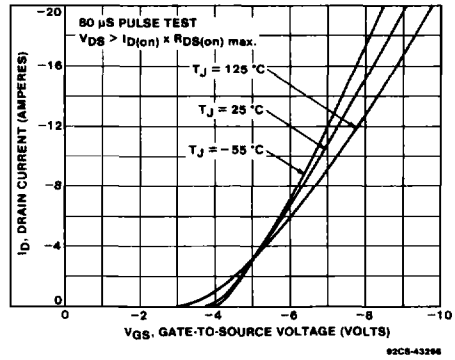


Fig. 2 - Typical Transfer Characteristics

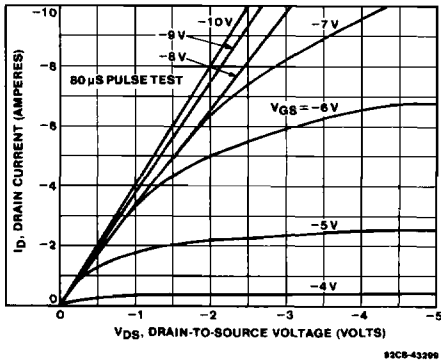


Fig. 3 - Typical Saturation Characteristics

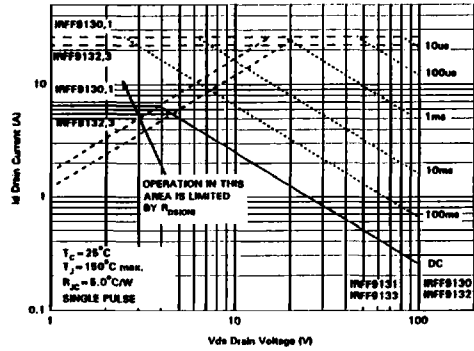


Fig. 4 - Maximum Safe Operating Area

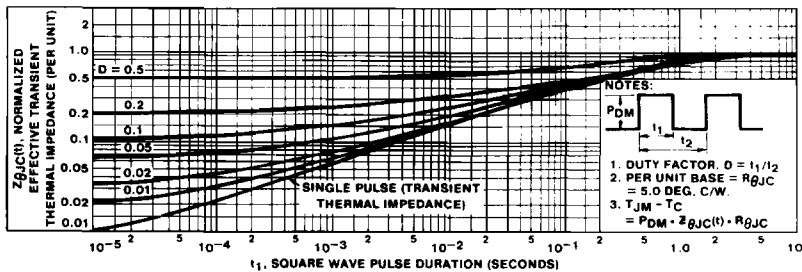


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

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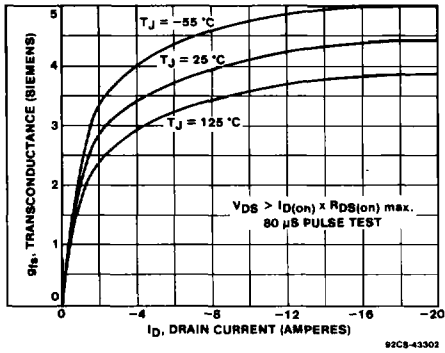


Fig. 6 - Typical Transconductance Vs. Drain Current

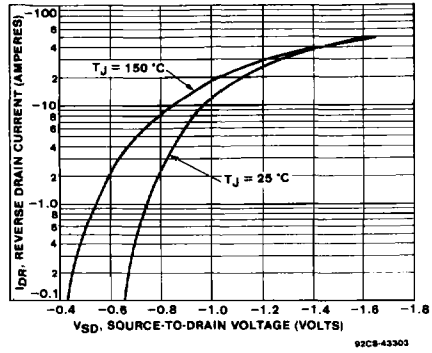


Fig. 7 - Typical Source-Drain Diode Forward Voltage

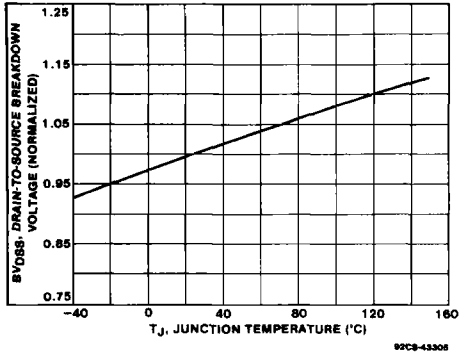


Fig. 8 - Breakdown Voltage Vs. Temperature

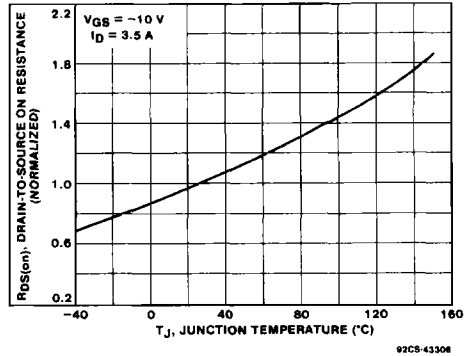


Fig. 9 - Normalized On-Resistance Vs. Temperature

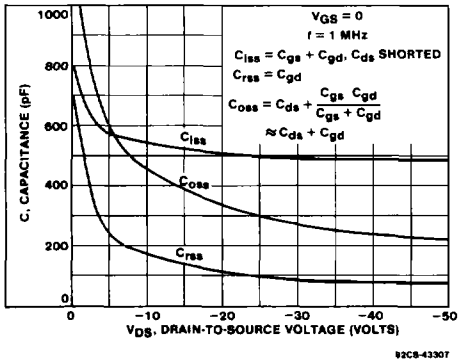


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

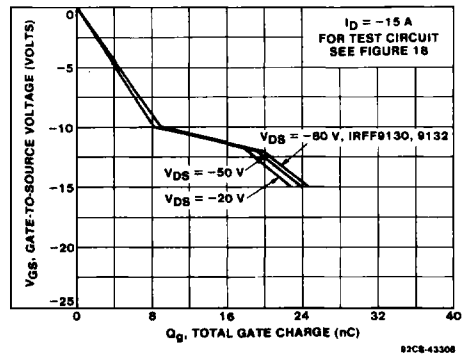


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

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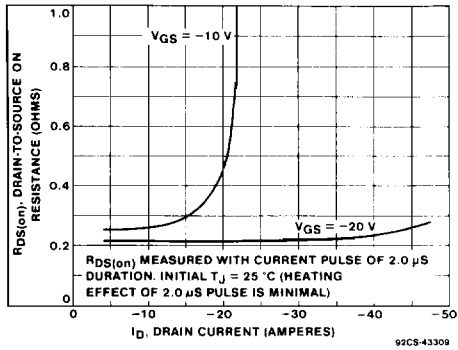


Fig. 12 - Typical On-Resistance Vs. Drain Current

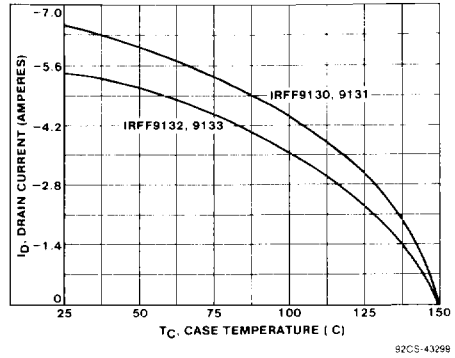


Fig. 13 - Maximum Drain Current Vs. Case Temperature

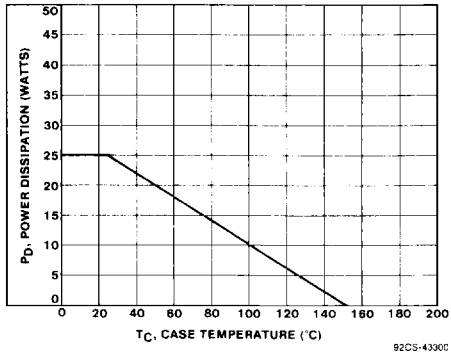


Fig. 14 - Power Vs. Temperature Derating Curve

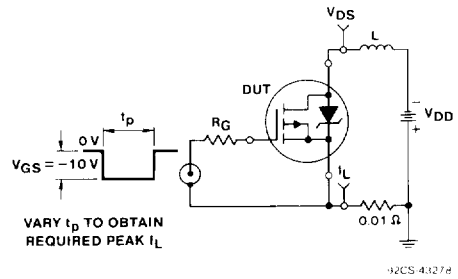


Fig. 15 - Unclamped Inductive Test Circuit

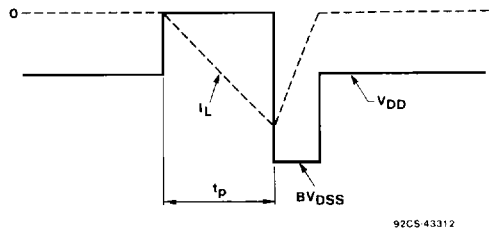


Fig. 16 - Unclamped Inductive Waveforms

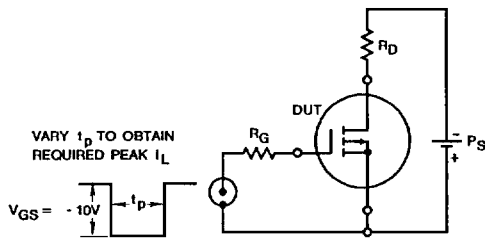


Fig. 17 - Switching Time Test Circuit

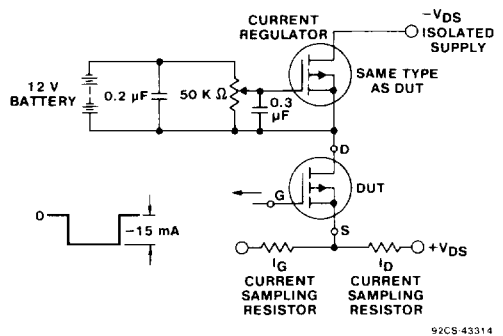


Fig. 18 - Gate Charge Test Circuit

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