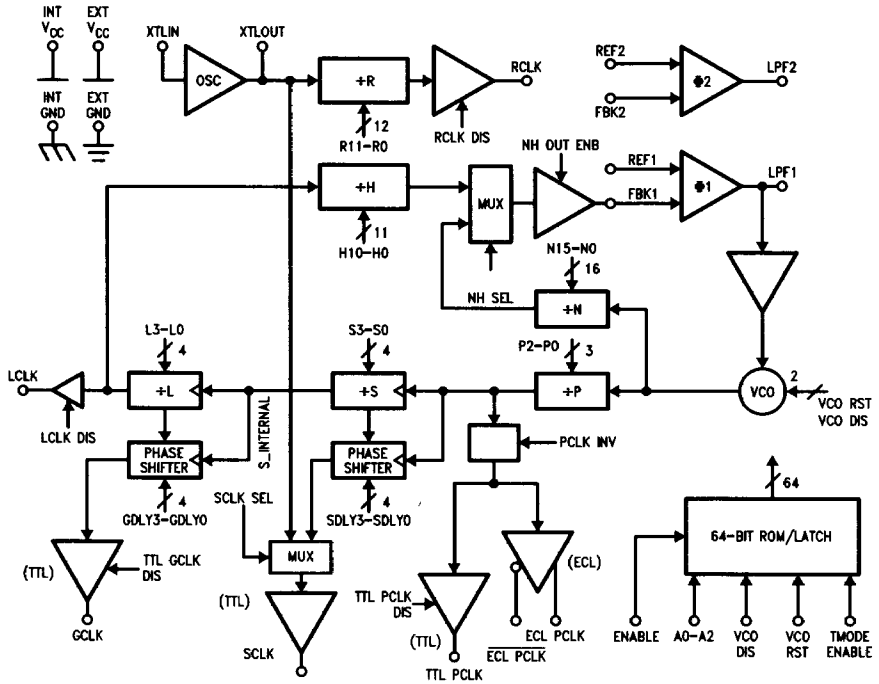
DP8532 Block Diagram



TL/F/10371–6

Pin Definitions

INPUTS

A3–A0: Address inputs. TTL compatible inputs used to select 1 of 16 address combinations. For DP8532 operation, A2–A0 are used to select one of eight user definable ROM patterns. All address information must be valid during active ENABLE time.

D3–D0: Data inputs. TTL compatible inputs used to strobe data into any one of the sixteen available registers. All data information must be valid during active ENABLE time.

ENABLE: An active high, level sensitive input. This TTL compatible input enables a data write into the DP8531. In order to modify only one desired target register per write, valid address/data must be stable, and meet the required setup and hold times throughout the active ENABLE time.

FBK1: Primary Phase detector loop input. This TTL compatible, rising edge triggered input is generally sourced from either the internal N or H counter, however, it may be fed by an external source. This pin is programmed via the NH SEL and NH OUT ENB bits. During power-up, this pin's N or H counter output may be enabled. If this pin is to be driven from an external source, precautions should be taken to avoid over-current conditions.

FBK2: Secondary Phase detector loop input. This TTL compatible, rising edge input normally used for GENLOCKing (external generator lock) applications. An example of this is

Pin Definitions (Continued)

for video application, where this input is sourced from a signal running at a horizontal line rate, or from RCLK. If the second phase detector is not used, this input should be tied to ground. For production testing, this pin serves as an input test mode, with TMODE ENABLE active for the DP8532 and TMODE ENABLE bit set for the DP8531.

LPF1: Primary Low Pass Filter Input. This pin is connected to the primary loop filter which consists of a capacitor in parallel with a resistor/capacitor series combination. Loop response is dictated by the loop divide ratio—N or H divide ratio and reference frequency; NOT by pixel clock frequency (see DP8531 Loop Filter Calculations). Refer to the section "Loop Filter Calculations" for additional information.

LPF2: Secondary Low Pass Filter Pin. This is often used in GENLOCK applications where phase alignment varies, pulls or warps the crystal oscillator frequency to a signal reference source. The secondary loop functions in conjunction with the primary loop, allowing the DP8531 to synchronize to an external frequency source.

REF1: Primary Phase detector input. This TTL compatible, rising edge triggered input is typically driven by RCLK, although an external source will serve as well. The frequency applied to this pin determines the frequency resolution of the VCO; that is, as the input frequency increases, the frequency resolution of the VCO decreases.

REF2: Secondary Phase detector input. This TTL compatible, rising edge triggered input typically serves as a secondary loop in order to GENLOCK the DP8531 to an external horizontal sync. For production testing, this pin serves as an input test mode, with TMODE ENABLE active for the DP8532 and TMODE ENABLE bit set for the DP8531.

XTLIN: Crystal input. The VCC/2 threshold allows this input to be directly driven by an external CMOS or capacitively coupled to a TTL source. The XTLIN is designed to operate with crystal, or ceramic resonator input. For crystal input applications, the crystal should be the fundamental parallel mode type. See applications diagrams for more information.

OUTPUTS

ECL PCLK, $\overline{\text{ECL PCLK}}$: Differential Pixel clock outputs. These are typically used to drive RAMDAC pixel clock inputs. Due to the inherent nature of ECL, care must be taken to properly terminate these outputs.

GCLK: Secondary Load Clock output. This TTL compatible, non-gated output is typically used in video applications to clock video shift registers, VRAM shift register or RAMDACs. This output is equivalent to the LCLK output except that it can be programmed so that its edge transitions are delayed incrementally up to 15 internal system clocks (SCLK internal) cycles.

LCLK: Load Clock output. This TTL compatible, non-gated output is typically used in video applications to clock video shift registers, VRAM shift register or RAMDACs.

SCLK: System Clock output. This TTL compatible output is typically used to drive a processor clock input. On power-up, SCLK select bit is low, thereby sourcing from XTLOUT. When SCLK select is programmed high, SCLK is sourced from the S-counter output.

RCLK: Reference clock output. This CMOS output determines the frequency resolution of the VCO when connected to the REF1 input. As the reference frequency increases, the VCO frequency resolution decreases.

TMODE ENABLE: Test mode enable. This DP8532 input is intended for test purposes only. A HIGH level input on this input will enable the FBK2 pin to function as a load strobe input for the N counter and the REF2 input to function as a VCO single step clock. For the DP8531, this function is bit programmable. Refer to the DP8531 Register Table description.

TTL PCLK: Compatible Pixel clock. This single ended output is typically used to drive pixel clocks which require TTL input characteristics.

VCO DISABLE: Voltage Controller Oscillator disable. This DP8532 active high, TTL compatible input allows the user to stop internal oscillation of the VCO in the DP8532. For the DP8531, this input is bit programmable. Refer to the DP8531 Register Table description.

VCO RESET: Voltage Controller Oscillator reset. This DP8532 active high, TTL compatible input allows the user to stop the VCO and force the LPF1 output towards ground. When a transition from a HIGH to LOW level occurs, normal VCO oscillation and loop phase lock will occur. It is recommended that on power up, or on address change selection that this pin be strobed. For the DP8531 this function is bit programmable. Refer to the DP8531 Register Table description.

XLTOUT: Crystal Output. This output is 180 degrees out of phase with XTLIN. XTLOUT is intended for crystal feedback in crystal applications, and left unconnected when XTLIN is driven by an external clock source. This output is not intended to be used as a digital output.

SUPPLIES

EXT V_{CC}: External V_{CC}. This positive power supply input sources all external output buffers intended for operation at 5V $\pm$10% relative to GND. The EXT V_{CC} and EXT GND should be adequately bypassed at the device pins.

EXT GND: External GND. Output buffer supply return. EXT GND and INT GND must be tied together.

INT GND: Internal GND. Internal analog and counter supply return. INT GND and EXT GND must be tied together.

INT V_{CC}: Internal V_{CC}. This positive power supply input sources the internal analog circuitry, and counter logic. Proper operation is from 5V $\pm$10%. Care must be taken to properly bypass this input with INT GND. INT V_{CC} and EXT V_{CC} should be tied together at the device pins.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
TTL Signals	
Inputs	7V
Outputs	7V
ECL Signals	
Output Current	−50 mA
Supplies	
EXT V_{CC} to EXT GND	−0.5V to +7V
INT V_{CC} to INT GND	−0.5V to +7V
ESD Susceptibility	500V

DC Electrical Characteristics

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{IC}	Input Clamp Voltage	V_{CC} = 4.5V	I_{IN} = −18 mA				−1.5	V
V_{OH}	Output High Voltage	V_{CC} = 4.5V	TTL Outputs (Note 2)	I_{OH} = −400 μA	V_{CC} − 2			V
			RCLK, FBK1	I_{OH} = −100 μA	V_{CC} − 0.3			V
			FBK1	I_{OH} = −4 mA	V_{CC} − 2			V
			RCLK	I_{OH} = −1 mA	V_{CC} − 2			V
			ECL Outputs 50Ω Load to V_{CC} − 2V			V_{CC} − 960		mV
V_{OL}	Output Low Voltage	V_{CC} = 4.5V	TTL Outputs (Note 2)	I_{OL} = 8 mA			0.5	V
			RCLK, FBK1	I_{OL} = 100 μA			0.3	V
			FBK1	I_{OL} = 4 mA			0.5	V
			RCLK	I_{OL} = 1 mA			0.5	V
			ECL Outputs 50Ω Load to V_{CC} − 2V			V_{CC} − 1650		mV
$\Delta V_{O(ECL)}$	ECL Logic Voltage Swing	V_{CC} = 4.5V	50Ω Load to V_{CC} − 2V		605	750	1130	mV
I_I	Max High Level Input Current	V_{CC} = 5.5V	TTL Inputs except FBK1 (Note 1)	V_{IN} = 7V			100	μA
			FBK1	V_{IN} = 5.5V			100	μA
I_{IH}	High Level Input Current		TTL Inputs (Note 1)	V_{IN} = 2.7V			±20	μA
			CMOS Input (XTLIN)	V_{IN} = 5.5V			±20	μA
I_{IL}	Low Level Input Current		TTL Inputs (Note 1)	V_{IN} = 0.4V			±20	μA
			CMOS Input (XTLIN)	V_{IN} = 0V			±20	μA
I_O	Output Drive Current		TTL Outputs (Note 2)	V_O = 2.25V	−30		−110	mA
I_{LPF}	LPF1,2 Output Current	V_{CC} = 5.0V		Source	−0.3	−0.5	−0.7	mA
				Sink	0.3	0.5	0.7	mA
				TRI-STATE®	−250	0	250	nA
I_{CC}	Supply Current	INT V_{CC} = EXT V_{CC} = 5.5V				125	200	mA

Note 1: TTL inputs are: A0 through A3, D0 through D3, ENABLE, REF1/2, TMODE ENABLE, VCO DISABLE, VCO RESET and FBK2.

Note 2: The TTL outputs are: TTL PCLK, GCLK, LCLK and SCLK.

Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Units
V_{CC} to GND	Power Supply Voltage		4.5		5.5	V
V_{IH}	High Level Input Voltage	XTLIN	$V_{CC} - 1$			V
		All Others	2			V
V_{IL}	Low Level Input Voltage	XTLIN			1	V
		All Others			0.8	V
I_{OH}	High Level Output Current TTL Outputs				−0.4	mA
	FBK1				−4	mA
	RCLK				−1	mA
I_{OL}	Low Level Output Current TTL Outputs				8	mA
	FBK1				4	mA
	RCLK				1	mA
f_{VCO}	VCO Frequency		100		210	MHz
f_{XTL}	Crystal Frequency (Note 1)				40	MHz
f_{LCLK}	LCLK Frequency (H Mode)				20	MHz
t_H	Hold Time Enable to Data or Address				25	ns
t_{SU}	Setup Time Address or Data to Enable		50			ns
t_{W1}	Enable Pulse Width	+	40			ns
t_{W2}	Pulse Width REF1, REF2, FBK1, FBK2	+	20			ns
		−	20			ns
t_{W3}	VCO Reset Pulse Width	+	100			ns
T_A	Operating Temperature Range		0		+70	°C

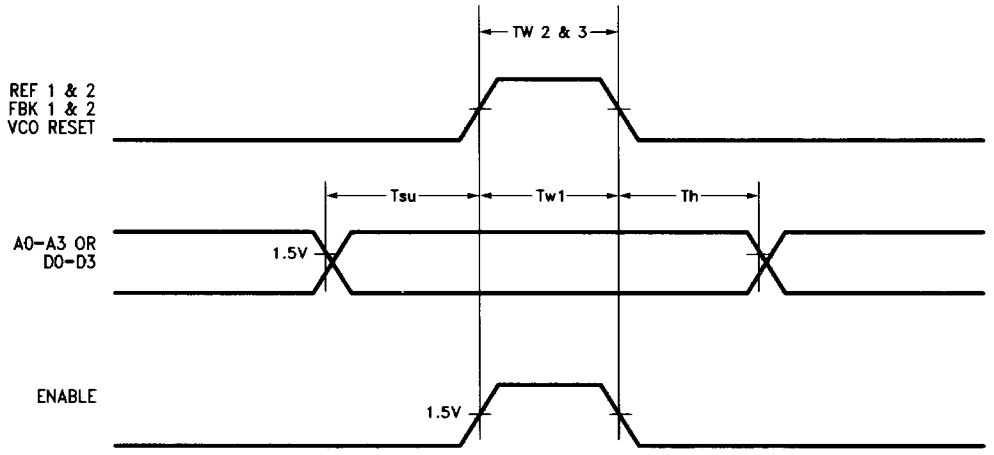
Note 1: Crystal should be parallel mode, fundamental type.

Switching Characteristics

Symbol	Parameter	Conditions	Typ	Units
t_{SKEW1}	Output Skew Time from ECL PCLK (−) to TTL PCLK (±)	V_{CC} = 4.5V to 5.5V, T_A = 0°C to +70°C	0 ±2	ns
t_{SKEW2}	Output Skew Time from TTL PCLK (−) to SCLK (±)	TTL Load: 500Ω 15 pF to Ground	3 ±5	ns
t_{SKEW3}	Output Skew Time from TTL PCLK (−) to TTL GCLK (±)	ECL Load: 50Ω Output to V_{CC} − 2V	0 ±5	ns
t_{SKEW4}	Output Skew Time from TTL PCLK (−) to LCLK (±)		0 ±5	ns
t_{SKEW5}	Output Skew Time from ECLK PCLK (−) to LCLK (±)		2 ±3	ns

Note: (−) = Transition from high to low level [Falling Edge]
(+) = Transition from low to high level [Rising Edge]
(±) = Either rising or falling edge

Timing Waveforms



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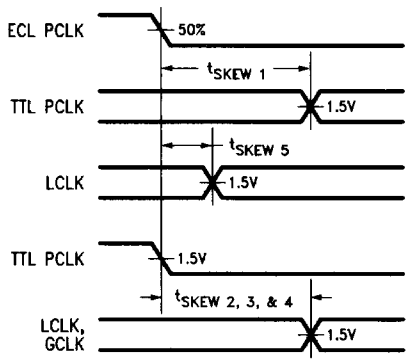

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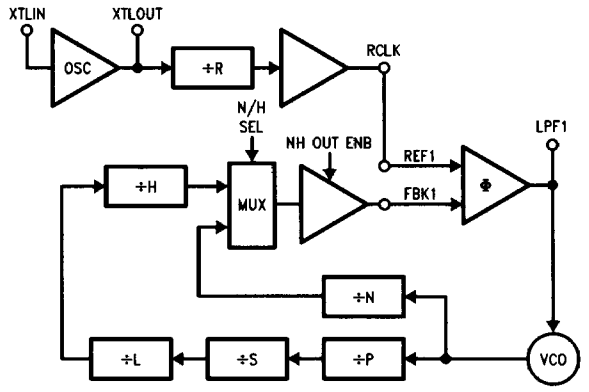
Simplified DP8531 Block Diagram



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Circuit Operation

The DP8531/32 programmable clock generators use a crystal oscillator as a frequency reference to generate several clock signals for video display systems. The clocks provided include a variety of pixel, load, system clocks, and a reference clock (RCLK) derived from the external crystal oscillator. All clock outputs are internally synchronized to simplify system timing.

This clock generator's versatility lies in the unique combination of functions such as an internal VCO, crystal oscillator, two independent phase comparators, various programmable counters and a 64-bit control register.

INTERNAL VCO OPERATION

The internal VCO has an operating range from 100 MHz to 210 MHz. No external VCO inductor or capacitor components are required for operation, thus simplifying PC board layout. The VCO has the appearance of operating over a 1-to-128 range with respect to the PCLK outputs due to the presence of the P counter. The P counter can be programmed to divide by powers of 2 between divide-by-1 and divide-by-128. These divide options, in conjunction with the VCO's 2-to-1 operating range, enable the PCLK to be programmed for operation continuously anywhere between 0.78125 MHz and 160 MHz. If for instance, a 25 MHz pixel clock frequency is desired, the P counter would be selected to divide by 8, and the VCO would operate at 200 MHz.

CRYSTAL OSCILLATOR OPERATION

Pins XTLIN and XTLOUT are used in conjunction with an external crystal, two capacitors, and two resistors to form an oscillator circuit. The crystal oscillator's output directly drives a large R counter so that a lower reference frequency (either load clock rate or horizontal line rate) can be used to lock up the VCO. The crystal oscillator output may also be directed to appear at the SCLK output by setting the SCLK SEL bit low. This bit is automatically set to select the crystal upon power up. The XTLIN pin can be driven from a CMOS logic gate directly as a system reference in lieu of using a crystal oscillator. In addition a small signal reference or a TTL reference can also be interfaced by capacitor coupling into the XTLIN pin while providing a 10 kΩ biasing resistor across the XTLIN and XTLOUT pins. The crystal oscillator can also be used as a VCXO for Genlock applications described in other sections of this circuit description.

PHASE COMPARATOR OPERATION

The phase comparators are used to control either the frequency of the internal VCO or the crystal oscillator. The phase comparator succeeds in controlling the VCO or crystal frequency by comparing the phase of a signal derived from a known accurate reference source such as a crystal or an external sync. signal. The VCO derived signal is applied to the FBK input and the reference frequency derived signal is applied to the REF input. In this manner the comparator detects whether the FBK input's positive phase transitions occur before or after the REF input's positive phase transitions and outputs a correction pulse proportional to the phase error. If the VCO is running too fast, the FBK phase transitions appear to occur first, and the phase comparator outputs a negative current pulse. The voltage across the phase comparator's loop filter will decrease and the VCO is gradually slowed down. On subsequent cycles the FBK's phase lead will diminish and the VCO will reach a stable lock condition.

Phase comparator #1 is normally used to control the internal VCO. Its feedback input is intended to be derived from the internal VCO by way of either the N counter, H counter or a horizontal counter from within an external processor. If the N or H counter paths are not selected as the return path, the NH OUT ENB bit must be programmed HIGH. This tri-states the output which is common with the FBK1 input.

Phase comparator #2 is intended to control the frequency and phase alignment of the crystal oscillator during Genlock operation. The second comparator's output, LPF2, applies a variable DC bias across a varactor during Genlock operation which influences the crystal's oscillation frequency. The REF2 input of the second phase comparator is usually an external horizontal sync signal. To successfully achieve Genlock, the signal applied to the FBK2 input must be very close to the external sync frequency, but derived from the crystal oscillator (usually by way of the R counter).

PROGRAMMABLE DIVIDER OPERATION

There are six programmable dividers within the device. The modulus of these dividers in the DP8531 is programmed by the control registers as shown in the Control Register section of this data sheet. The modulus of these dividers in the DP8532 is fixed by the ROM.

The R (reference) divider provides a reference frequency from a low cost crystal oscillator output. The R divider's modulus range is from 2 to 4095. The modulus is programmed using control address words 4, 5, and 6. The modulus selected is the direct binary equivalent loaded in the register. The duty cycle of the divider's output is a one crystal oscillator period wide LOW pulse and an R − 1 crystal oscillator periods wide HIGH pulse.

The P (pixel) divider provides a means of generating a pixel clock over a wide frequency range from a VCO which has a fixed frequency range. The modulus selections of the P divider are powers of 2 from 1 to 128. Because the range of the VCO has a two-to-one range, it is possible to cover a continuous pixel clock range of from 0.78125 MHz to 160 MHz. The modulus of this counter is programmed within control address word 9. The modulus selected is two raised to the binary power loaded in the register as shown in the Control Register table.

The S (system clock) divider provides a means of obtaining a system clock output which is some multiple higher frequency than the load clock. The modulus range of the S divider is between 1 and 16. The modulus is programmed using control address word 7. The modulus selected is the binary equivalent loaded into the register plus one. The duty cycle of an even divide modulus is 50% and an odd divide modulus is one pixel clock period short of being HIGH for 50%. When the S counter is selected for divide by one, the L counter is driven at the pixel clock rate however the SCLK output is disabled.

The L (load clock) divider in conjunction with the S divider provides a means of obtaining a load clock output which is sychronous with the pixel clock output but at a rate which is lower than P by the product of the S and L counters. The modulus range of the L divider is between 1 and 16. The modulus is programmed using control address word 8. The modulus selected is the binary equivalent loaded into the register plus one. The duty cycle of an even divide modulus

Circuit Operation (Continued)

is 50% and an odd divide modulus is one pixel clock period short of being HIGH for 50%. When the L counter is selected for divide by one, the H counter and the LCLK outputs are disabled.

The S and L counters also feature a phase shifting capability of the GCLK and SCLK outputs to ease the designer's task of aligning clock edges in backplane applications. The phase shifting for each counter is independently programmed using control address words 14 and 15 as shown in the Control Register Table. Word 14 is used to set the phase of the SCLK. The phase is equal to the decimal equivalent number of pixel clocks (PCLK) delayed from the rising edge of the LCLK. Word 15 is used to set the phase of the GCLK. The phase is equal to the decimal equivalent number of internal system clocks (SCLK internal) delayed from the rising edge of the LCLK.

The H (horizontal) divider provides a means of synchronizing the load clock output to the horizontal line rate without the requirement for a graphics processor to provide the horizontal line counter function. The modulus range of the H counter is from 3 to 2048. The modulus is programmed using control address words 1 through 3. The modulus selected is the binary equivalent loaded into the register plus one. The output for the H divider must be enabled using the NHout ENB and N/H SEL bits within control address word 11. The duty cycle of the H divider's output is a one LCLK period wide HIGH pulse and an H − 1 LCLK period wide LOW pulse.

The N divider provides a means of locking the VCO with a constant tuning resolution that is independent of the pixel, system, and load clock divider requirements. The penalty paid for operation in this mode is that the phase of the FBK input is not necessarily an integer of LCLK nor is its phase relationship always consistant relative to LCLK. The "continuous" modulus range of this divider is 961 to 65,535. The N counter can be used in the non-continuous mode. Valid N modulus below 961 are shown in a table later in this data sheet. The modulus is programmed using control address words 0 through 3. The modulus selected is the binary equivalent loaded into the register. The output for the N divider must be enabled using the NHout ENB and N/H SEL bits within control address word 11. The duty cycle of the N divider's output is a 32 VCO clock periods wide HIGH pulse and an N − 32 VCO clock periods wide LOW pulse.

CONTROL REGISTER OPERATION

The Control Register provides a convenient means to program the various functions within the DP8531. Inputs to the control register for the DP8531 consist of nine lines; four for Address, four for Data and one as an enable input. The address and data bits must be stable (no transitions), for a specified time before the positive transition of the enable input and during the complete positive pulse, to ensure proper entry of these bits. To program a function, Address and Data bits are set, followed by a positive pulse on the enable input. Details on the Control Register are given in the DP8531 Register Table section. Inputs to the control register for the DP8532 consist of four lines; three select lines (A0 through A2) and an enable input. The three select lines choose one of eight predefined operating conditions.

POWER-UP CONDITIONS

At power-up the Control Register bits are set to provide initial operating conditions as follows:

1. SCLK SEL bit is initialized low to select the crystal reference as the SCLK clock output reference.
2. The DP8531 VCO DIS bit is initialized low. This ensures the VCO is enabled. DP8532 VCO DISABLE pin should be tied low at all times unless it is desired to occasionally shut down the VCO.
3. TMODE EN bit is initialized low. This places the DP8531 in a normal operating condition. The DP8532 TMODE EN pin should be set low for normal operation.
4. During the initialization sequence after power-up, for the DP8531 it is recommended that the VCO RST bit be programmed HIGH. This causes the VCO to reset, and after a short period of time, to re-start. The VCO RST bit is internally reset upon completion of the internal restart sequence. In the case of the DP8532, the VCO RESET pin should be pulsed high during power-up and subsequently returned low.
5. The DP8532 output conditions will depend upon the state of EN, A2, A1, and A0 at the time of power-up.
6. All other bits in the DP8531 are **not** dictated at power-up and must be loaded as shown in the typical register loading sequence.

DP8531 Register Table

Address	Address Bits				Data Bits			
	A3	A2	A1	A0	D3	D2	D1	D0
0	0	0	0	0	N3	N2	N1	N0
1	0	0	0	1	N7/H2	N6/H1	N5/H0	N4
2	0	0	1	0	N11/H6	N10/H5	N9/H4	N8/H3
3	0	0	1	1	N15/H10	N14/H9	N13/H8	N12/H7
4	0	1	0	0	R3	R2	R1	R0
5	0	1	0	1	R7	R6	R5	R4
6	0	1	1	0	R11	R10	R9	R8
7	0	1	1	1	S3	S2	S1	S0
8	1	0	0	0	L3	L2	L1	L0
9	1	0	0	1	PCLK INV	P2	P1	P0
10	1	0	1	0	TTLPCLK DIS	TTLGCLK DIS	LPF1 DIS	LPF2 DIS
11	1	0	1	1	NH OUT ENB	NH SEL	SCLK SEL	TMOD EN
12	1	1	0	0	VCO DIS	VCO RST	IRING1	IRING0
13	1	1	0	1	RCLK DIS	(NOT USED)	(NOT USED)	LCLK DIS
14	1	1	1	0	SDLY3	SDLY2	SDLY1	SDLY0
15	1	1	1	1	GDLY3	GDLY2	GDLY1	GDLY0

ADDRESS 0 to 3

These data bits (D3–D0) represent either the desired N or H counter modulus in binary. The modulus selection, of whether N or H modulus is selected, is determined by the status of the NH SEL bit (word 11, bit D2).

The H counter's modulus is equal to the binary value of the H bits plus one, where H0 is the least significant bit (LSB). The minimum H counter modulus is 3, while the maximum is 2,048.

The N counter's modulus is equal to the binary value of the N bits where N0 is the LSB. The minimum continuous N counter modulus is 961 as governed by the following equation.

$$N \text{ modulus} = 32 (B - \overline{A}) + 31 (1 + \overline{A})$$

where

B is the eleven more significant bits of N and $\overline{A}$ is the inverse of the five least significant bits of N.

B (Min) = 2
$\overline{A}$ (Max) = B

The non-continuous region of the N counter (values less than 961) can be used for some modulus values. A table of legal modulus values is included after the modulus tables later in the data sheet. The maximum value of the N counter modulus is 65,535.

ADDRESS 4 to 6

These data bits (D3–D0) represent the desired R counter modulus in binary, where R0 is the LSB. The R counter's modulus is equal to the binary value of the data bits. The minimum valid R modulus is 2 while the maximum value is 4,095.

ADDRESS 7

These data bits (D3–D0) represent the desired S counter modulus in binary, where S0 is the LSB. The S counter's modulus is the binary value of these bits plus 1. The selection of S = 0000 produces a static logic LOW level at the output of SCLK while internally presenting P divided by one to the L counter. The minimum valid S modulus is 1 while the maximum value is 16.

ADDRESS 8

These data bits (D3–D0) represent the desired L counter modulus in binary, where L0 is the LSB. The L counter's modulus is the binary value of these bits plus 1. The selection of L = 0000 produces a static logic LOW level at the output of LCLK and prevents the H counter from dividing. The minimum valid L modulus is 2 while the maximum value is 16.

ADDRESS 9

The three least significant data bits of this address (D2–D0) represent the desired P counter modulus. The P counter's modulus is equal to two raised to the power of the decimal equivalent of these binary bits. The minimum valid P modulus is 1 while the maximum value is 128.

The most significant data bit of this address (D3) selects whether the PCLK outputs true or inverted (PCLK INV) data. A LOW level selects a true output while a HIGH level selects an inverted output.

ADDRESS 10

The least significant data bit of this address (D0) selects whether the LPF2 pin is disabled or enabled (LPF2 DIS). A HIGH level disables the second phase detector from issuing charge pump pulses thereby tri-stating the LPF2 pin while a LOW level selects the LPF2 to be enabled.

The second least significant data bit of this address (D1) selects whether the LPF1 pin is disabled or enabled (LPF1 DIS). A HIGH level disables the first phase detector from issuing charge pump pulses thereby tri-stating the LPF1 pin while a LOW level selects the LPF1 to be enabled.

The third least significant data bit of this address (D2) selects whether the TTL GCLK output is disabled or enabled (TTL GCLK DIS). A HIGH level selects the TTL GCLK output pin to be disabled to a high logic level while a LOW level selects the TTL GCLK output pin to be enabled.

The most significant data bit of this address (D3) selects whether the TTL PCLK output is disabled or enabled (TTL PCLK DIS). A HIGH level selects the TTL PCLK output pin to be disabled to a high logic level while a LOW level selects the TTL PCLK output pin to be enabled.

ADDRESS 11

The least significant data bit of this address (D0) selects whether the VCO test mode (TMOD EN) is disabled or enabled. A LOW level selects the VCO test mode to be disabled (normal operation) while a HIGH level selects the VCO test mode to be enabled.

The second least significant data bit of this address (D1) selects whether the SCLK is referenced from the crystal or the S counter (SCLK SEL). A LOW level selects the crystal to be the reference of the SCLK while a HIGH level selects the S counter as the SCLK reference.

The third least significant data bit of this address (D2) selects whether the data entered in the first four address words are either H or N modulus (NH SEL). A LOW level selects the H counter mode while a HIGH level selects N counter mode.

The most significant data bit of this address (D3) selects whether the FBK1 (N/H counter output) is tri-stated or enabled (NH OUT ENB). A HIGH level selects the FBK1 output pin to be tri-stated while a LOW level selects the FBK1 output pin to be enabled.

ADDRESS 12

The two least significant bits of this address (D1,D0) select the ring oscillator current mirror ratio (IRING1:IRING0). For normal operation both these bits are set to a LOW level. The other combinations of these bits are intended for NSC test purposes only.

The third least significant data bit of this address (D2) selects whether the VCO reset is activated or not (VCO RST). A HIGH level activates the VCO reset function. This sequence includes momentarily driving the LPF1 pin towards ground and stopping the VCO from oscillating. After the VCO restarts the RST bit is automatically returned LOW.

The most significant data bit of this address (D3) selects whether the VCO is disabled or enabled (VCO DIS). A LOW level selects the VCO to be enabled while a HIGH level selects the VCO to be disabled from oscillating.

ADDRESS 13

The least significant bit of this address (D0) selects whether the LCLK output is enabled or disabled (LCLK DIS). A LOW level selects the LCLK output to be enabled while a HIGH level selects the LCLK output to be disabled to a HIGH logic level.

The second and third least significant bits of this address are unused.

The most significant bit of this address (D3) selects whether the RCLK output is enabled or disabled (RCLK DIS). A LOW level selects the RCLK output to be enabled while a HIGH level selects the RCLK output to be disabled to a HIGH logic level.

ADDRESS 14

These data bits (D3–D0) represent the desired number of pixel clock cycles of phase delay between the SCLK output and the S internal clock, which drives the L counter (SDLY3–SDLY0). The phase delay is equal to the decimal equivalent number of pixel clocks (PCLK) delayed from the rising edge of the LCLK. The minimum delay is 0 while the maximum delay is 15 pixel clocks.

ADDRESS 15

These data bits (D3–D0) represent the desired number of S internal clock cycles of phase delay between the GCLK and the LCLK (GDLY3–GDLY0). The phase shift is equal to the decimal equivalent number of internal system clocks (S internal) delayed from the rising edge of the LCLK. The minimum delay is 0 while the maximum delay is 15 internal S clocks.

Modulus Tables

Modulus*	N Modulus Table															
	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0
961 (Min)	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	1
962	0	0	0	0	0	0	1	1	1	1	0	0	0	0	1	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
65,534	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
65,535 (Max)	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

*See non-continuous region N counter modulus table for valid codes less than 961.

Modulus	H Modulus Table										
	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0
3 (Min)	0	0	0	0	0	0	0	0	0	1	0
4	0	0	0	0	0	0	0	0	0	1	1
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
2,047	1	1	1	1	1	1	1	1	1	1	0
2,048 (Max)	1	1	1	1	1	1	1	1	1	1	1

Modulus	R Modulus Table											
	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
2 (Min)	0	0	0	0	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	0	0	0	0	1	1
•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•
4,094	1	1	1	1	1	1	1	1	1	1	1	0
4,095 (Max)	1	1	1	1	1	1	1	1	1	1	1	1

Modulus	L or S Modulus Table			
	(L or S)3	(L or S)2	(L or S)1	(L or S)0
1 (Min)	0	0	0	0
2	0	0	0	1
•	•	•	•	•
•	•	•	•	•
15	1	1	1	0
16 (Max)	1	1	1	1

Delay	Phase Shift Table			
	$(SDLY \text{ or } GDLY)_3$	$(SDLY \text{ or } GDLY)_2$	$(SDLY \text{ or } GDLY)_1$	$(SDLY \text{ or } GDLY)_0$
0 (Min)	0	0	0	0
1	0	0	0	1
•	•	•	•	•
•	•	•	•	•
14	1	1	1	0
15 (Max)	1	1	1	1

Modulus Tables (Continued)

P Modulus	P2	P1	P0
1	0	0	0
2	0	0	1
4	0	1	0
8	0	1	1
16	1	0	0
32	1	0	1
64	1	1	0
128	1	1	1

N Counter Modulus Table (Non-Continuous Region)

The following table lists the valid N counter modulus's below the minimum continuous modulus of 961. They occur in a sequential order which obeys the equation:

$$N = 32(B - \overline{A}) + 31(1 + \overline{A})$$

where A = the 5 least significant bits of N
B = The 11 most significant bits of N
B min = 2
$\overline{A}$ max = B

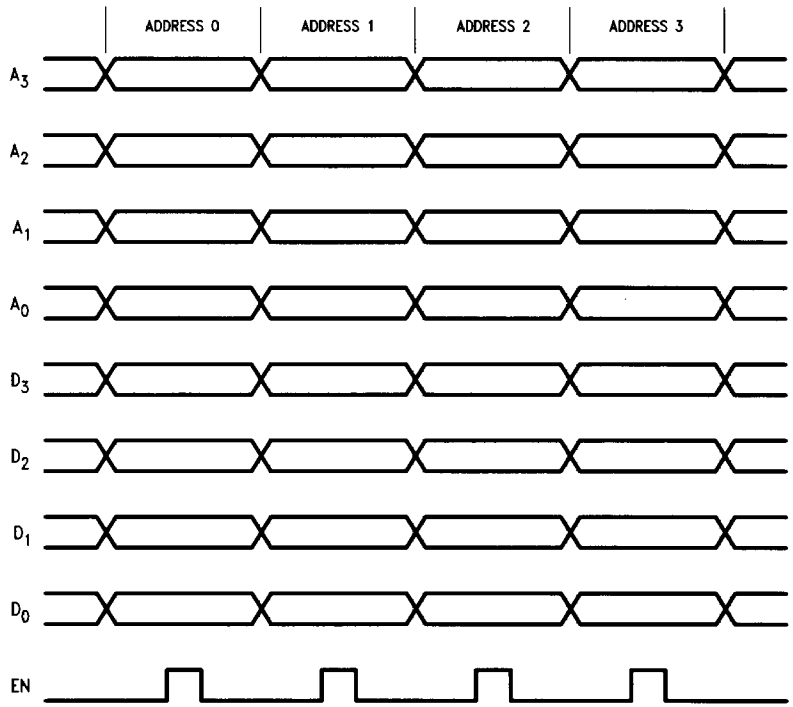
93–95	310–319	527–543	744–767
124–127	341–351	558–575	775–799
155–159	372–383	589–607	806–831
186–191	403–415	620–639	837–863
217–223	434–447	651–671	868–895
248–255	465–479	682–703	899–927
279–287	496–511	713–735	930–959

One method to determine if a given N value is a legal modulus is to see if it satisfies the following:

$N \geq 93$ and

$N < 32 * \text{INT}(N/31)$

Typical Register Loading Sequence



TL/F/10371–9

Loop Filter Calculations

Several constants need to be known in order to determine the loop filter components. They are the loop divide ratio, N, the phase detector gain, Kp, the VCO gain, Ko, the loop bandwidth, ωo, and the phase margin, F. The constants Kp and Ko for the DP8531 are fixed at 80 μA/rad and 2.5E9 radians/V. N is equal to the VCO frequency divided by the frequency input at FBK1. ωo is recommended to be less than 1/20th of the FBK1 frequency (times 2π rads). Having found all these constants, the following equations are used to find the component values:

For F = 57 degrees phase margin:

$$R1 = 1.1\ N\ \omega o/Kp\ Ko$$

$$C1 = 3\ Kp\ Ko/N\ \omega o^2$$

$$C2 = 0.3\ Kp\ Ko/N\ \omega o^2$$

For a phase margin other than 57 degrees:

$$R1 = (\text{Cosec } F + 1)\ (N\ \omega o/2\ Kp\ Ko)$$

$$C1 = (\text{Tan } F)\ (2\ Kp\ Ko/N\ \omega o^2)$$

$$C2 = (\text{Sec } F - \text{Tan } F)\ (Kp\ Ko/N\ \omega o^2)$$

Let us now design an example system with the following characteristics:

- 20 MHz external resonator
- 1024 x 1024 monitor resolution
- 60 Hz refresh rate
- 13% overhead on refresh (69.44 kHz external Horiz. sync = 60 Hz × 1024 × 1.13)
- Dot clock rate (Pixel clock, PCLK) of 80.56 MHz (69.44 kHz × 1024 × 1.13)
- System clock rate of 20 MHz (SCLK)
- Load clock rate of 10 MHz (LCLK) (8-bit wide video shift register: PCLK/LCLK = 8)

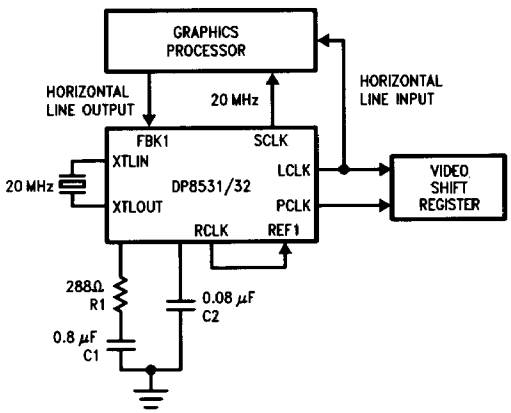
Since the desired PCLK frequency of 80 MHz is approximately a factor of 2 below the VCO's direct operating range of 100 MHz to 200 MHz, the P counter will be programmed for division by 2. The VCO frequency will thus be driven to 160 MHz to get the required 80 MHz PCLK operation. The S block must then be set to divide-by-4 and the L block to divide-by-2 to get the chosen SCLK and LCLK. The R block must be set to divide-by-288 to reduce the 20 MHz resonator clock to the 69.44 kHz needed for the REF1 input. N is equal to 2320, the 160 MHz VCO frequency divided by 69.44 kHz. We will also set ωo to be about 1/30th of the external horizontal sync or 14.6 krads.

From these values we get:

$$C1 = 0.8\ \mu F \qquad C2 = 0.08\ \mu F$$

$$\text{and } R1 = 288\Omega.$$

Example of System Used for Loop Filter Calculation

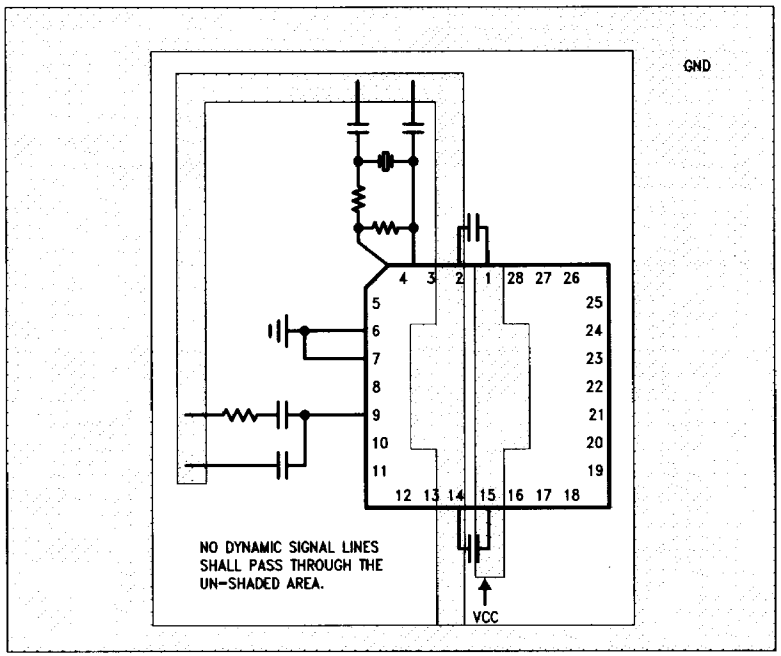


TL/F/10371-10

DP8531 Layout Considerations

- This device is sensitive to noise on certain pins, especially LPF1, LPF2 (if used), and the V_{CC} and GND pins. Special care must be taken with board layout if optimum performance is to be obtained.
- The part should be bypassed between the EXT VCC and EXT GND as close to the chip as possible (preferably under the chip using chip caps).
- No dynamic signal lines should pass through the resonator or LPF circuitry areas to avoid the possibility of noise due to crosstalk.
- The INT GND pin and the ground for the resonator circuitry should be on the same ground branch and be connected to the EXT GND pin only.
- If using a multilayered board with dedicated V_{CC} and GND planes ensure that for the ground plane that the resonator circuitry has its own small isolated island that is connected to the INT GND and EXT GND pins as shown in the recommended layout drawing. In addition, a GND island should be set up for the LPF circuitry as shown in the same drawing.

DP8531 Layout Considerations



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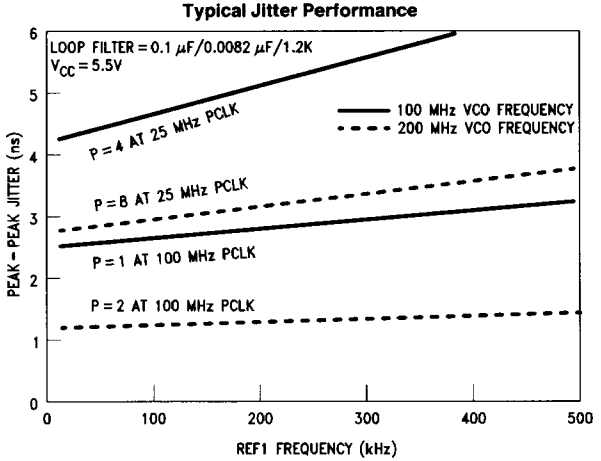
Typical Jitter Performance



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Jitter Minimization Techniques

The following items will assist the user in obtaining the best possible jitter performance from the DP8531/32. They are listed in order of importance. Be aware, however, that jitter in the clock outputs is a function of **externally** coupled noise (via V_{CC}, GND, and LPF lines) as well as the noise intrinsic to the chip itself.

1. **Maximize the VCO frequency whenever possible.** For example, pixel frequencies between 50 MHz and 52.5 MHz can be programmed with a VCO frequency equal to twice the pixel rate (P = 2) or four times the pixel rate (P = 4) since the VCO frequency spec is 100 MHz–210 MHz.
2. **Shut off all unused outputs.** This may include TTL PCLK, GCLK, SCLK and LCLK. Outputs are disabled by loading their respective control bits high in the program registers. The SCLK is disabled by loading SCLK SEL high (to select the S counter output) and also setting the S modules to 1. The S internal signal will still clock the L counter. The LPF2 pin is tri-stated by loading the LPF2 DIS bit high (also be sure to tie REF2 and FBK2 to ground if the secondary phase comparator is not used).
3. **Determine the best reference frequency for the primary loop.** This is the frequency seen at the inputs to the phase comparator. From what we have observed to date, the jitter is usually best with high reference frequencies (>500 kHz) when the device is operated in a noisy environment. This is because the loop is able to track out the high frequency noise that is modulating the VCO. However, on the demo board, a "clean" environment, jitter appears to be slightly lower at lower reference rates in the range of 10 kHz–100 kHz.
4. **Optimize loop filter component values.** The data sheet contains equations for calculating the standard loop filter with 57 degree phase margin. Do not hesitate to try variations on these values. One possibility is doubling or tripling the value of the resistor. Another is varying the ratio of the capacitors. 10:1 is standard, but a reasonable range is 5:1 up to 30:1.
5. **If possible, operate the device at a reduced V_{CC}.** Values between 4.5V and 5.0V will reduce internal digital noise and improve the clocks.

DP8532-AB ROM Mask Output Frequencies

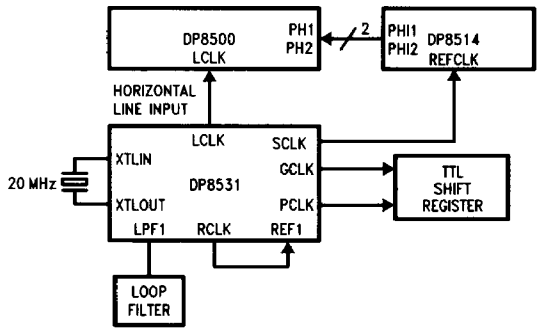
Address		PCLK	RCLK	SCLK	LCLK	VCO	PCLK/XTAL Ratio
DEC	BIN						
0	000	25.18939	0.53030	6.29735	3.14867	100.75756	1.75926
1	001	28.33807	1.19318	7.08452	3.54226	113.35226	1.97917
2	010	32.51420	0.59659	8.12855	4.06428	130.05680	2.27083
3	011	44.86363	0.95455	11.21591	5.60795	179.45452	3.13333
4	100	50.37878	0.53030	12.59470	6.29735	100.75756	3.51852
5	101	65.02840	0.59659	16.25710	8.12855	130.05680	4.54167
6	110	80.01336	0.84225	20.00334	10.00167	160.02672	5.58824
7	111	40.00668	0.84225	10.00167	5.00084	160.02672	2.79412

Note: All above frequencies in MHz
Nominal Crystal Frequency = 14.31818 MHz
PCLK = Pixel Clock (ECL or TTL)
RCLK = Reference Clock
SCLK = System Clock (Programmed to be S Counter Output)
LCLK = Load Clock
All Outputs Enabled

DP8532-AB ROM Mask Counter Values

Counter	Address							
	0	1	2	3	4	5	6	7
R	27	12	24	15	27	24	17	17
S	4	4	4	4	4	4	4	4
L	2	2	2	2	2	2	2	2
H	0	0	0	0	0	0	0	0
SDLY	2	2	2	2	2	2	2	2
GDLY	1	1	1	1	1	1	1	1
N	190	95	218	188	190	218	190	190
P	4	4	4	4	2	2	2	4

Typical System Configuration



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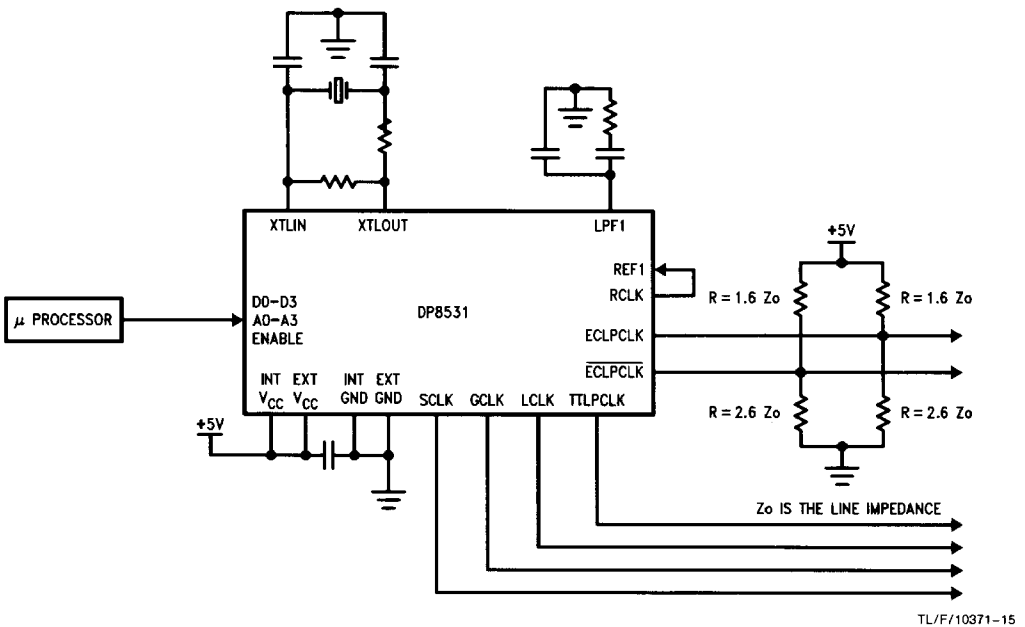
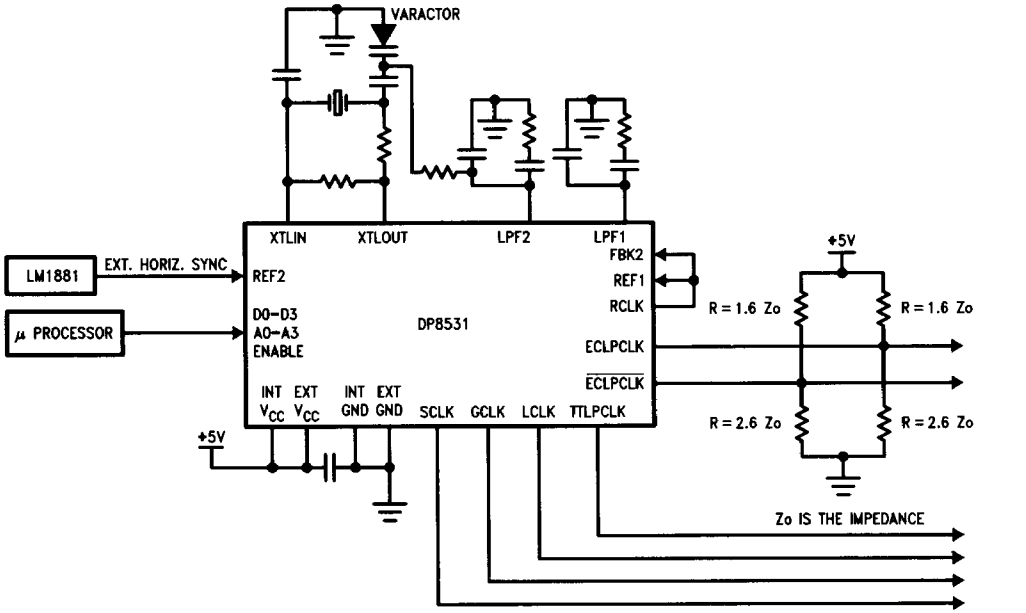
DP8531 General Wiring Diagram



TL/F/10371–15

DP8531 General Wiring Diagram with External Reference System (Genlock)



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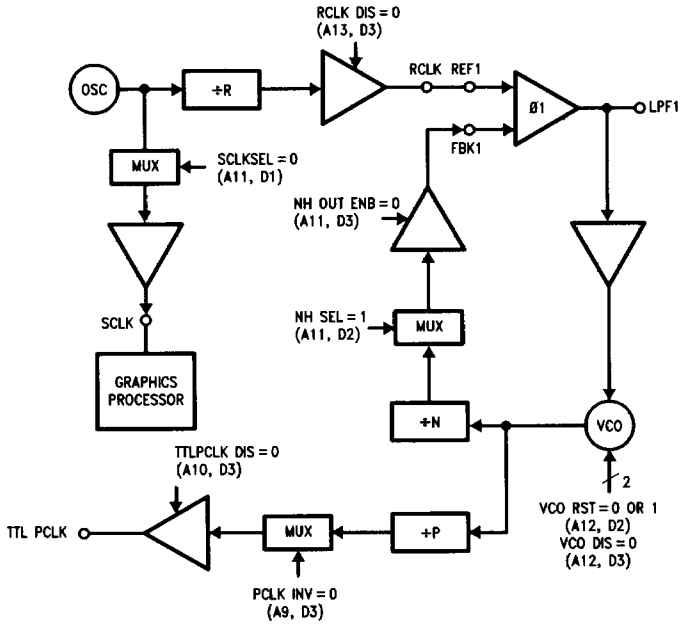
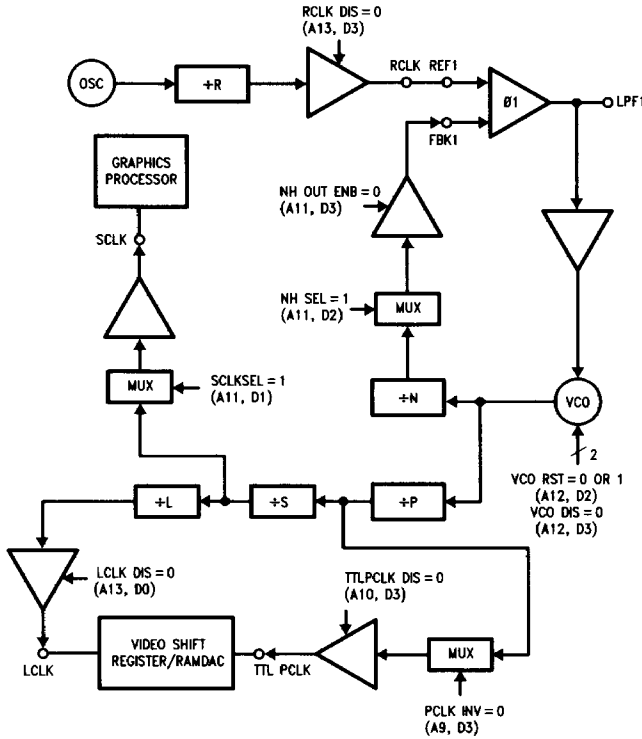
Application Diagram 1



TL/F/10371–17

Application Diagram 2



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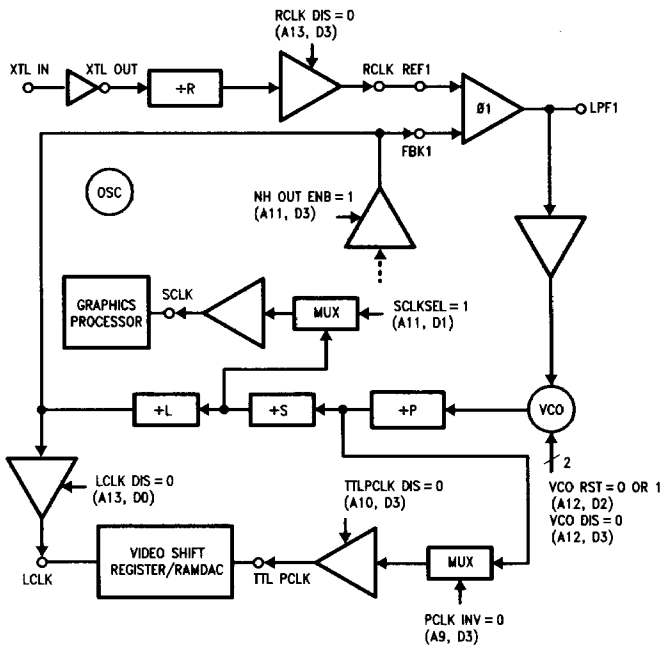
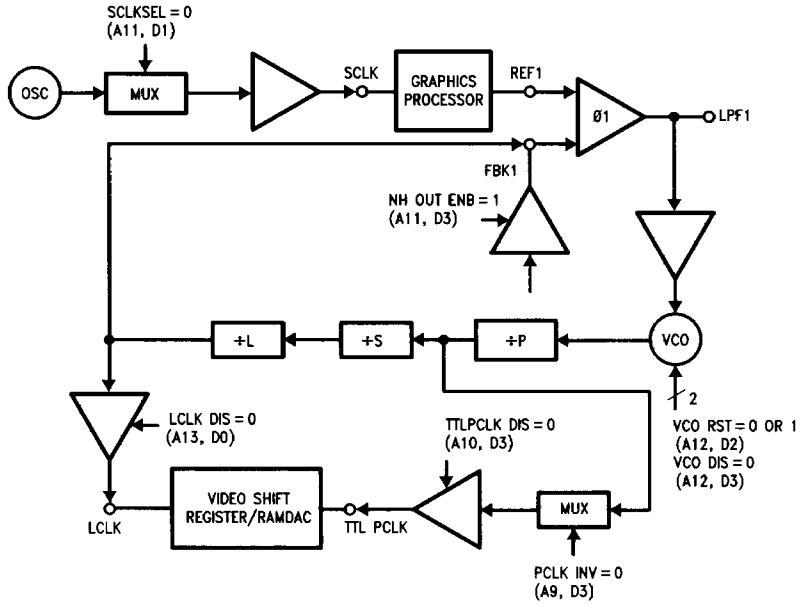
Application Diagram 3



TL/F/10371–19

Application Diagram 4



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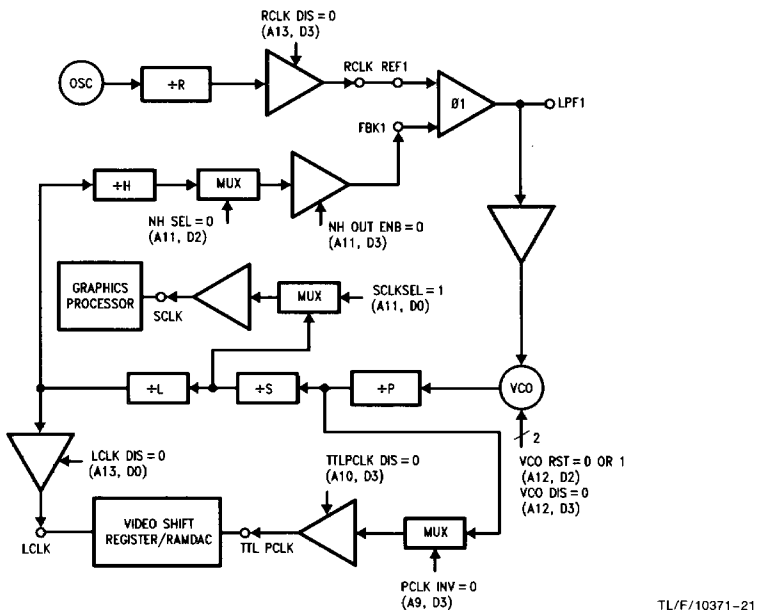
Application Diagram 5



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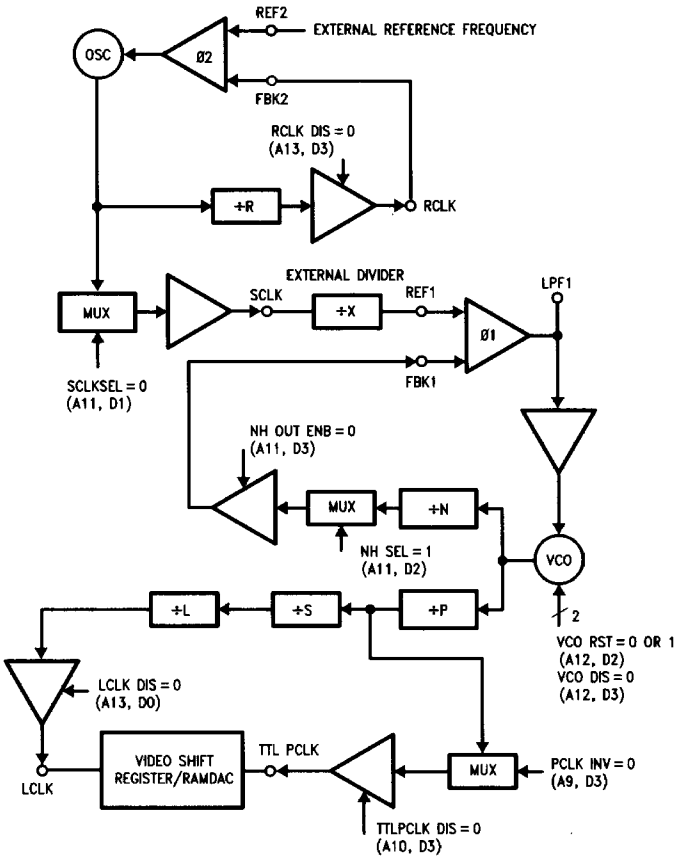
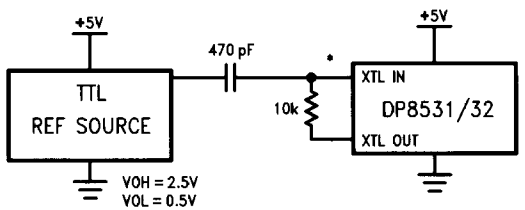
Application Diagram 6



TL/F/10371-22

DP8531 Application Method of Driving Crystal Input with TTL or Small Signal Input



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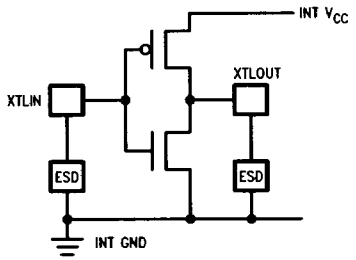
*XTLIN has a CMOS (i.e., $V_{CC}/2$) input threshold voltage. 10 kΩ resistor biases inverting gate at its $V_{CC}/2$ threshold.

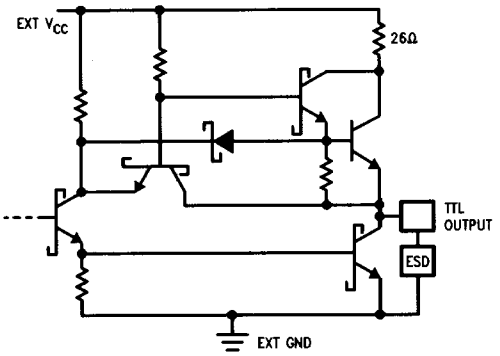
Input/Output Structures

XTL In, XTL Out



TL/F/10371–23

TTL Outputs (TTL PCLK, SCLK, TTL GCLK, LCLK)



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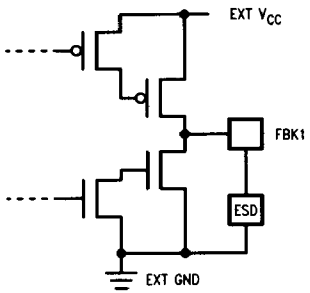
FBK1 Output Buffer



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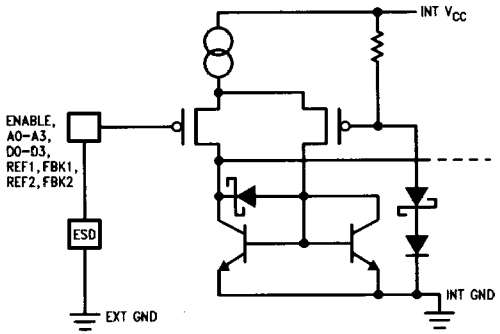
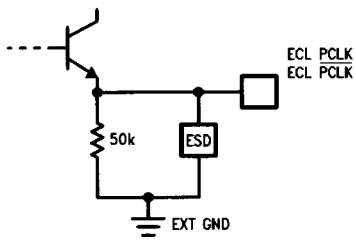
Enable, A0–A3, D0–D3, REF1, FBK1, REF2, FBK2



TL/F/10371–28

ECL PCLK, $\overline{\text{ECL PCLK}}$



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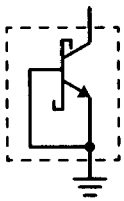
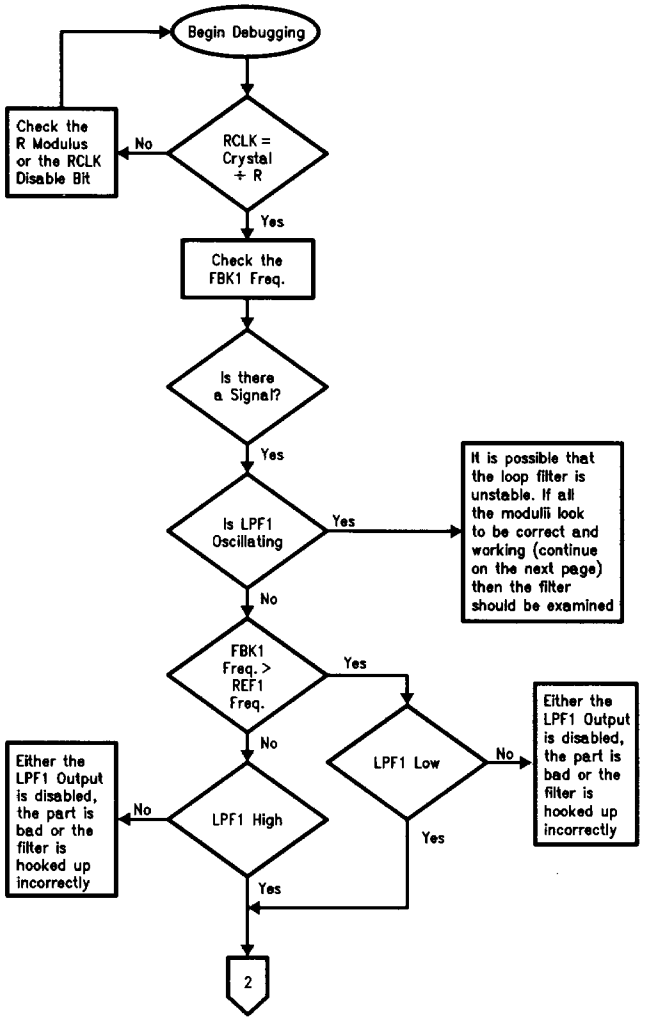
Typical ESD Structure



TL/F/10371–27

DP8531 System Debugging Flowchart



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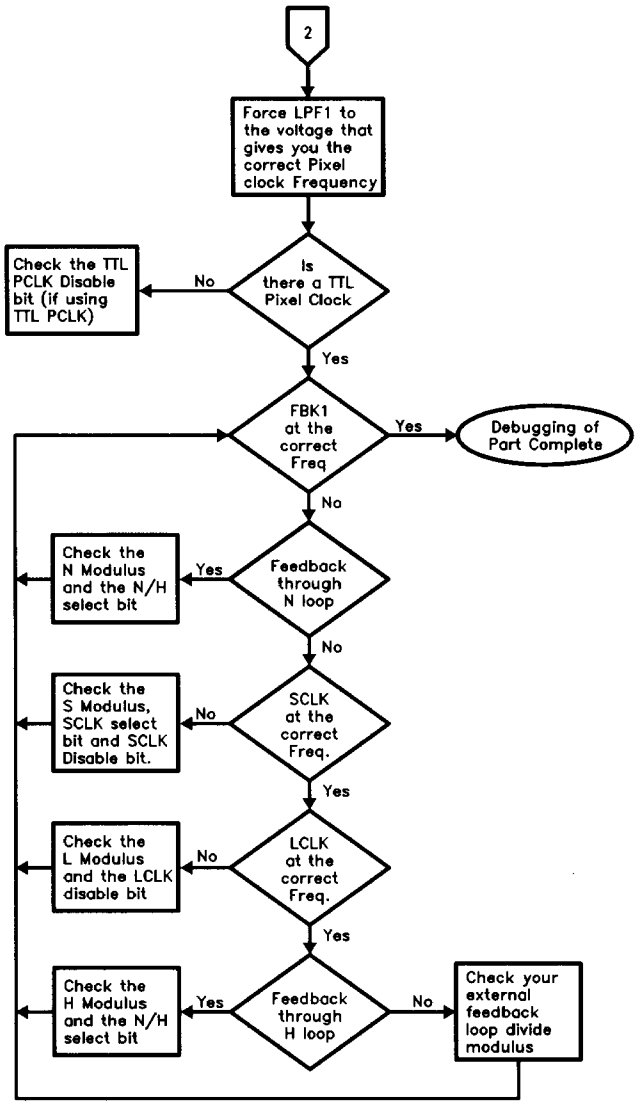
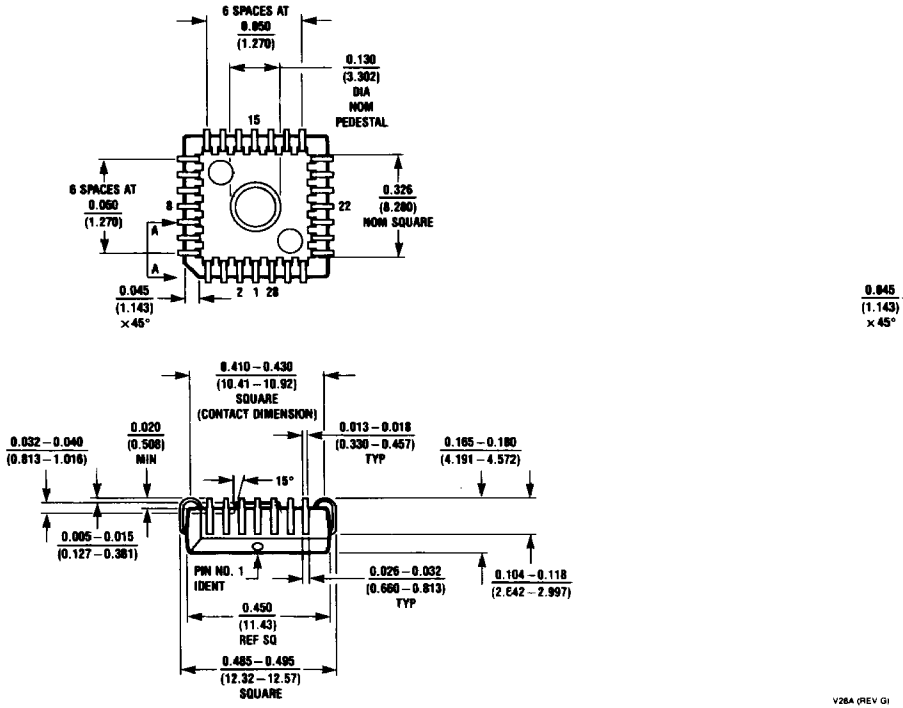
DP8531 System Debugging Flowchart (Continued)



TL/F/10371–30

Physical Dimensions inches (millimeters)



V28A (REV G)

Order Number DP8531V or DP8532V
NS Package Number V28A

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PRELIMINARY
May 1990

PC16551C Universal Asynchronous Receiver/Transmitter with FIFOs, Parallel Interface and Decode Logic†

PC16551C Universal Asynchronous Receiver/Transmitter with FIFOs, Parallel Interface and Decode Logic

General Description

The PC16551C integrates a CMOS version of the 16550 UART with a bidirectional parallel interface and an on-chip address decoder into a single IC. The UART is compatible with all existing software written for the 8250A, 16450, and 16550. The parallel port is compatible with all existing software written for the IBM® PC®, XT®, AT®, PS/2® and Centronics parallel ports. Chip selection can be done through an on-chip decoder to reduce the external hardware required when interfacing the PC16551C with an IBM AT or compatible I/O map. The improved AC timings ensure compatibility with state-of-the-art CPUs.

The UART can operate with on-chip transmitter and receiver FIFOs (FIFO mode) to relieve the CPU of excessive software overhead. In FIFO mode each channel is capable of buffering 16 bytes (plus 3 bits of error data per byte in the RCVR FIFO) of data in both the transmitter and receiver. All the FIFO control logic is on-chip to minimize system overhead and maximize system efficiency.

Signalling for DMA transfers is done through two pins per channel ($\overline{TXRDY}$ and $\overline{RXRDY}$). The $\overline{RXRDY}$ function is multiplexed on one pin with the $\overline{OUT\ 2}$ and BAUDOUT functions. The CPU can select these functions through a new UART register (Alternate Function Register).

The UART includes one programmable baud rate generator capable of dividing the clock input by divisors of 1 to ($2^{16} - 1$), and producing a 16 × clock for driving the internal logic of both the receiver and transmitter sections. The UART has complete MODEM-control capability, and a processor-interrupt system.

The parallel port has three registers, two of which provide status and control for the data register. The CPU can transfer data through this register in both directions by control of the $\overline{POS}$ Mode Pin, a bit in the Control register and the $\overline{RD}$ $\overline{WR}$ signals. All of the signals required by PC and Centronics printers to transfer data and monitor printer status are provided. On-Chip buffers meet or exceed drive current requirements of the PS/2 systems.

The on-chip decode logic can be used as an alternate to the chip select and channel select pins. When the PC16551C is mapped to the same addresses as COM1, COM2, LPT1, LPT2 and LPT3 on the AT bus, the decode logic will sense these addresses and enable the appropriate serial or parallel port.

The PC16551C is fabricated using National Semiconductor's advanced M²CMOS™.

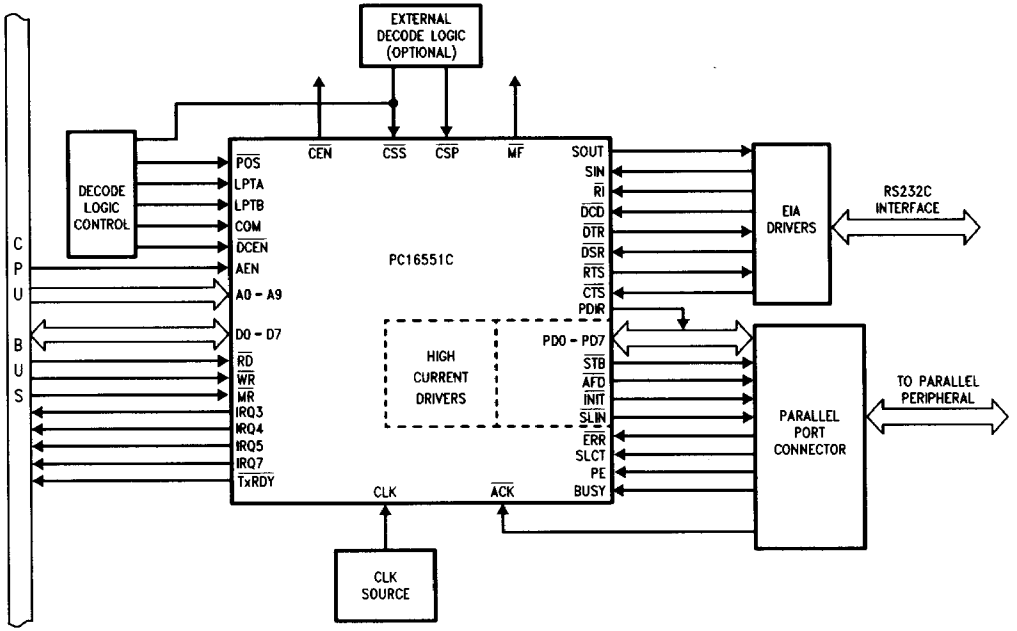
Features

- UART capable of interfacing with existing 8250A, 16450, and 16550 software
- Capable of interfacing with all PC, PS/2 and Centronics parallel port software
- High current drivers that meet or exceed all Micro Channel and PS/2 parallel port drive current requirements
- Provides all control and status pins for a complete PC, AT, PS/2, Micro Channel, and Centronics parallel port interface
- Monitors all signals necessary to decode standard COM1, COM2, LPT1, LPT2 and LPT3 addresses on the PC AT bus
- Read and Write cycle times of 84 ns
- After reset, all UART registers are identical to the 16450 register set
- In the FIFO mode transmitter and receiver are each buffered with 16-byte FIFOs to reduce the number of interrupts presented to the CPU
- Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from the serial data
- Independently controlled transmit, receive, line status, and data set interrupts
- Programmable baud generator divide any input clock by 1 to ($2^{16} - 1$) and generate the 16 × clock
- MODEM control functions (CTS, RTS, DSR, DTR, RI, and DCD)
- Fully programmable serial-interface characteristics:
  - 5-, 6-, 7-, or 8-bit characters
  - Even, odd, or no-parity bit generation and detection
  - 1-, 1½-, or 2-stop bit generation
  - Baud generation (DC to 1.5M baud) with 16 × clock
- False start bit detection
- Line break generation and detection
- Loopback controls for communications link fault isolation
- Break, parity, overrun, framing error simulation
- Full prioritized interrupt system controls

†**Note: This part is patented.**

Table of Contents

Basic Configuration



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