

CSD18533Q5A 60 V N-Channel NexFET™ Power MOSFET

1 Features

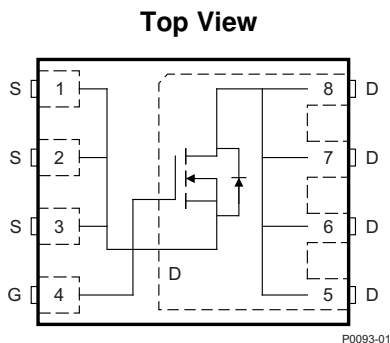
- Ultra Low Qg and Qgd
- Low Thermal Resistance
- Avalanche Rated
- Logic Level
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5 mm × 6 mm Plastic Package

2 Applications

- DC-DC Conversion
- Secondary Side Synchronous Rectifier
- Motor Control

3 Description

This 4.7 mΩ, 60 V, SON 5 × 6 mm NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



Product Summary

T _A = 25°C		TYPICAL VALUE		UNIT
V _{DS}	Drain-to-Source Voltage	60		V
Q _g	Gate Charge Total (10 V)	29		nC
Q _{gd}	Gate Charge Gate-to-Drain	5.4		nC
R _{DS(on)}	Drain-to-Source On-Resistance	V _{GS} = 4.5 V	6.5	mΩ
		V _{GS} = 10 V	4.7	mΩ
V _{GS(th)}	Threshold Voltage	1.9		V

Ordering Information⁽¹⁾

Device	Qty	Media	Package	Ship
CSD18533Q5A	2500	13-Inch Reel	SON 5 mm × 6 mm Plastic Package	Tape and Reel
CSD18533Q5AT	250	7-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

T _A = 25°C		VALUE	UNIT
V _{DS}	Drain-to-Source Voltage	60	V
V _{GS}	Gate-to-Source Voltage	±20	V
I _D	Continuous Drain Current (Package limited), T _C = 25°C	100	A
	Continuous Drain Current (Silicon limited), T _C = 25°C	103	
	Continuous Drain Current, T _A = 25°C ⁽¹⁾	17	
I _{DM}	Pulsed Drain Current, T _A = 25°C ⁽²⁾	267	A
P _D	Power Dissipation ⁽¹⁾	3.2	W
	Power Dissipation, T _C = 25°C	116	
T _J , T _{stg}	Operating Junction and Storage Temperature Range	-55 to 150	°C
E _{AS}	Avalanche Energy, single pulse I _D = 53 A, L = 0.1 mH, R _G = 25 Ω	140	mJ

(1) Typical R_{θJA} = 40°C/W on a 1 inch², 2 oz. Cu pad on a 0.06 inch thick FR4 PCB.

(2) Max R_{θJC} = 1.3°C/W, pulse duration ≤ 100 μs, duty cycle ≤ 1%

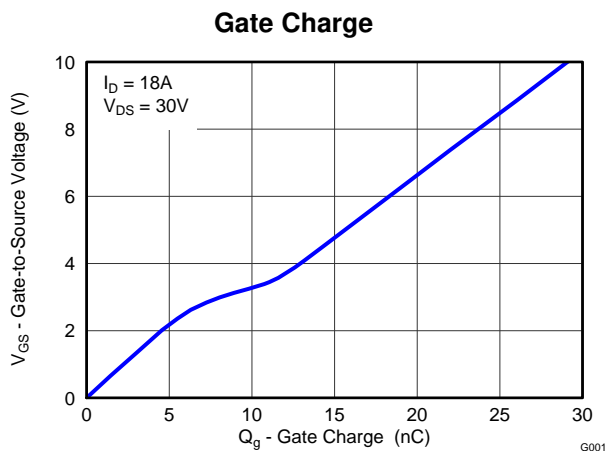
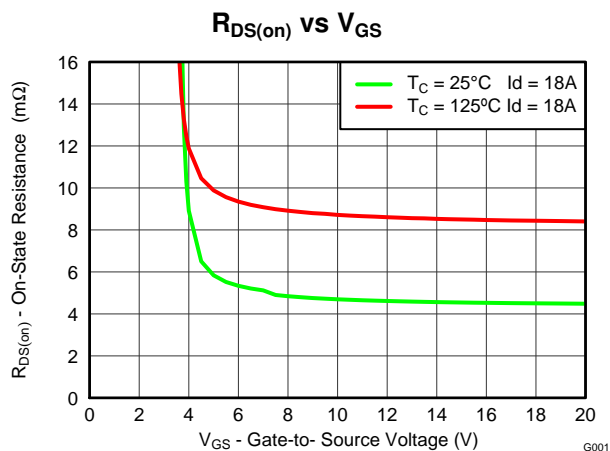


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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2013) to Revision B

Page

• Added part number to title	1
• Increased Pulsed Drain Current to 267 A	1
• Added line for max power dissipation with case temperature held to 25° C	1
• Updated pulsed current conditions	1
• Changed Figure 1 to normalized $R_{\theta JC}$ curve	4
• Updated SOA in Figure 10	6

Changes from Original (September 2012) to Revision A

Page

• Changed the $R_{\theta JC}$ MAX value From: 2.3°C/W to 1.3°C/W	3
• Changed From: Max $R_{\theta JA}$ = 121°C/W To: Max $R_{\theta JA}$ = 125°C/W	4
• Changed Typ $R_{th JA}$ = 99°C/W To: $R_{th JA}$ = 100°C/W in Figure 1	4
• Added the Recommended Stencil Opening section	9

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
V _{DSS}	Drain-to-Source Voltage	V _{GS} = 0 V, I _D = 250 μA	60			V
I _{DSS}	Drain-to-Source Leakage Current	V _{GS} = 0 V, V _{DS} = 48 V			1	μA
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0 V, V _{GS} = 20 V			100	nA
V _{GS(th)}	Gate-to-Source Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	1.5	1.9	2.3	V
R _{DS(on)}	Drain-to-Source On-Resistance	V _{GS} = 4.5 V, I _D = 18 A		6.5	8.5	mΩ
		V _{GS} = 10 V, I _D = 18 A		4.7	5.9	mΩ
g _{fs}	Transconductance	V _{DS} = 30 V, I _D = 18 A		122		S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input Capacitance	V _{GS} = 0 V, V _{DS} = 30 V, f = 1 MHz		2200	2750	pF
C _{oss}	Output Capacitance			292	365	pF
C _{rss}	Reverse Transfer Capacitance			7	9	pF
R _G	Series Gate Resistance			1.3	2.6	Ω
Q _g	Gate Charge Total (4.5 V)	V _{DS} = 30 V, I _D = 18 A		14	18	nC
Q _g	Gate Charge Total (10 V)			29	36	
Q _{gd}	Gate Charge Gate-to-Drain			5.4		nC
Q _{gs}	Gate Charge Gate-to-Source			6.6		nC
Q _{g(th)}	Gate Charge at V _{th}			4.7		nC
Q _{oss}	Output Charge		V _{DS} = 30 V, V _{GS} = 0 V		31	
t _{d(on)}	Turn On Delay Time	V _{DS} = 30 V, V _{GS} = 10 V, I _{DS} = 18 A, R _G = 0 Ω		5.2		ns
t _r	Rise Time			5.5		ns
t _{d(off)}	Turn Off Delay Time			15		ns
t _f	Fall Time			2.0		ns
DIODE CHARACTERISTICS						
V _{SD}	Diode Forward Voltage	I _{SD} = 18 A, V _{GS} = 0 V		0.8	1	V
Q _{rr}	Reverse Recovery Charge	V _{DS} = 30 V, I _F = 18 A, di/dt = 300 A/μs		68		nC
t _{rr}	Reverse Recovery Time			40		ns

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

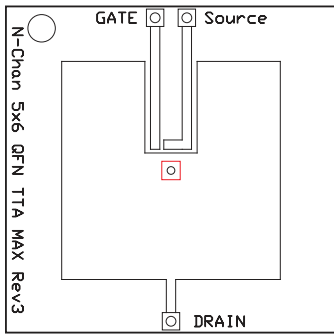
THERMAL METRIC		MIN	TYP	MAX	UNIT
R _{θJC}	Thermal Resistance Junction to Case ⁽¹⁾			1.3	°C/W
R _{θJA}	Thermal Resistance Junction to Ambient ⁽¹⁾⁽²⁾			50	

- (1) R_{θJC} is determined with the device mounted on a 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu pad on a 1.5 inch × 1.5 inch (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 PCB. R_{θJC} is specified by design, whereas R_{θJA} is determined by the user's board design.
- (2) Device mounted on FR4 material with 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu.

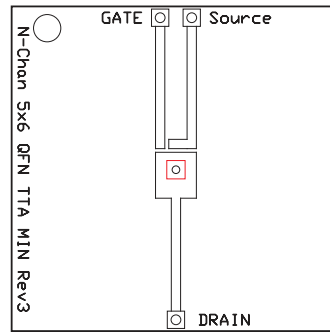
CSD18533Q5A

SLPS388B – SEPTEMBER 2012 – REVISED JANUARY 2015

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Max $R_{\theta JA} = 50^{\circ}\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of
2 oz. (0.071 mm thick)
Cu.



Max $R_{\theta JA} = 125^{\circ}\text{C/W}$
when mounted on a
minimum pad area of
2 oz. (0.071 mm thick)
Cu.

5.3 Typical MOSFET Characteristics

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)

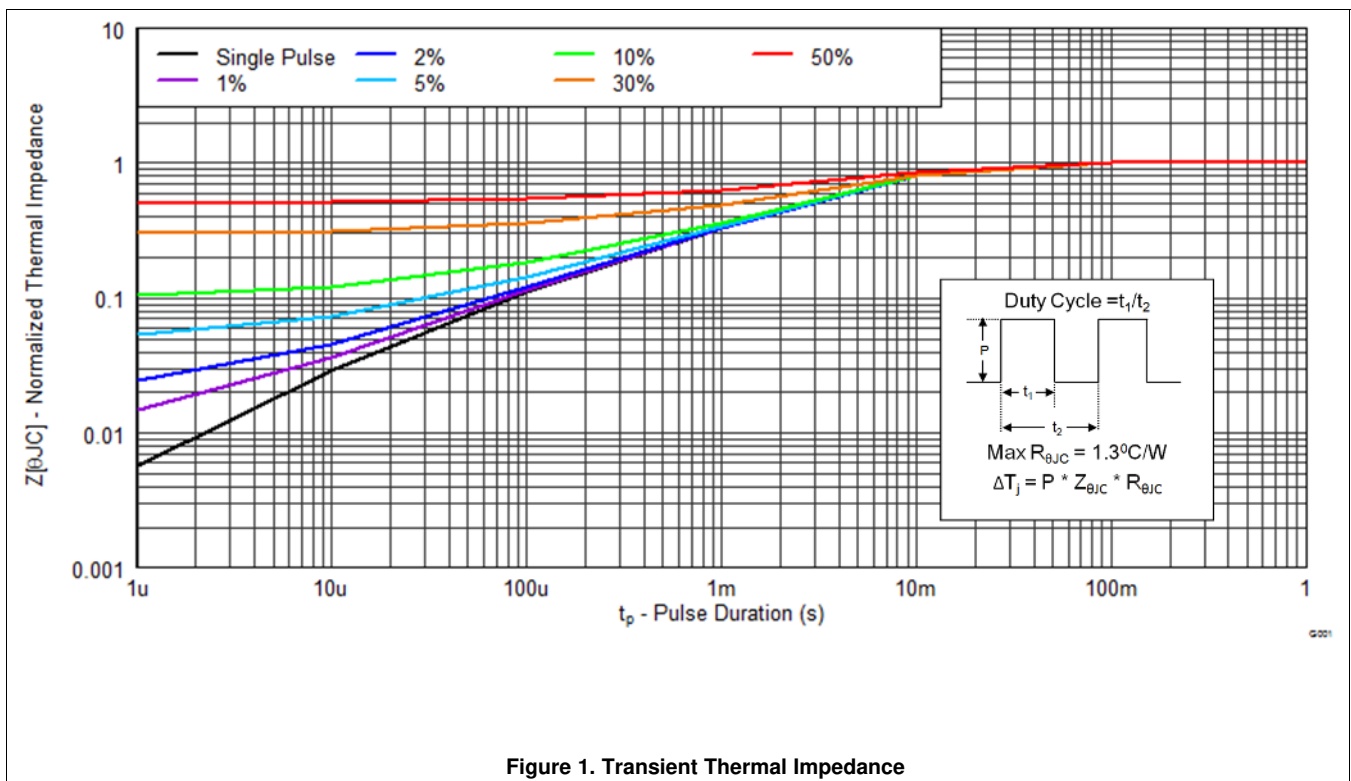


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

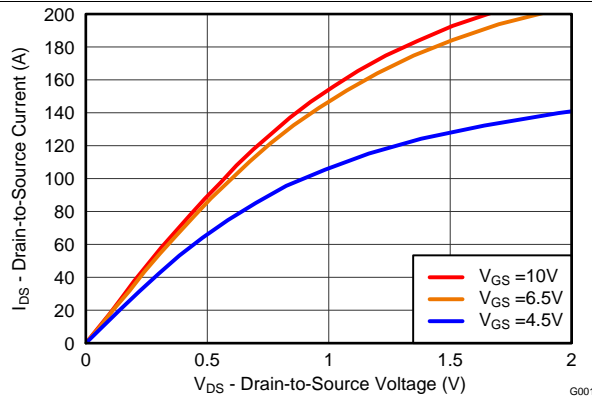


Figure 2. Saturation Characteristics

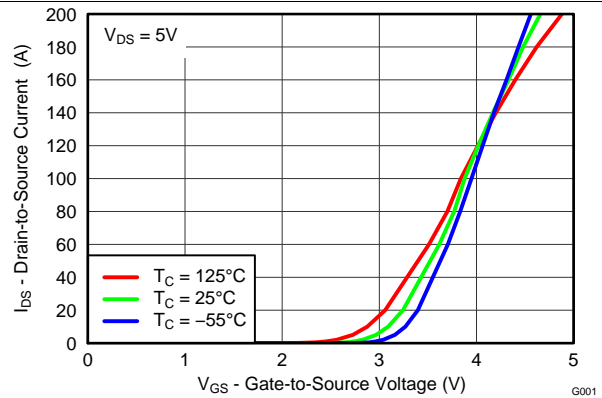


Figure 3. Transfer Characteristics

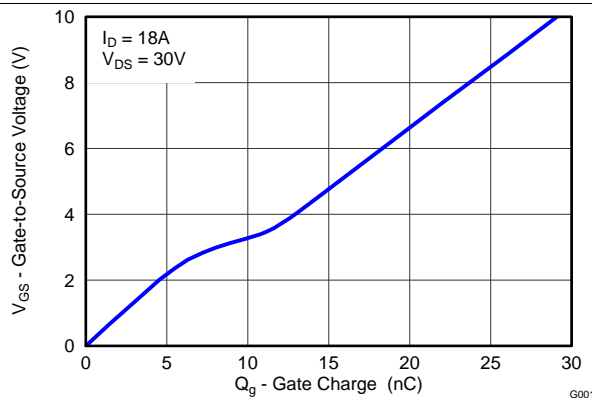


Figure 4. Gate Charge

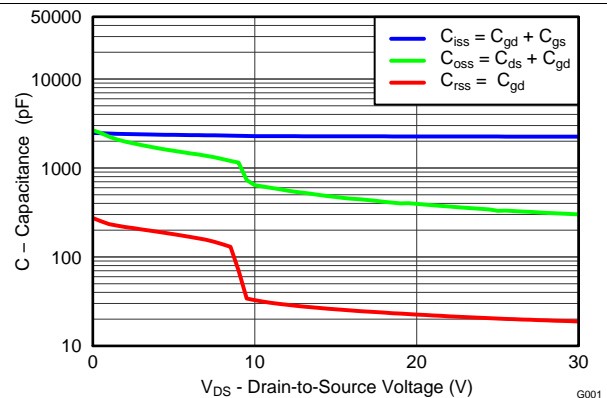


Figure 5. Capacitance

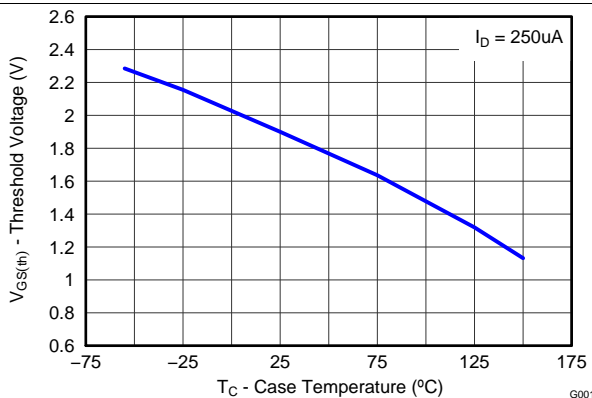


Figure 6. Threshold Voltage vs Temperature

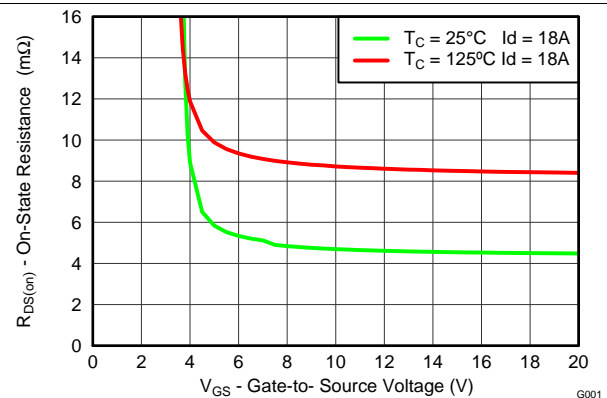


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

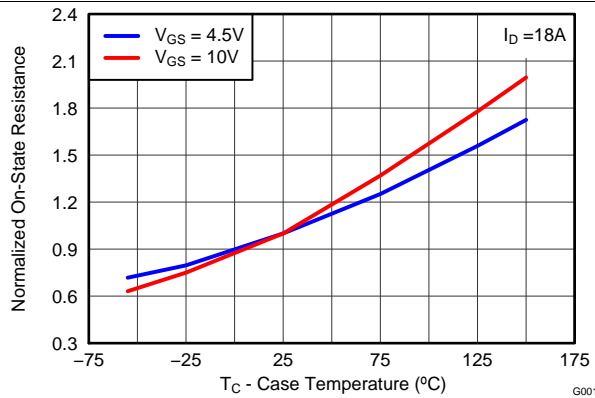


Figure 8. Normalized On-State Resistance vs Temperature

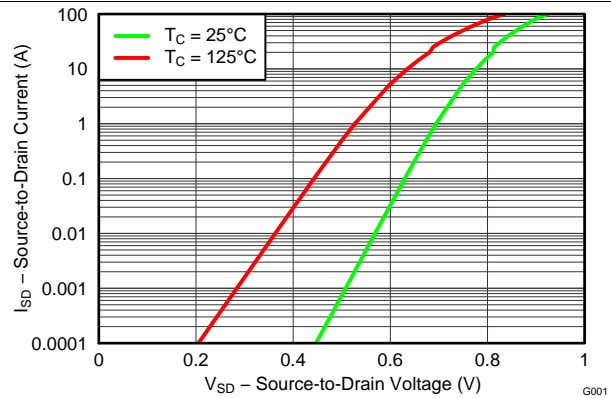


Figure 9. Typical Diode Forward Voltage

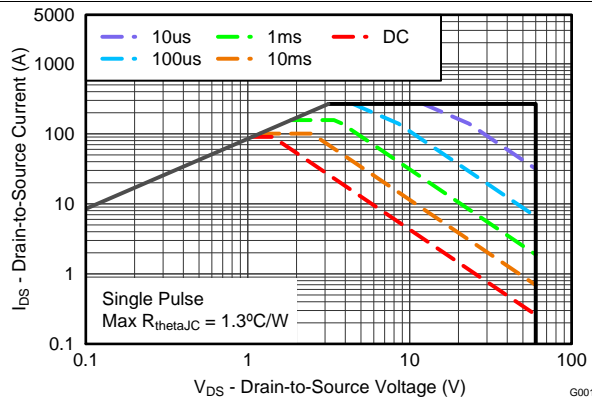


Figure 10. Maximum Safe Operating Area

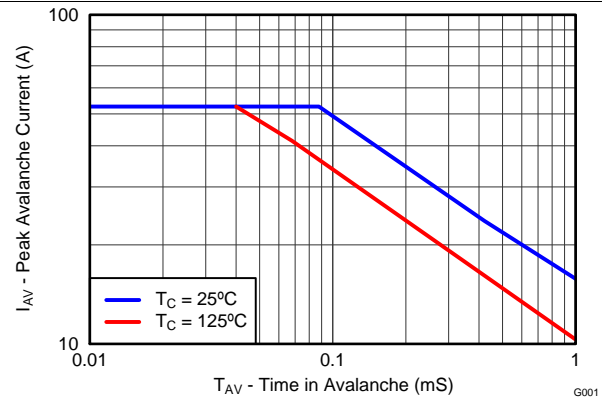


Figure 11. Single Pulse Unclamped Inductive Switching

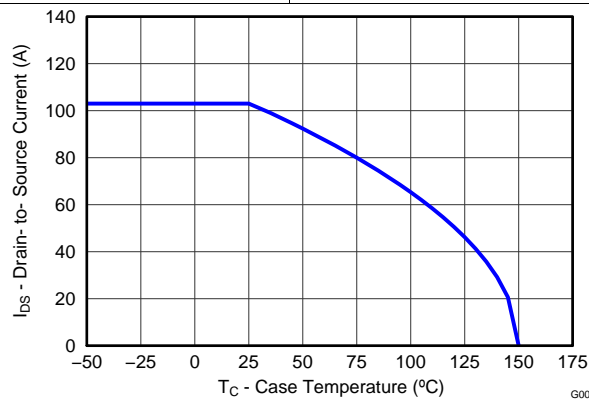


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Trademarks

NexFET is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

6.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

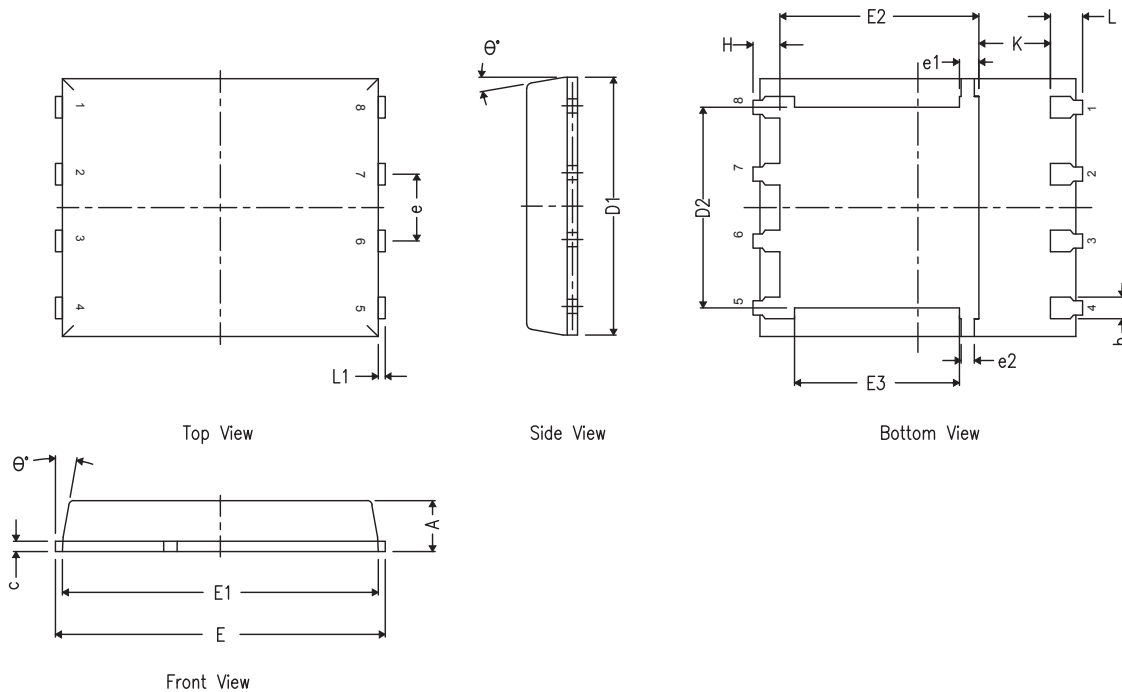
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

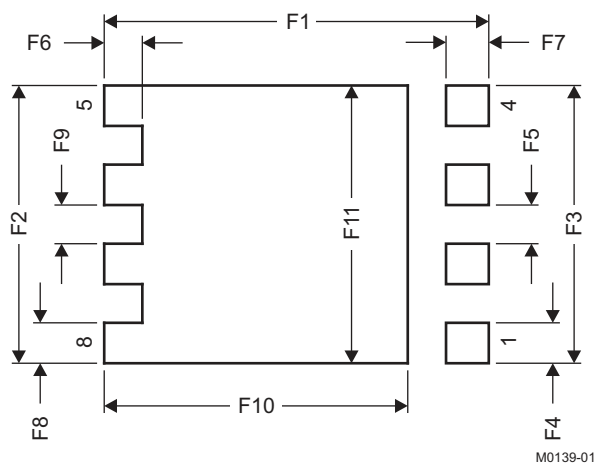
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Q5A Package Dimensions



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.34
D1	4.80	4.90	5.00
D2	3.61	3.81	4.02
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
E3	3.03	3.13	3.23
e	1.17	1.27	1.37
e1	0.27	0.37	0.47
e2	0.15	0.25	0.35
H	0.41	0.56	0.71
K	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
θ	0°		12°

7.2 Recommended PCB Pattern

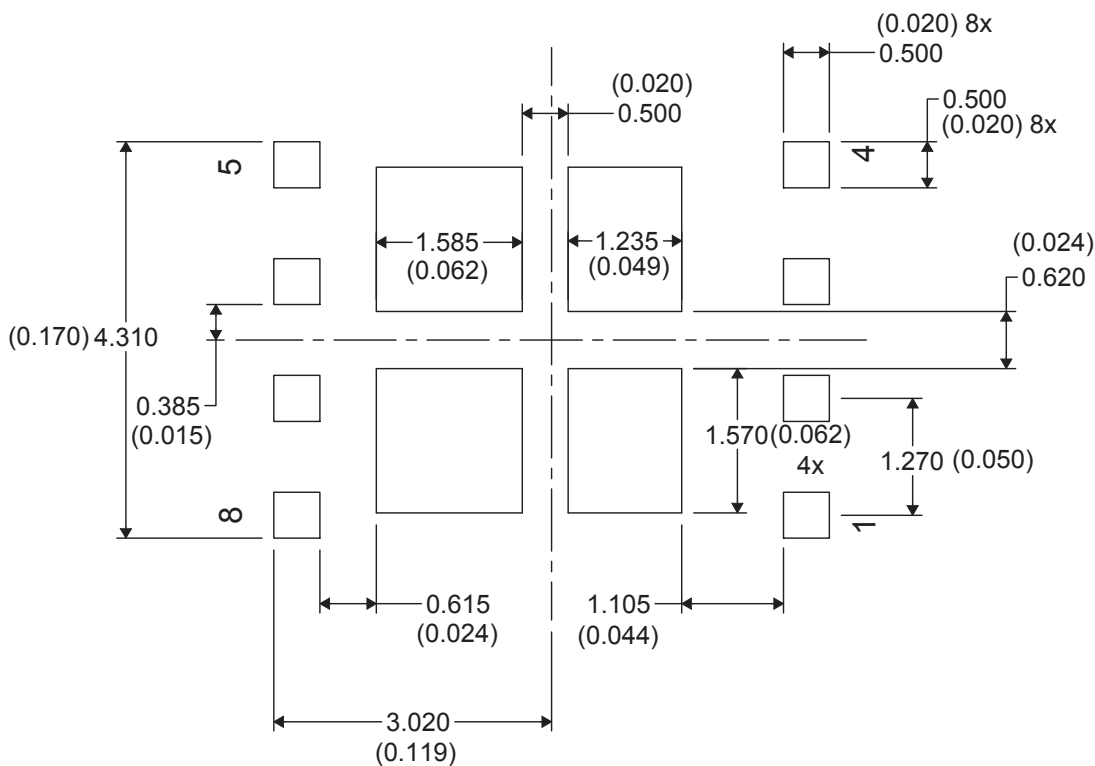


Recommended PCB Pattern (continued)

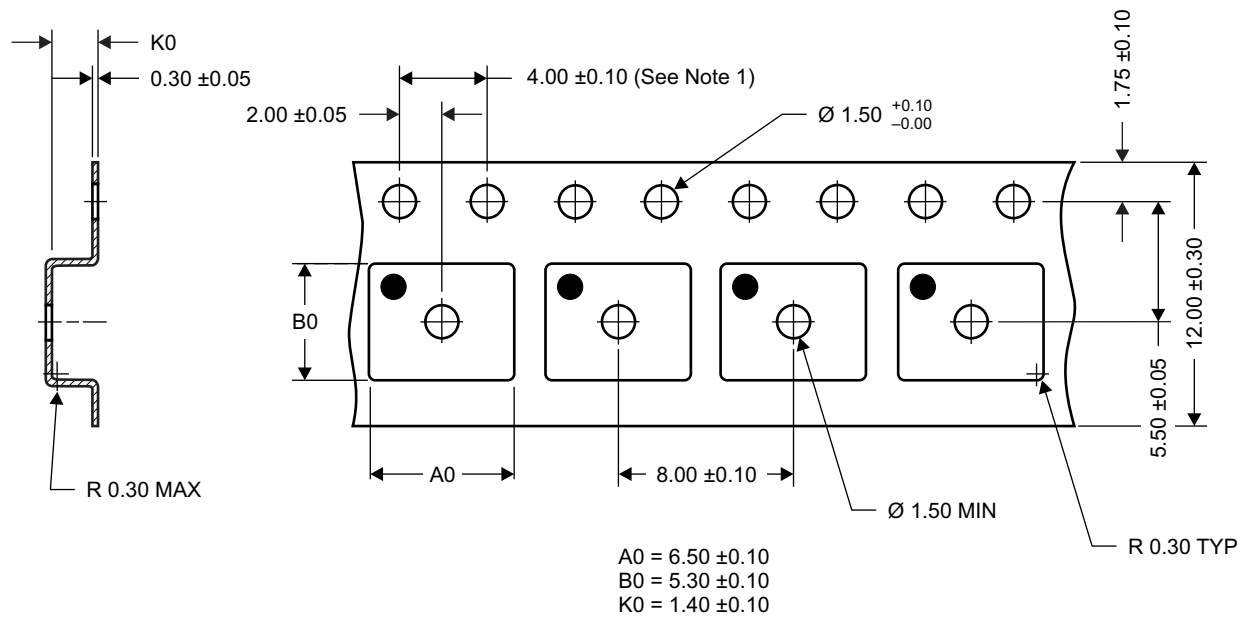
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

For recommended circuit layout for PCB designs, see application note [SLPA005 – Reducing Ringing Through PCB Layout Techniques](#).

7.3 Recommended Stencil Opening



7.4 Q5A Tape and Reel Information





M0138-01

Notes:

1. 10-sprocket hole-pitch cumulative tolerance ± 0.2
2. Camber not to exceed 1mm in 100mm, noncumulative over 250mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified)
5. A0 and B0 measured on a plane 0.3mm above the bottom of the pocket

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD18533Q5A	ACTIVE	VSONP	DQJ	8	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD18533	
CSD18533Q5AT	ACTIVE	VSONP	DQJ	8	250	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD18533	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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