CD74LPT16827

December 1996

Fast CMOS 3.3V 20-Bit Buffer

Features

- Advanced 0.6 micron CMOS Technology
- Compatible with LCX™ Family
- Supports 5V Tolerant Mixed Signal Mode Operation
  - Input Can Be 3V or 5V
  - Output Can Be 3V or Connected to 5V Bus
- Advanced Low Power CMOS Operation
- Excellent Output Drive Capability:
  - Balanced Drives (24mA Sink and Source)
- Pin Compatible with Industry Standard Double-Density Pinouts
- Low Ground Bounce Outputs
- Hysteresis on All Inputs
- Multiple Center Pin and Distributed V_{CC}/GND Pins Minimizing Switching Noise

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74LPT16827AMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74LPT16827ASM	-40 to 85	56 Ld SSOP	M56.300-P
CD74LPT16827BMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74LPT16827BSM	-40 to 85	56 Ld SSOP	M56.300-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

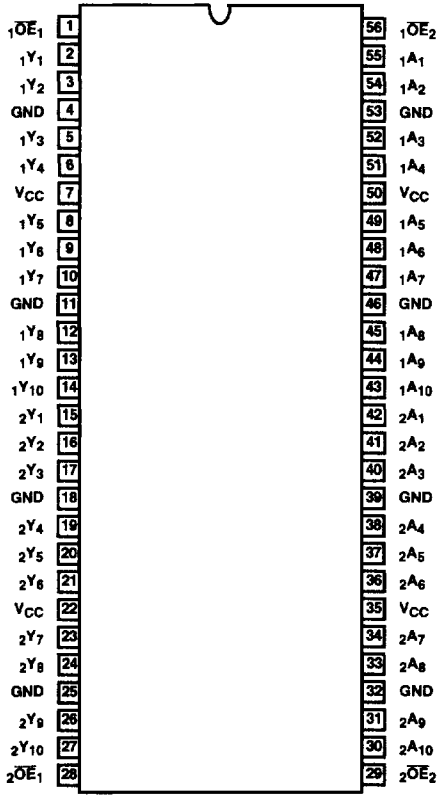
Description

The CD74LPT16827 is a 20-bit wide bus driver designed to provide buffering and high-performance bus interfacing for wide data/address paths or busses with parity. Two pair of nanded output enable controls allow the device to be operated as two 10-bit buffers or as one 20-bit buffer. Signal pins are arranged in a flow-through organization for ease of layout and hysteresis is designed into all inputs to improve noise margin.

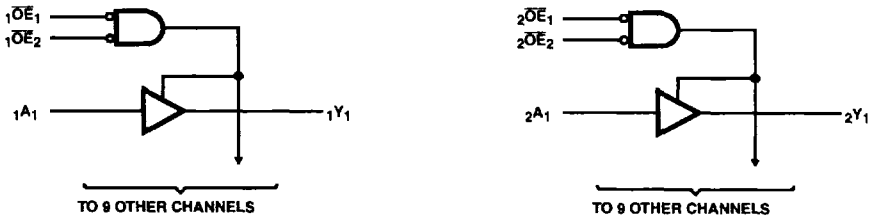
The CD74LPT16827 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Pinout

CD74LPT16827 (SSOP, TSSOP)
TOP VIEW



Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS			OUTPUT
$_x\overline{OE}_1$	$_x\overline{OE}_2$	$_xA_x$	$_xY_x$
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z= High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$_x\overline{OE}_x$	Output Enable Inputs (Active LOW)
$_xA_x$	Data Inputs
$_xY_x$	Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
TSSOP Package	85
SSOP Package	70

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 2.7V to 3.6V							
Input HIGH Voltage (Input Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.2	-	5.5	V
Input HIGH Voltage (I/O Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	5.5	V
Input LOW Voltage (Input and I/O Pins)	V_{IL}	Guaranteed Logic LOW Level		-0.5	-	0.8	V
Input HIGH Current (Input Pins)	I_{IH}	V_{CC} = Max	V_{IN} = 5.5V	-	-	±1	µA
Input HIGH Current (I/O Pins)	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	±1	µA
Input LOW Current (Input Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
Input LOW Current (I/O Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
High Impedance Output Current (Three-State Output Pins)	I_{OZH}	V_{CC} = Max	V_{OUT} = 5.5V	-	-	±1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = GND	-	-	±1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Output HIGH Current	I_{ODH}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 5)		-36	-60	-110	mA
Output LOW Current	I_{ODL}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 5)		50	90	200	mA
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -0.1mA	V_{CC} - 0.2	-	-	V
			I_{OH} = -3mA	2.4	3.0	-	V
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -8mA	2.4 (Note 7)	3.0	-	V
			I_{OH} = -24mA	2.0	-	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA	-	-	0.2	V
			I_{OL} = 16mA	-	0.2	0.4	V
			I_{OL} = 24mA	-	0.3	0.5	V

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Short Circuit Current (Note 6)	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-85	-240	mA
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq 4.5V$		-	-	±100	µA
Input Hysteresis	V_H			-	150	-	mV
CAPACITANCE $T_A = 25^oC$, f = 1MHz							
Input Capacitance (Note 8)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 8)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	V_{CC} = Max	$V_{IN} = V_{CC}$ - 0.6V (Note 9)	-	2.0	30	µA
Dynamic Power Supply Current (Note 10)	I_{CCD}	V_{CC} = Max, Outputs Open $x\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	50	75	µA/ MHz
Total Power Supply Current (Note 12)	I_C	V_{CC} = Max, Outputs Open f_i = 10MHz, 50% Duty Cycle $x\overline{OE}$ = GND One Bit Toggling	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	0.6	2.3	mA
		V_{CC} = Max, Outputs Open f_i = 2.5MHz, 50% Duty Cycle $x\overline{OE}$ = GND 16 Bits Toggling	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	2.1	4.7 (Note 11)	mA

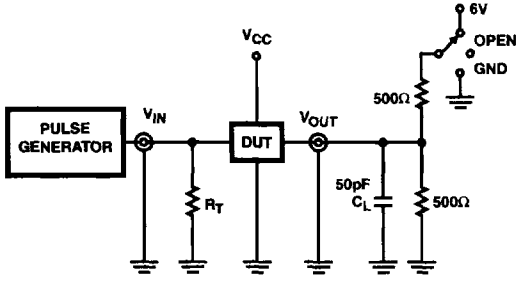
Switching Specifications Over Operating Range (Note 13)

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	CD74LPT16827A (NOTE 15) MIN	CD74LPT16827A MAX	CD74LPT16827B (NOTE 15) MIN	CD74LPT16827B MAX	UNITS
Propagation Delay A_N to Y_N	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	5.0	ns
		C_L = 300pF R_L = 500Ω (Note 16)	1.5	15.0	1.5	13.0	ns
Output Enable Time $\overline{OE}_N$ to Y_N	t_{PZH}, t_{PZL}	C_L = 50pF R_L = 500Ω	1.5	9.5	1.5	8.0	ns
		C_L = 300pF R_L = 500Ω (Note 16)	1.5	23.0	1.5	15.0	ns
Output Disable Time (Note 16) $\overline{OE}_N$ to Y_N	t_{PHZ}, t_{PLZ}	C_L = 5pF R_L = 500Ω	1.5	8.5	1.5	6.0	ns
		C_L = 50pF R_L = 500Ω	1.5	10.0	1.5	7.0	ns
Output Skew (Note 17)	$t_{SK(O)}$		-	0.5	-	0 5	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is guaranteed but not tested.
7. $V_{OH} = V_{CC}$ - 0.6V at rated current.
8. This parameter is determined by device characterization but is not production tested.
9. Per TTL driven input; all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current (I_{CCL},I_{CCH} and I_{CCZ})
    ΔI_{CC} = Power Supply Current for a TTL High Input
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    N_{CP} = Number of Clock Inputs at f_{CP}
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
13. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
14. See test circuit and wave forms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.
17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

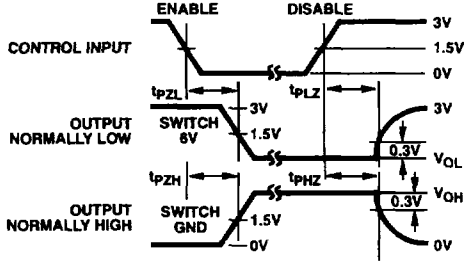


FIGURE 2. ENABLE AND DISABLE TIMING

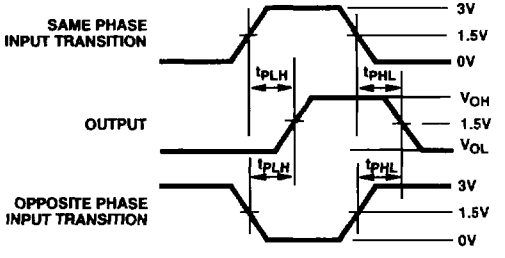


FIGURE 3. PROPAGATION DELAY