

# MM54HC51/MM74HC51 Dual AND-OR-Invert Gate

## MM54HC58/MM74HC58 Dual AND-OR Gate

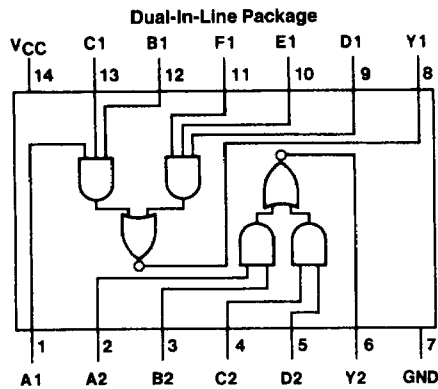
### General Description

These gates utilize advanced silicon-gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### Features

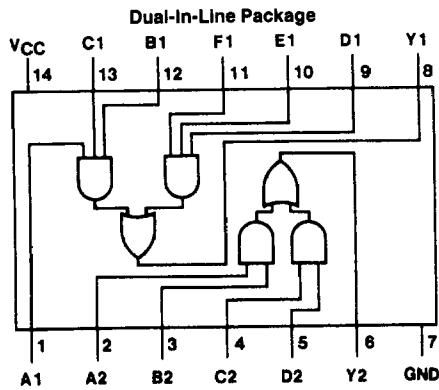
- Typical propagation delay: 10 ns
- Wide power supply range: 2–6V
- Low quiescent supply current: 20  $\mu$ A maximum (74 Series)
- Low input current: 1  $\mu$ A maximum
- High output current: 4 mA minimum

### Connection Diagrams



TL/F/5302-1

Order Number MM54HC51\* or MM74HC51\*



TL/F/5302-2

Order Number MM54HC58\* or MM74HC58\*

\*Please look into Section 8, Appendix D for availability of various package types.

**AC Electrical Characteristics**  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $C_L = 15\text{ pF}$ ,  $t_r = t_f = 6\text{ ns}$ 

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay		10	20	ns

**AC Electrical Characteristics**  $V_{CC} = 2.0V$  to  $6.0V$ ,  $C_L = 50\text{ pF}$ ,  $t_r = t_f = 6\text{ ns}$  (unless otherwise specified)

Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$		74HC	54HC	Units
						$T_A = -40$ to $85^\circ C$	$T_A = -55$ to $125^\circ C$	
				Typ	Guaranteed Limits			
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay		2.0V	63	125	158	186	ns
			4.5V	13	25	32	37	ns
			6.0V	11	21	27	32	ns
$t_{TLH}$ , $t_{THL}$	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
$C_{PD}$	Power Dissipation Capacitance (Note 5)	(per AND-OR-Gate)		20				pF
$C_{IN}$	Maximum Input Capacitance			5	10	10	10	pF

**Note 5:**  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .