User's Guide
SLAU467D–November 2012–Revised February 2017

ADS42JB46, ADS42JB49, and ADS42JB69 Evaluation Module

This document outlines the basic steps and functions that are required to ensure the proper operation of the Texas Instruments (TI) ADS42JB46, ADS42JB49, and ADS42JB69 Evaluation Modules (hereafter in this document, ADS42JBxxEVM or EVM). The EVM package includes an ADS42JBxxEVM, a 5-VDC power supply, and a mini-USB cable. This EVM is designed to be used with the TSW14J5xEVM (a JESD204B data capture card). The ADS42JBxx EVM can also be connected to all FPGA development platforms with an FMC connector for evaluation. The ADS42JBxxEVM includes either an ADS42JB49 (14-bit), or ADS42JB69 (16-bit) dual-channel, 250-MSPS, or an ADS42JB46 (14-bit) dual channel, 160-MSPS analog-to-digital converter. The EVM also includes a TI LMK04828 clock jitter cleaner to provide a low jitter/phase noise sampling clock to the ADC. This user's guide outlines the steps to quickly evaluate the performance of the ADS42JBxx ADC by capturing and displaying signal waveforms using the TSW14J5xEVM and the High Speed Data Converter Pro GUI software. The EVM schematics, BOMs, and layout files are found in the design package under the ADS42JBxxEVM product folder available on http://www.ti.com.

Contents

List of Figures

List of Tables

Trademarks

1 Introduction

1.1 Overview

The ADS42JBxxEVM is an evaluation module (EVM) used to evaluate Texas Instruments' ADS42JBxx ADC. The ADS42JB49 (14-bit) and ADS42JB69 (16-bit) are low-power, 250-MSPS analog-to-digital converter (ADC) with a buffered analog input and outputs featuring a JESD204B interface. The ADS42JB46 (14-bit) is a low power 160-MSPS ADC version of the same family of ADC's. The EVM has transformer-coupled analog inputs accommodating a wide range of signal sources and frequencies. The onboard LMK04828 provides an ultra-low jitter and phase-noise ADC sample clock along with system reference clocks (SYSREF) for the ADC and the mating FPGA capture board (TSW14J5xEVM), for a complete JESD204B subclass 1 clocking solution.

The ADS42JBxx and LMK04828 are controlled through an easy-to-use software GUI enabling quick configuration for a variety of modes.

The TSW14J5xEVM is an FPGA-based data capture platform that mates with the ADS42JBxxEVM across an FMC connector. Sampled data from the ADS42JBxx EVM is captured by the FPGA and stored in external DDR3 memory. The HSDC Pro software interface is available for reading and displaying the stored ADC samples in both frequency and time domains.

1.2 Block Diagram

The block diagram for the ADS42JB69EVM is shown in Figure 1. The various inputs, outputs, and jumper configurations of the ADS42JBxxEVM are described in Table 1.

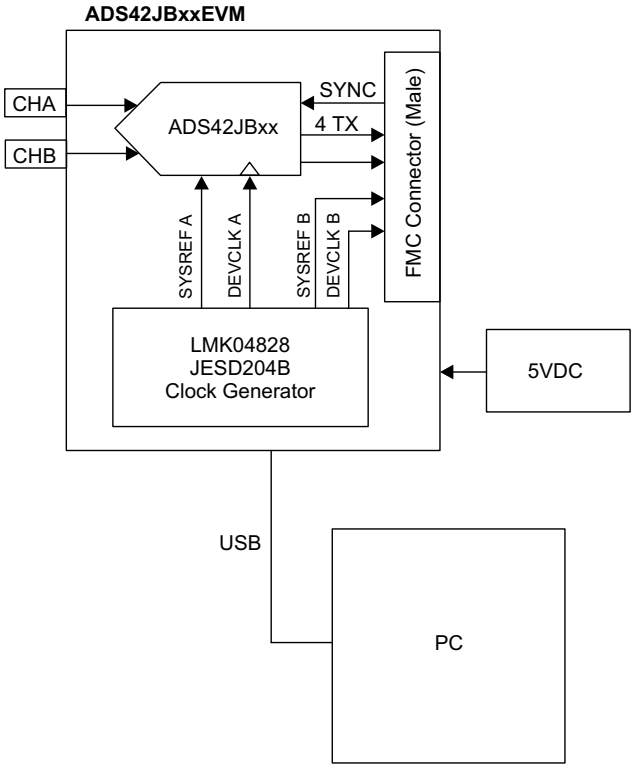

Figure 1. Block Diagram of the ADS42JBxxEVM

Table 1. Input and Output Connectors and Jumper Descriptions of the ADS42JBxxEVM

Component	Description
J1 (AINP)	Single-ended analog input for channel A
J2 (BINP)	Single-ended analog input for channel B
J19 (EXT_ADC_CLK)	Single-ended ADC clock input
J8 (+5V)	Positive power connection (5 V)
J9 (GND)	Negative power connection (GND)
J13 (Main PWR)	5-V input for provided power cable
J14 (REF OSC_IN)	External reference option for LMK04828, REFOUT1 source on J16 and CPLD_CLK
J16 (REFOUT1)	10-MHz CMOS level reference output or frequency of REF OSC_IN if option selected
J6 (USB)	USB connection
J3	JESD204B FMC interface connector
J5 (LMK SYNC)	LMK04828 sync input
J7 (LMK CLKIN1_P)	CLKIN0 input for LMK04828. Option to provide an external clock source to the LMK in place of on-board 100-MHz VCXO.
J10 (CLKOUT10P)	DCLKOUT6p from LMK04828. Default is LVPECL at 250 MHz.
J15 (CLKOUT10N)	DCLKOUT6n from LMK04828. Default is LVPECL at 250 MHz.
J17 (CLKOUT12P)	SDCLKOUT7p from LMK04828. Default is LVPECL at 6.25 MHz.
J4 (CLKOUT12M)	SDCLKOUT7p from LMK04828. Default is LVPECL at 6.25 MHz.
J18 (PROG CPLD)	JTAG interface for CPLD U3
SW1 (ADC_RESET)	Switch to reset the ADC using the RESET input pin
SW3 (CPLD)	Switch inputs to CPLD. Currently not used.
SW2 (Reset CPLD)	CPLD reset
SJP12	ADC CNTRL1 pin. Not used by ADC. Connected to GND.
JP3	ADC CNTRL2 pin. Not used by ADC. Connected to GND.
JP6 (XO_PWR)	Provides power to VCXO Y2 or oscillator Y3
SJP3 (REF_SEL)	Selects input or external reference source for LMK, J16 and CPLD. Default is internal 10-MHz source.
JP2 (CDC_CLK)	Reference clock buffer output enable
JP5 (REF_PWR)	Power enable for 10-MHz reference oscillator
SJP1 (REF_EN)	Enable for 10-MHz reference oscillator
SJP4-SJP11	USB/FMC Interface select. Default is using USB.
SJP2 (WP)	EEPROM write protect.
JP4 (ENABLE)	U11 enable. Install jumper to disable switcher U11. Default is uninstalled.
JP1 (PWRGD)	Test point for power good output pin from U11.

2 Software Control

This section provides installation instructions for the ADS42JBxx GUI and descriptions of the various controls. Please note, any illustration and textual references to ADS42JB69 or ADS42JBx9 in this section apply to the ADS42JB46 as well.

2.1 Installation Instructions for ADS42JBxxEVM GUI

1. Download the software installation package (SLAC544) from the ADS42JBxxEVM product page.
2. Extract the files from the zip file named *ADS42JBx9 GUI vXpY installer.zip* where *XpY* represents the version number.
3. Run *setup.exe* and follow the installation prompts to install the software.
4. After successfully installing the software, start the GUI by going to **Start Menu → All Programs → Texas Instruments ADCs → ADS42JBxx GUI**

2.2 Quick Start

Figure 2 illustrates the EVM hardware setup.

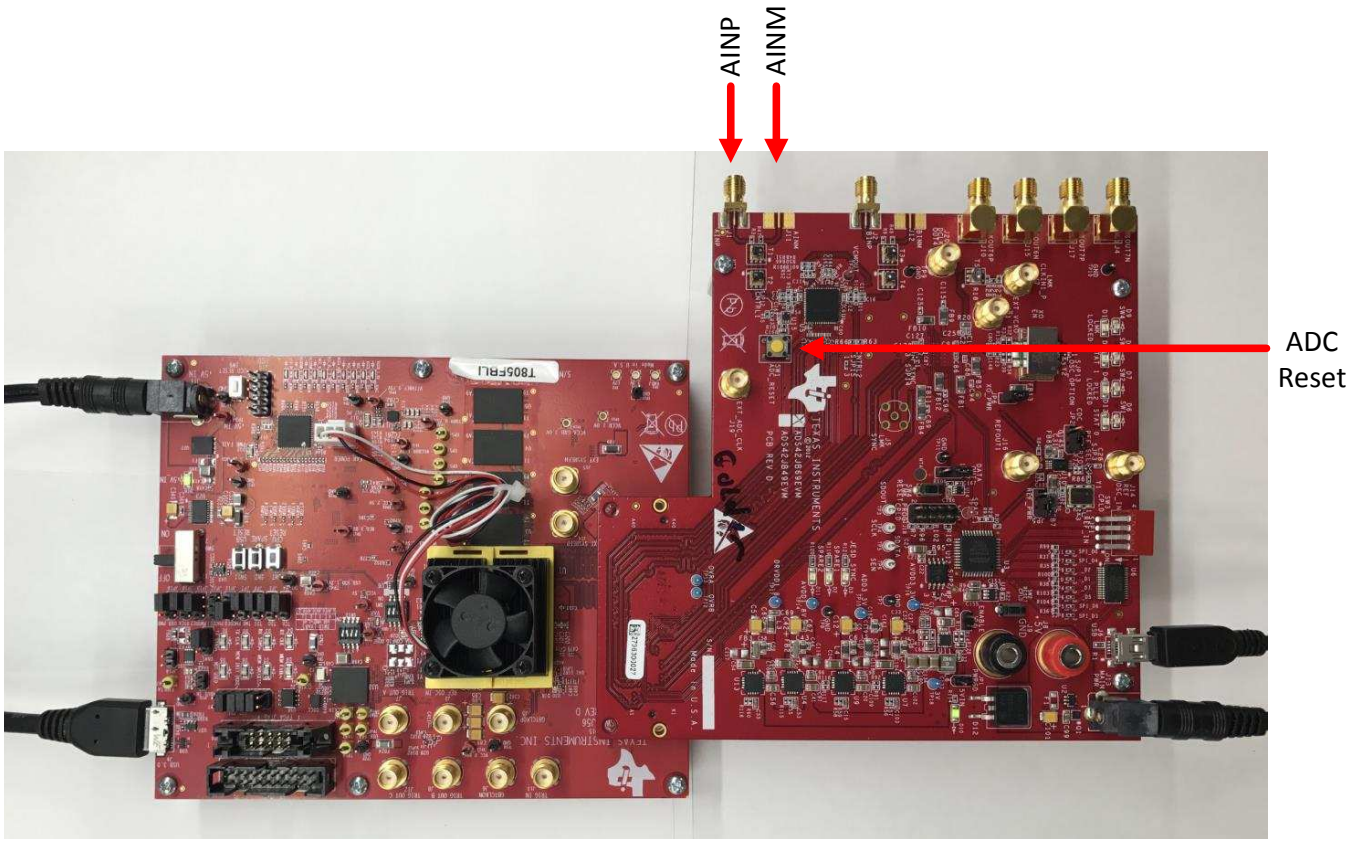

Figure 2. EVM Hardware Setup

Use the following steps to set up the ADS42JBxxEVM and TSW14J5xEVM for evaluation:

1. Connect the ADS42JBxx EVM to the TSW14J5x via the FMC connector.
2. Plug one end of the provided 5-V power cables into both EVMs and connect the other ends to a +5V DC power supply capable of providing 4 amps.
3. Plug a mini-USB into both EVMs. Plug the other end of USB to the PC or laptop running the ADS42JBxx software and HSDC Pro software.
   Note: When plugging the ADS42JBxxEVM board into the computer through the USB cable for the first time, you are prompted to install the USB drivers.
   - Microsoft® Windows® XP: If Windows XP does not automatically install the drivers, follow the prompts on the screen to do so. Do not let Windows XP search Microsoft Update for the drivers, but do let Windows XP install the drivers automatically.
   - Windows 7: After installing the GUI, Windows 7 should automatically be able to install the drivers for the ADS42JBxxEVM with no user input.
4. Move SW6 on the TSW14J56 (or SW3 on the TSW14J57) to the 'ON' position to power up the board.
5. **IMPORTANT:** Push the hardware reset (SW1) on the ADS42JBxx EVM board. This is required each time the EVM is powered up to ensure proper operation.

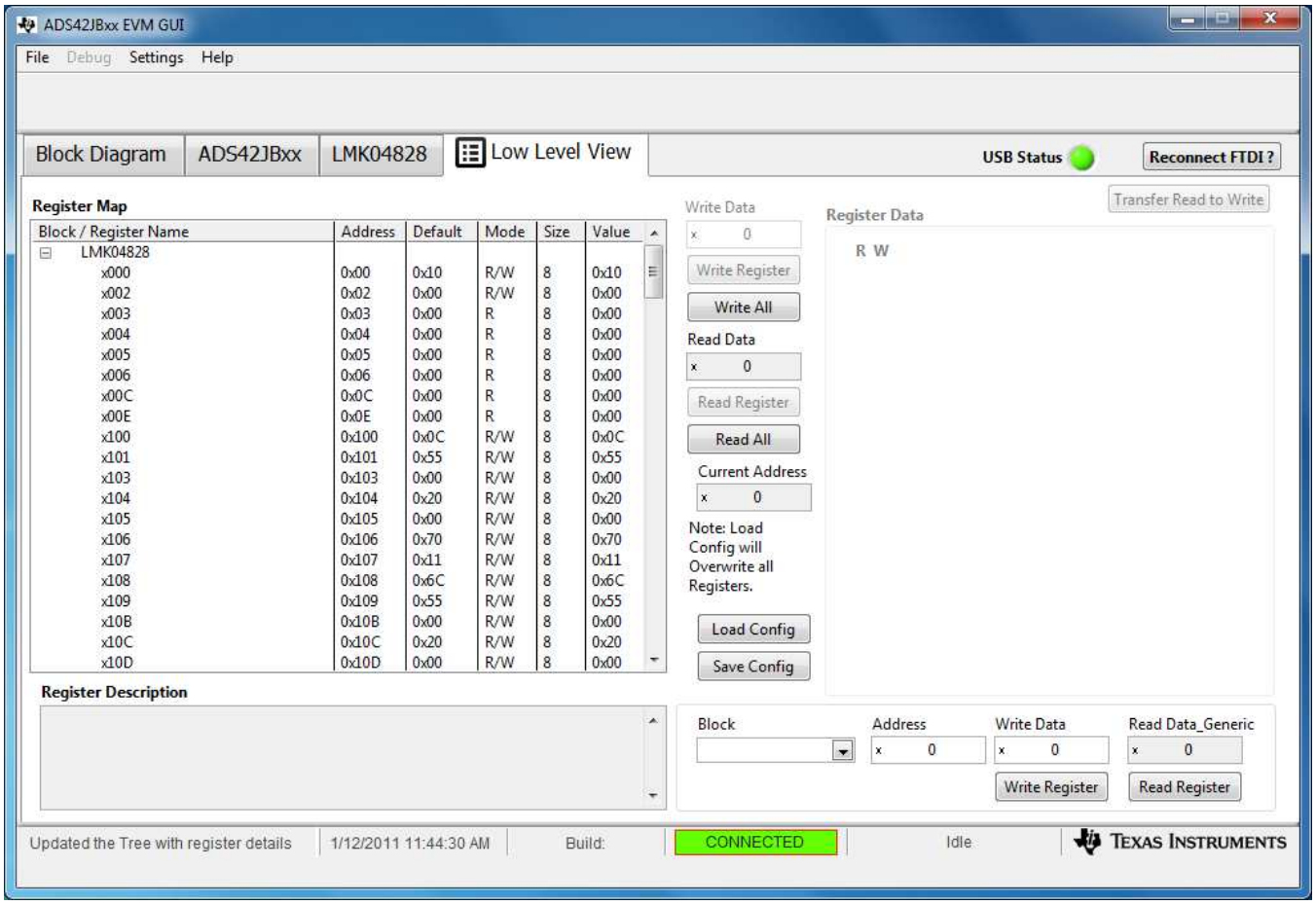

Figure 3. ADS42JBxx EVM GUI Setup

6. Start the ADS42JBxxEVM software (Figure 3).
   - On Windows platforms, start the ADS42JBxx EVM GUI software from Start → All Programs → Texas Instruments ADCs → ADS42JBxx.
7. Go to "Low Level View" and click the "Load Config" button. *ADS42JB69_EVM_LMF421_250M.cfg*. This configuration file should be located in the GUI software installation directory.
   - The configuration file sets the ADC up for Fsampling = 250 MHz, lane rate = 2.5 GHz, L = 4, M = 2, F = 1.

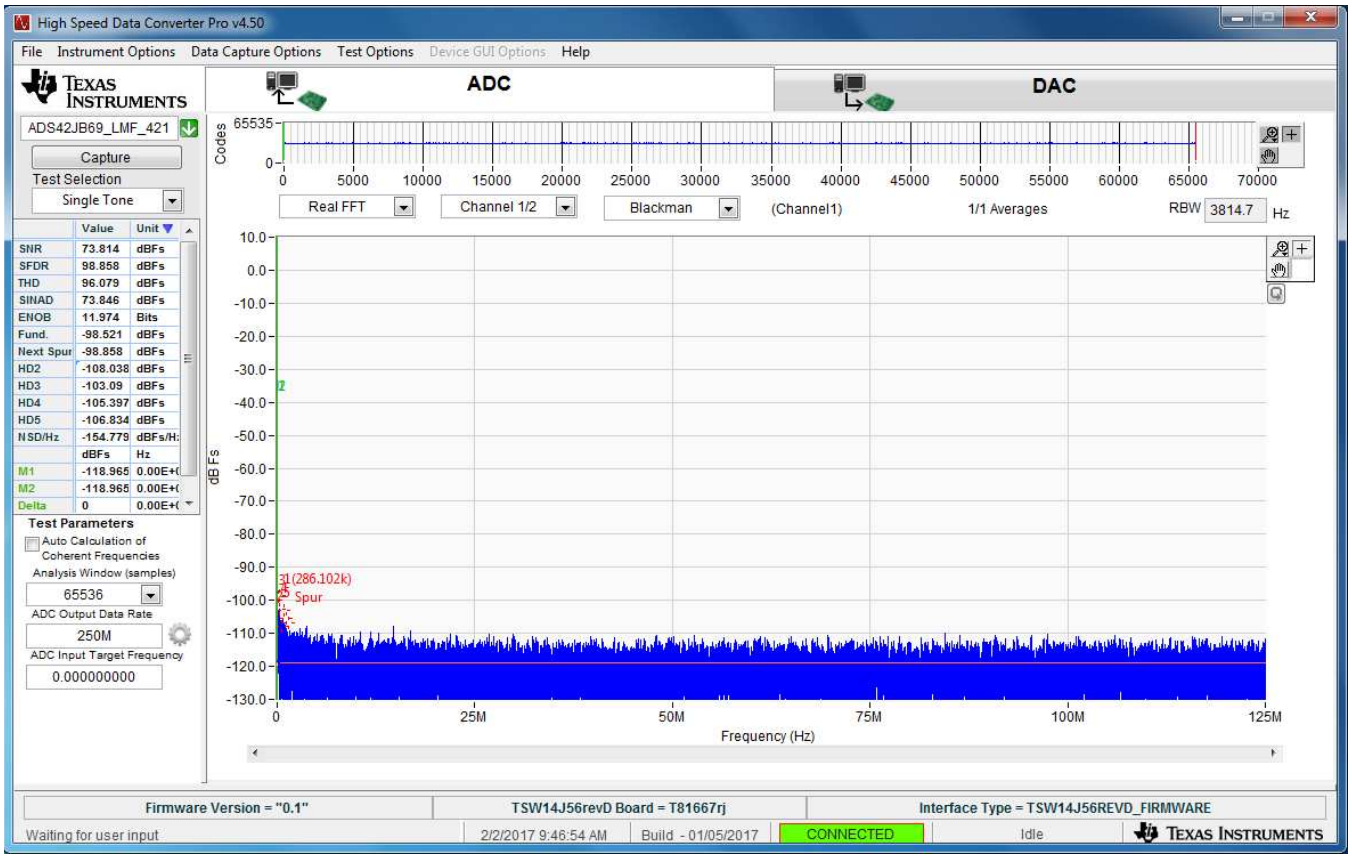

Figure 4. HSDC Pro Software Setup

8. Start the HSDC Pro GUI and follow the onscreen prompts to connect to the TSW14J5x board.
9. In the ADC selection box, select **ADS42JBxx_LMF_421**. xx represents the unique part number for the device being evaluated. Table 2 summarizes the ADC to choose based on the device and mode being evaluated.

Table 2. ADC device ini file selection in HSDC Pro

Device	Mode	HSDC Pro ini file
ADS42JB46	20x	ADS42JB46_LMF_222
ADS42JB46	10x	ADS42JB46_LMF_421
ADS42JB49	20x	ADS42JB49_LMF_222
ADS42JB49	10x	ADS42JB49_LMF_421
ADS42JB69	20x	ADS42JB69_LMF_222
ADS42JB69	10x	ADS42JB69_LMF_421

10. After selecting the appropriate ADC, click **Yes** when prompted to download firmware.
11. After the firmware downloads, LED's D8 and D3 should be ON for the TSW14J5xEVM.
12. Set the data capture to 65536 samples and the ADS Sampling Rate as 250MSPS.
13. Click the **Capture** button to capture data from the ADC.
    - With no input signal connected to the ADC inputs, the captured noise floor of the ADC should look like Figure 4.

14. Connect an analog signal to analog INP or analog INM and capture the data again from the ADC. Figure 5 shows data captured from the ADC with a 25-MHz sinusoid at analog INP and sampling rate of 250 MSPS.
    - You can switch between data from channel 1 and 2 of the ADC from the HSDC Pro GUI interface. Refer to the HSDC Pro GUI users guide (SLWU087) for more details.

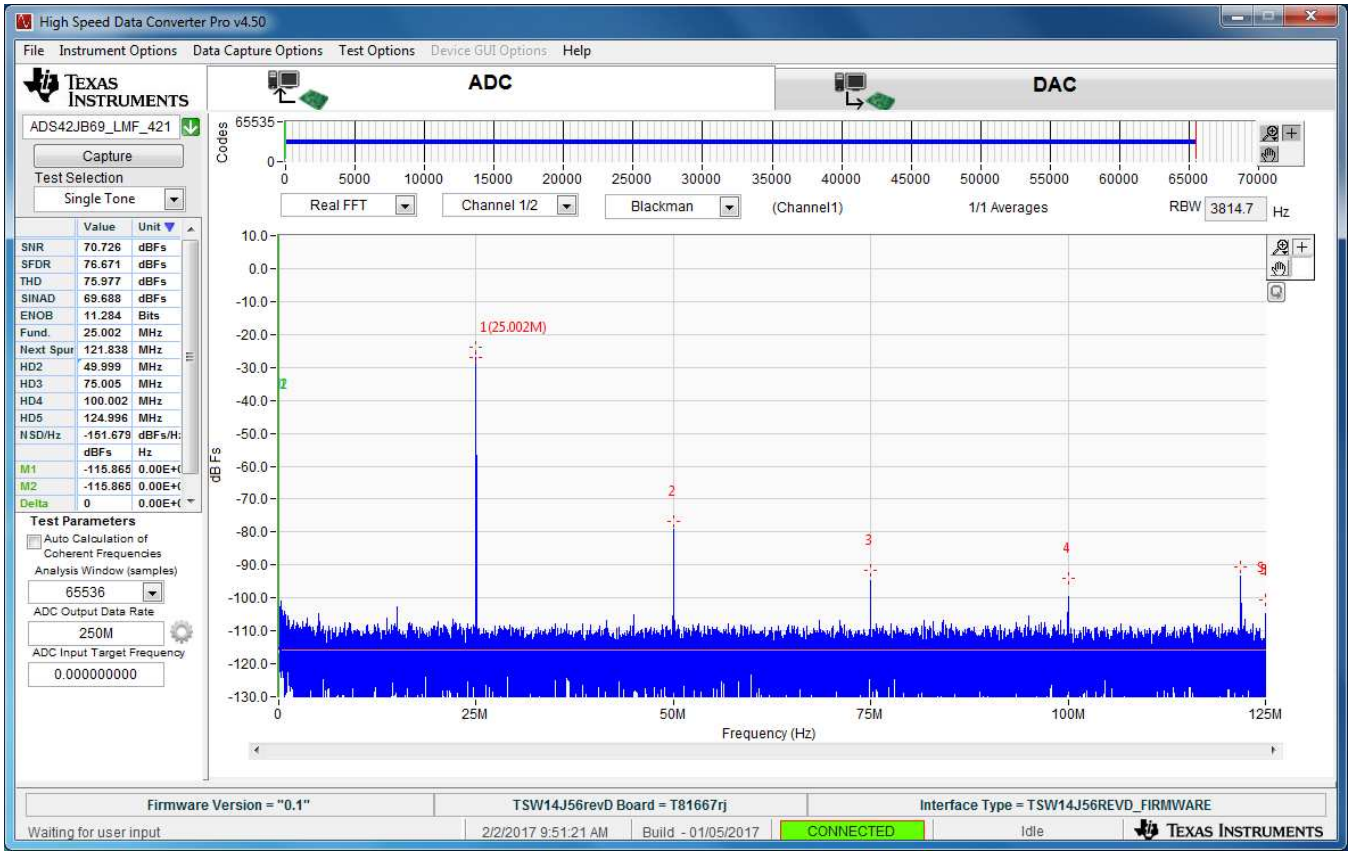

Figure 5. ADC Data Capture, 25 MHz Sinusoid, 250 MSPS Sampling Rate

3 Software Operation

The software GUI allows full programming control of the ADS42JBxx and LMK04828 devices. Figure 6 shows the GUI front panel which contains a block diagram of the ADS42JBxx. Clicking on the ADS42JBxx tab allows configuration of the settings for the device. Detailed descriptions for each screen of the GUI are given in this section. Please refer to the datasheet (ADS42JB46 - SLAS621, ADS42JBx9 - SLAS900) for more detailed explanations of the register fields.

3.1 Top Level GUI Controls

Figure 6 shows the top-level view of the GUI which contains the block diagram of the ADS42JBxx. Along the top of the GUI are four tabs that can be used to navigate and configure the device. Also on the top-right is the **The Reconnect FTDI?** Button, this Button can be used to initialize the FTDI device in case it was disconnected. The USB Status indicator is provided to show that the GUI is successfully connected to the EVM. If the USB is disconnected or the device isn't communicating, then the green indicator light will turn off. Additionally, monitoring the power supply current when toggling the power down mode is a simple way to verify that the GUI is communicating with the device.

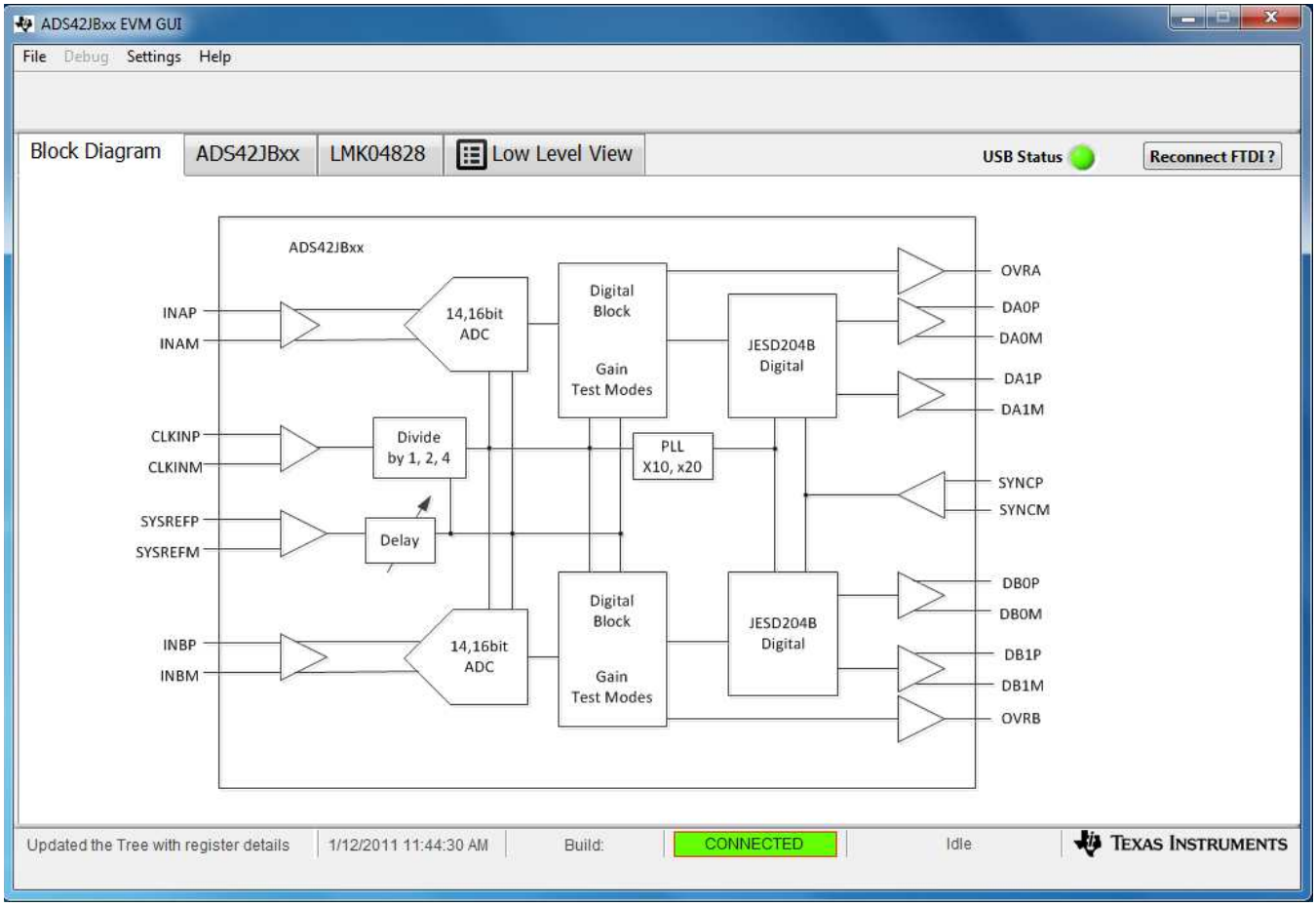

Figure 6. Top-Level Block Diagram Window of the ADS42JBxx GUI

3.2 ADC Controls

Clicking the ADS42JBxx tab brings up the ADC controls as seen in Figure 7. The *ADS42JBxx* tab provides various controls to configure the ADC and the JESD204B standard. Table 3 describes the controls seen in this window.

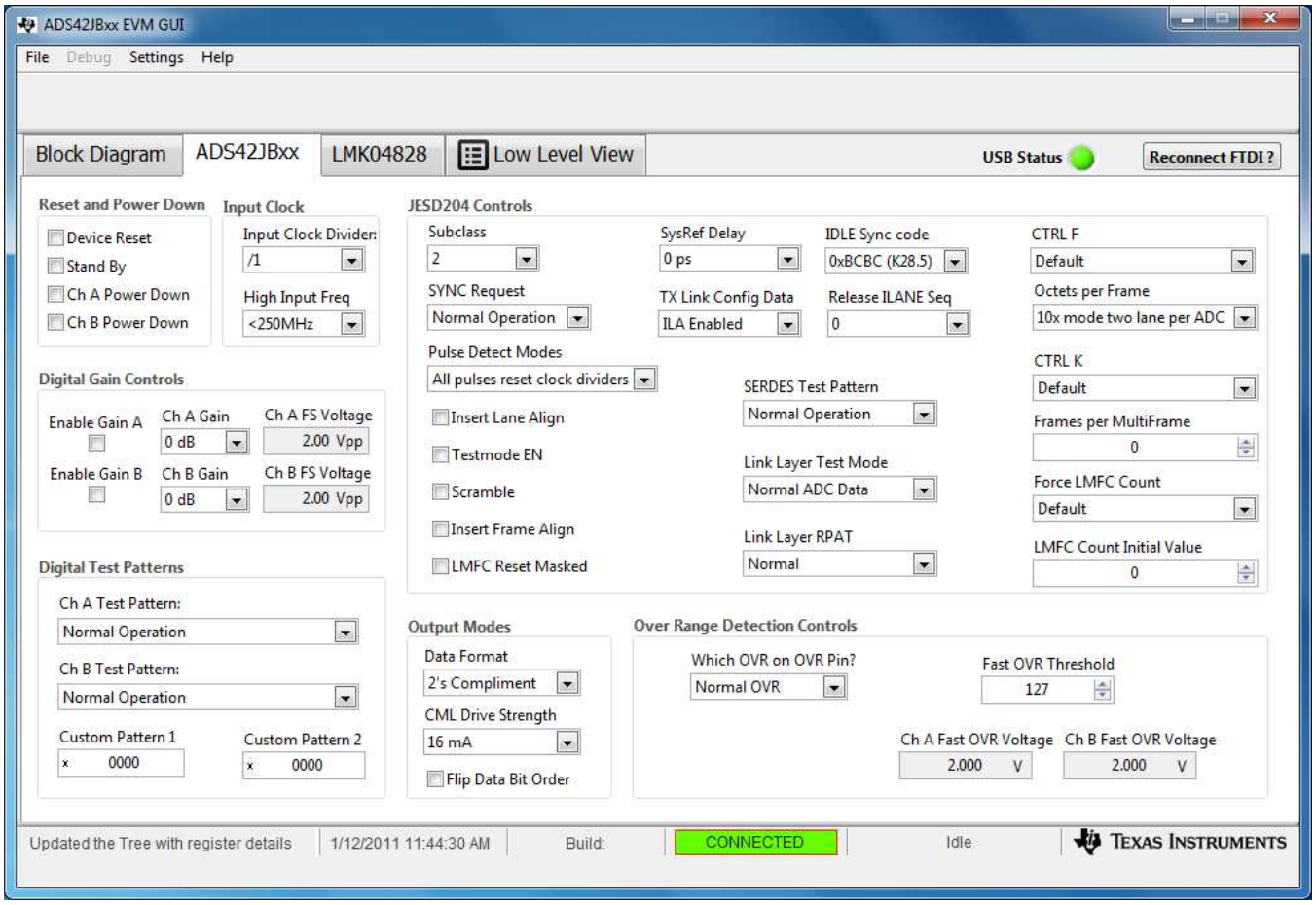

Figure 7. ADC Controls Window of the ADS42JBxx GUI

Table 3. ADC Controls Window Descriptions

Section	Control	Description
Reset and Power Down	Device Reset	Automatically clears the device, so only a single mouse click is needed
	Stand By	ADC is placed into standby mode. Both ADCs are powered down (input clock buffer and CML output buffers are alive)
	Ch A Power Down	Turn ON and OFF channel A
	Ch B Power Down	Turn ON and OFF channel B
Input Clock	Input Clock Divider	Internal clock divider for input sample clock
	High Input Freq	Change as necessary for input frequencies over or under 250MHz
Digital Gain Controls	Enable Gain A	Enables digital gain for channel A
	Ch A Gain	Set gain for channel A between -2.7dB to 6dB
	Ch A FS Voltage	Automatically sets the equivalent Full-Scale Input Voltage when the CH A Gain is set
	Enable Gain B	Enables digital gain for channel B
	Ch B Gain	Set gain for channel B between -2.7dB to 6dB
	Ch B FS Voltage	Automatically sets the equivalent Full-Scale Input Voltage when the CH B Gain is set
Digital Test Patterns	Ch A Test Pattern	Select from 12 different test patterns to be applied as inputs to JESD block for channel A
	Ch B Test Pattern	Select from 12 different test patterns to be applied as inputs to JESD block for channel B
	Custom Pattern 1	Add in a custom 16-bit test pattern 1 for both channels
	Custom Pattern 2	Add in a custom 16-bit test pattern 2 for both channels
Output Modes	Data Format	Set the digital output data format
	CML Drive Strength	Changes JESD output buffer current
	Flip Data Bit Order	Output data order is reversed: MSB – LSB
Over Range Detection Controls	Which Ovr on Ovr Pin?	Select if normal or fast OVR signal is presented on OVRA, OVRB pins
	Fast OVR Threshold	Set the input voltage level at which the overload is detected. The threshold at which fast OVR is triggered is (full-scale × [the decimal value of the FAST OVR THRESHOLD bits] / 127)
	Ch A Fast OVR Voltage	Overrange indication channel A (Ch A FS Voltage × [Fast OVR Threshold / 127])
	Ch B Fast OVR Voltage	Overrange indication channel B (Ch B FS Voltage × [Fast OVR Threshold / 127])

Table 3. ADC Controls Window Descriptions (continued)

Section	Control	Description
JESD204B Controls	Subclass	Sets JESD204B subclass
	SysRef Delay	Set the delay of the SYSREF input with respect to the input clock
	IDLE Sync Code	Sets output pattern when SYNC~ is asserted
	SYNC Request	Generates synchronization request
	TX Link Config Data	Disables sending initial link alignment (ILA) sequence when SYNC~ is de-asserted
	Release ILANE Seq	Delays the generation of the lane alignment sequence by 0, 1, 2, or 3 multiframes after the code group synchronization
	Pulse Detect Modes	Selects different detection modes for SYSREF (subclass 1) and SYNC (subclass 2)
	Insert Lane Align	Inserts a lane alignment character (K28.3) for the receiver to align to the lane boundary per section 5.3.3.5 of the JESD204B specification
	Testmode EN	Generates a long transport layer test pattern mode according to the 5.1.63 clause of the JESD204B specification
	Scramble	Scramble enable bit in the JESD204B interface
	Insert Frame Align	Inserts a frame alignment character (K28.7) for the receiver to align to the frame boundary per section 5.3.3.4 of the JESD204B specification
	LMFC Reset Masked	Mask LMFC reset coming to digital
	SERDES Test Pattern	Sets test patterns in the transport layer of the JESD204B interface
	Link Layer Test Mode	Generates a pattern according to clause 5.3.3.8.2 of the JESD204B document
	Link Layer RPAT	Changes the running disparity in modified RPAT pattern test mode
	CTRL F	Enables bit for number of octets per frame
	Octets per Frame	Sets number of octets per frame (F)
	CTRL K	Enables bit for number of frames per multiframe
	Frames per multiframe	Sets number of frames per multiframe
	Force LMFC Count	Forces LMFC count, enables using a different starting value for the LMFC counter
	LMFC Count Initial Value	The initial value that the LMFC count resets to

3.3 LMK Controls

Click the *LMK04828* tab located at the top of the GUI. A new window opens to provide four tabs that can be used configure the LMK04828, Figure 8 shows the PLL1 Configuration, PLL2 Configuration, Sys and Sync and Output Clock tabs. Clicking on each option opens a new panel in the GUI for control of that section.

3.3.1 PLL1 Configuration

By default, the *PLL1 Configuration* tab is shown when LMK04828 tab is selected. To the right of the panel is a block diagram, shown in Figure 8. This panel controls the PLL1 settings of the LMK04828. Once these values are properly entered and PLL1 becomes locked, LED D1 (LMK Locked) on the ADS42JBxxEVM illuminates. Some reasons for this not illuminating are using the wrong divider values or the reference oscillator tolerance (ppm) is too large.

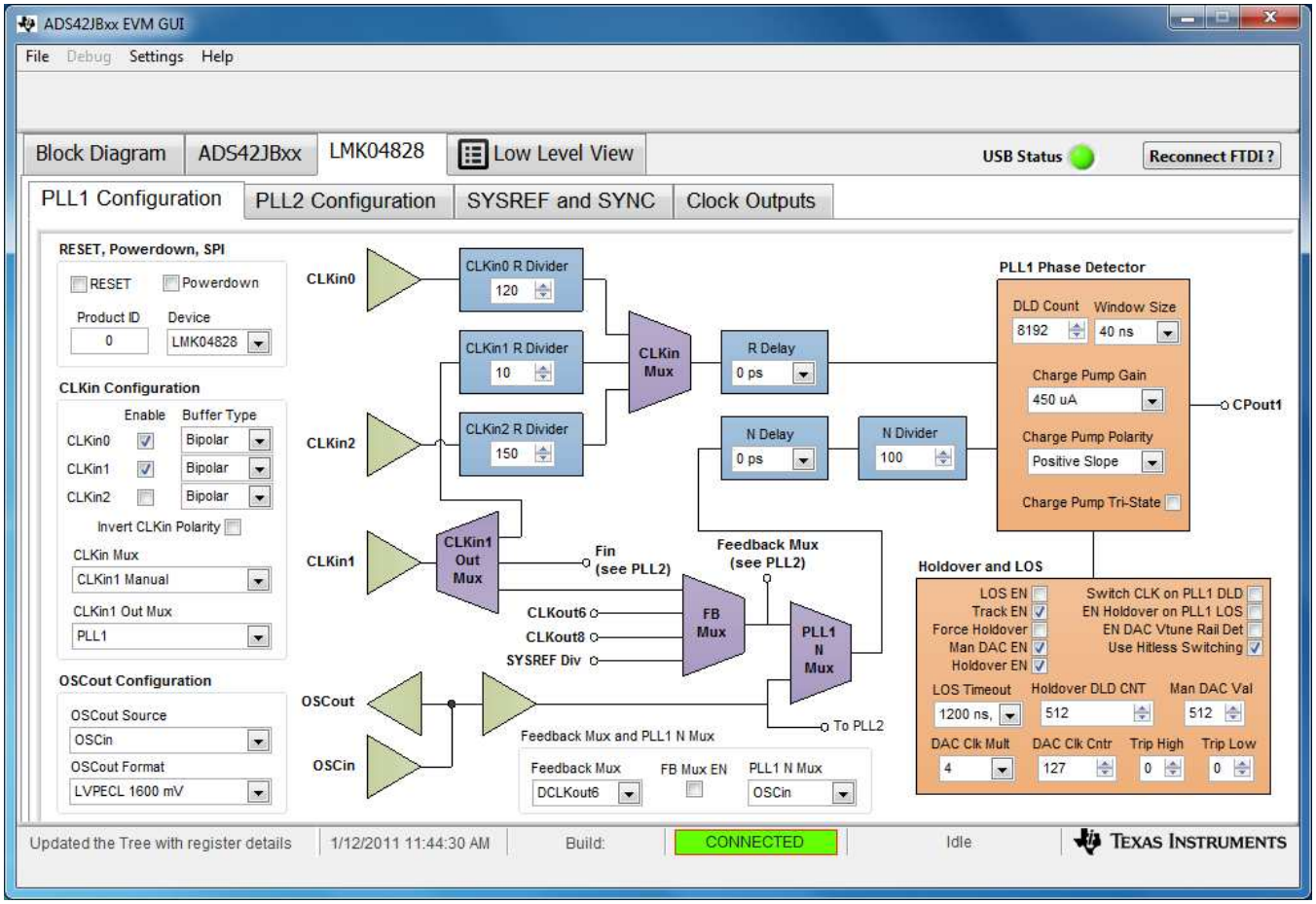

Figure 8. LMK04828 Outputs Control Window of the ADS42JBxx GUI

3.3.2 PLL2 Configuration

Clicking the *PLL2 Configuration* tab opens a new window with a block diagram of PLL2 as shown in Figure 9. This panel controls the PLL2 settings of the LMK04828. Once these values are properly entered and PLL2 becomes locked, LED D4 (PLL2 Locked) on the ADS42JBxxEVM illuminates. A wrong divider value would be a reason for this LED not illuminating. Use the LMK clock design tools when determining external PLL loop filter components. Go to the LMK04828 product folder on the TI website to download this tool and other application notes.

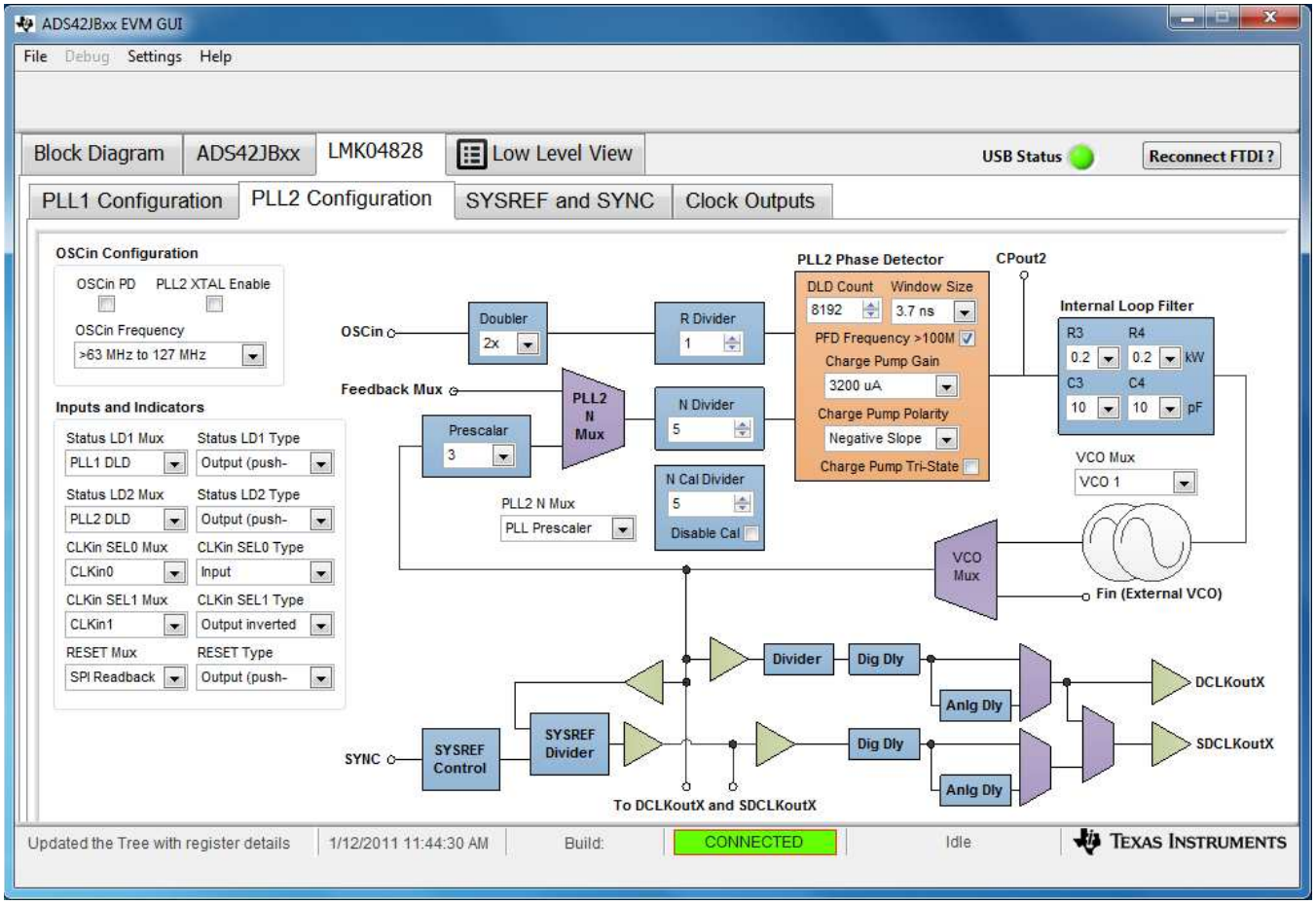

Figure 9. LMK04828 PLL2 Controls

3.3.3 SYSREF and SYNC

Clicking *SYSREF and SYNC* tab opens a new window as shown in Figure 10. This panel controls the SYSREF and SYNC output global settings of the LMK04828. The settings made in this panel apply to all SYSREF outputs. Using the SYNC input causes all active clock outputs to share a rising edge as programmed by fixed digital delay. The SYNC event must occur for digital delay values to take effect.

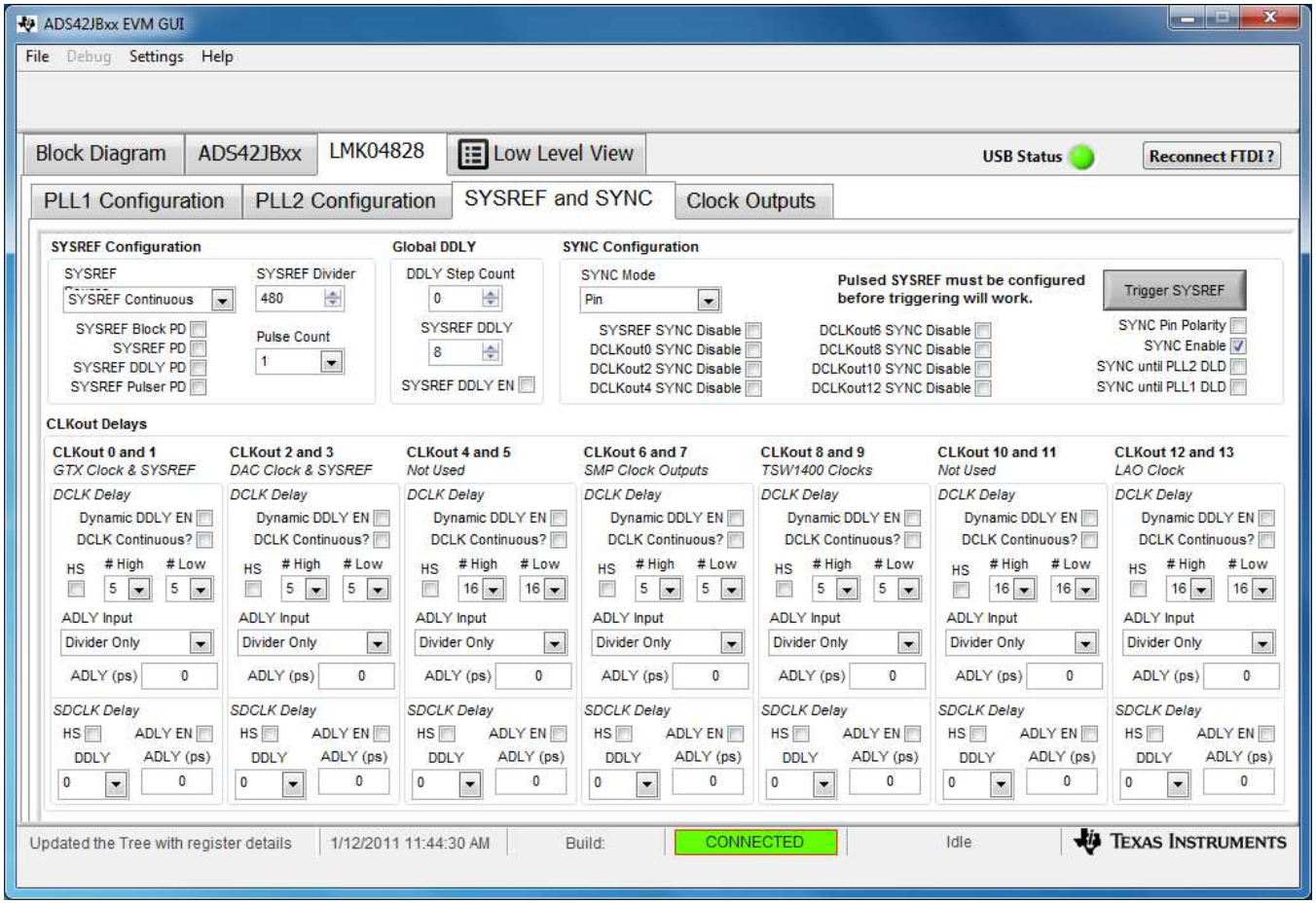

Figure 10. LMK04828 SYSREF and SYNC Settings

3.3.4 Clock Outputs

Clicking the *Clock Outputs* tab opens a new window as shown in Figure 11. This panel controls the output clock settings of the LMK04828. The LMK0482x family features a total of 14 PLL2 clock outputs driven from the internal or external VCO. The 14 clock outputs from PLL2 can be configured to drive seven JESD204B converters or other logic devices using device and SYSREF clocks. Not limited to JESD204B applications, each of the 14 outputs can be individually configured as high performance outputs for traditional clocking systems.

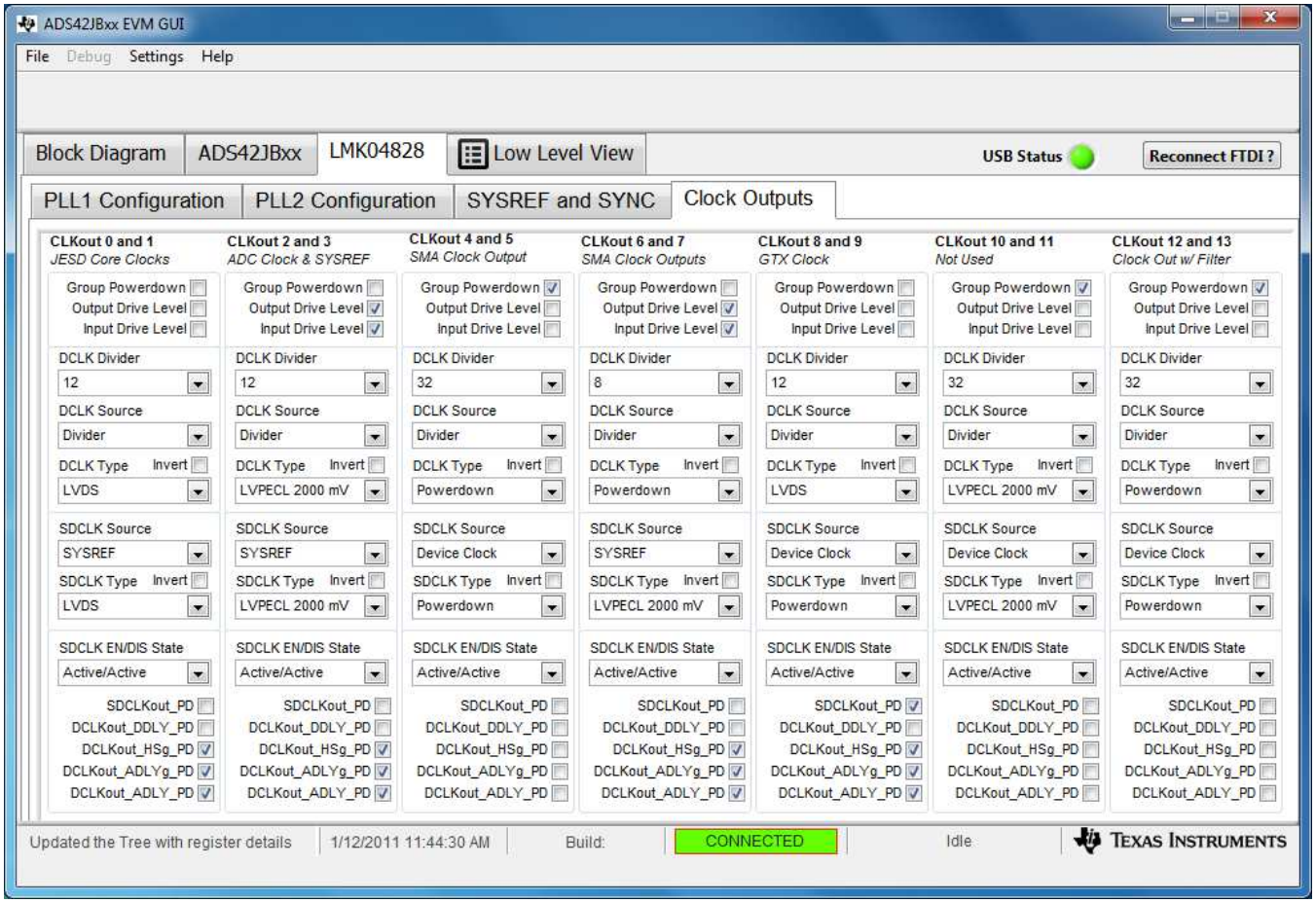

Figure 11. LMK04828 Output Clock Settings

3.4 Low Level View

The Low Level View tab can be used to access the various registers of the LMK04828 and ADS42JBxx. High-level control of most of these registers is accessible in the ADS42JBxx tab and LMK04828 tab. This page also provides the option of saving a register configuration or loading a previously saved configuration. Figure 12 shows a screen shot of the Low Level View tab.

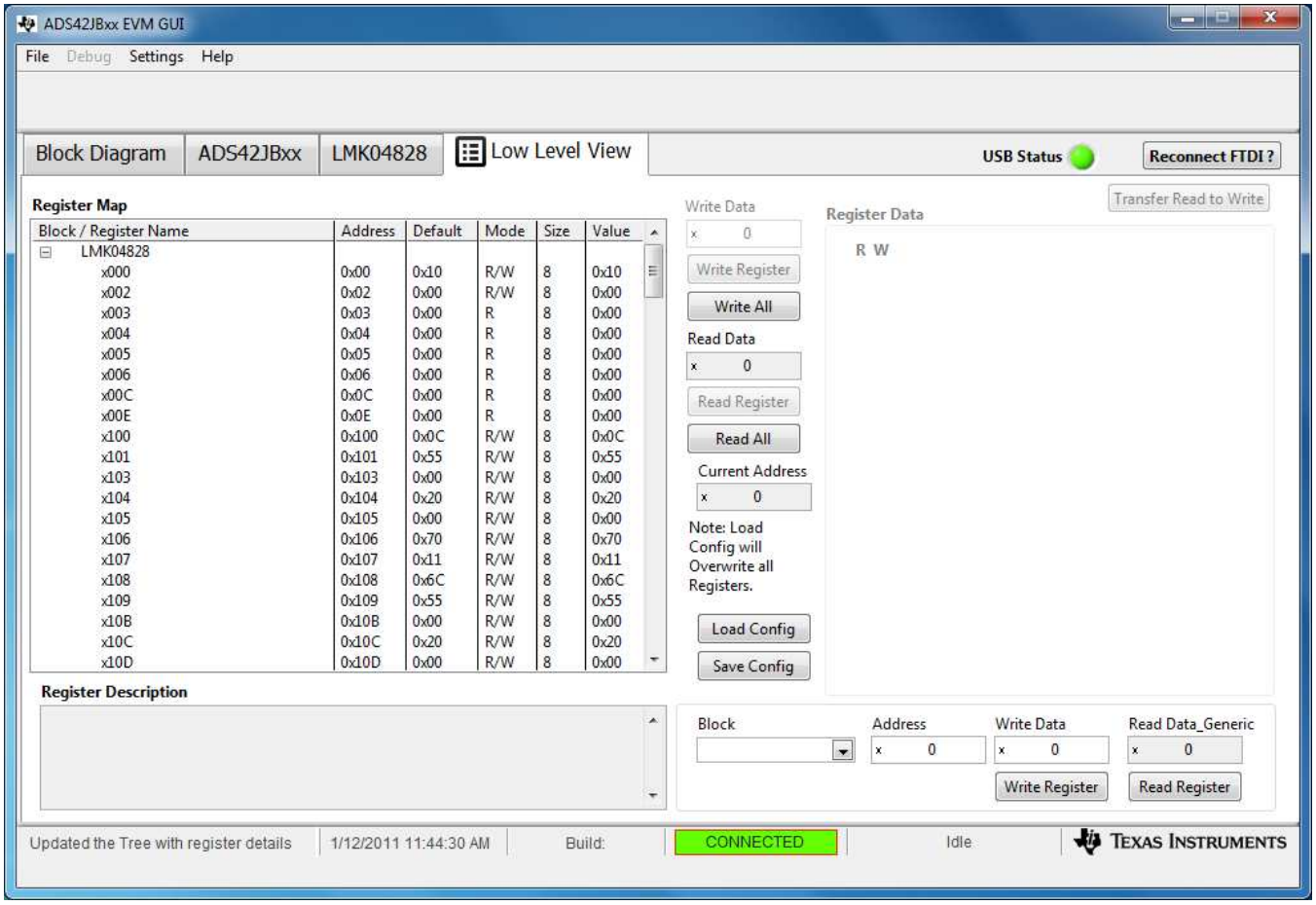

Figure 12. Low Level View

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from C Revision (April 2016) to D Revision **Page**

- Changed TSW14J56EVM throughout the document to TSW14J5xEVM (TSW14J56 to TSW14J5x, as well). 1
- Updated images and text in the *Software Control* section due to software changes..... 4
- Updated images and text in the *Software Operation* section due to software changes 9

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。
上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社
東京都新宿区西新宿６丁目２４番１号
西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page
電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

   6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

   6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ('TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265