NCP5222

High Performance Dual-Channel / Two-Phase Synchronous Buck Controller for Notebook Power System

The NCP5222, a fast−transient−response and high−efficiency dual−channel / two−phase buck controller with built−in gate drivers, provides multifunctional power solutions for notebook power system. 180° interleaved operation between the two channels / phases has a capability of reducing cost of the common input capacitors and improving noise immunity. The interleaved operation also can reduce cost of the output capacitors with the two−phase configuration. Input supply voltage feedforward control is employed to deal with wide input voltage range. On−line programmable and automatic power−saving control ensures high efficiency over entire load range. Fast transient response reduces requirement on the output filters. In the dual−channel operation mode, the two output power rails are regulated individually. In the two−phase operation mode, the two output power rails are connected together by an external switch and current−sharing control is enabled to balance power delivery between phases.

Features

- Wide Input Voltage Range: 4.5 V to 27 V
- Adjustable Output Voltage Range: 0.8 V to 3.3 V
- Option for Dual−Channel and Two−Phase Modes
- Fixed Nominal Switching Frequency: 300 kHz
- 180° Interleaved Operation Between the Two Channels in Continue−Conduction−Mode (CCM)
- Adaptive Power Control
- Input Supply Voltage Feedforward Control
- Transient−Response−Enhancement (TRE) Control
- Resistive or Inductor’s DCR Current Sensing
- 0.8% Internal 0.8 V Reference
- Internal 1 ms Soft−Start
- Output Discharge Operation
- Built−in Adaptive Gate Drivers
- Input Supplies Undervoltage Lockout (UVLO)
- Output Overvoltage and Undervoltage Protections
- Accurate Over Current Protection
- Thermal Shutdown Protection
- QFN−28 Package
- This is a Pb−Free Device

Typical Applications

- CPU Chipsets Power Supplies
- Notebook Applications

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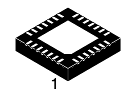


QFN28
CASE 485AR

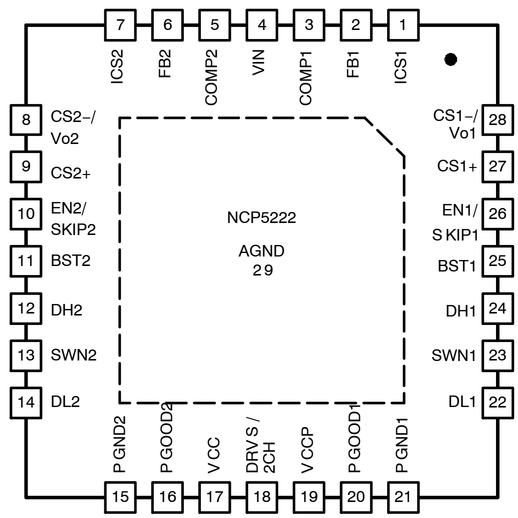
MARKING DIAGRAM

N5222
ALYW▪
▪

A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP5222MNR2G	QFN28 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

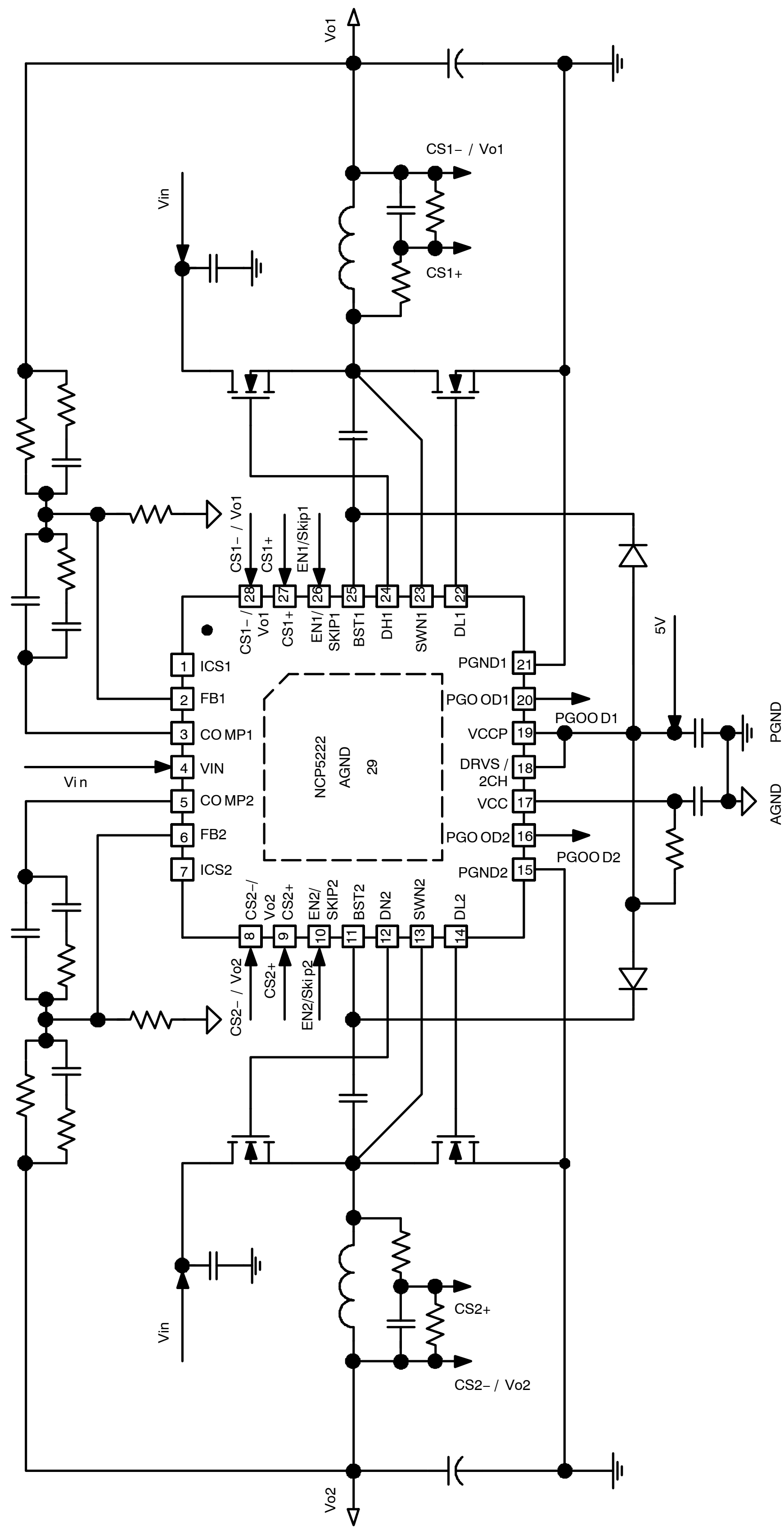


Figure 1. Typical Application Diagram for A Dual−Channel Application

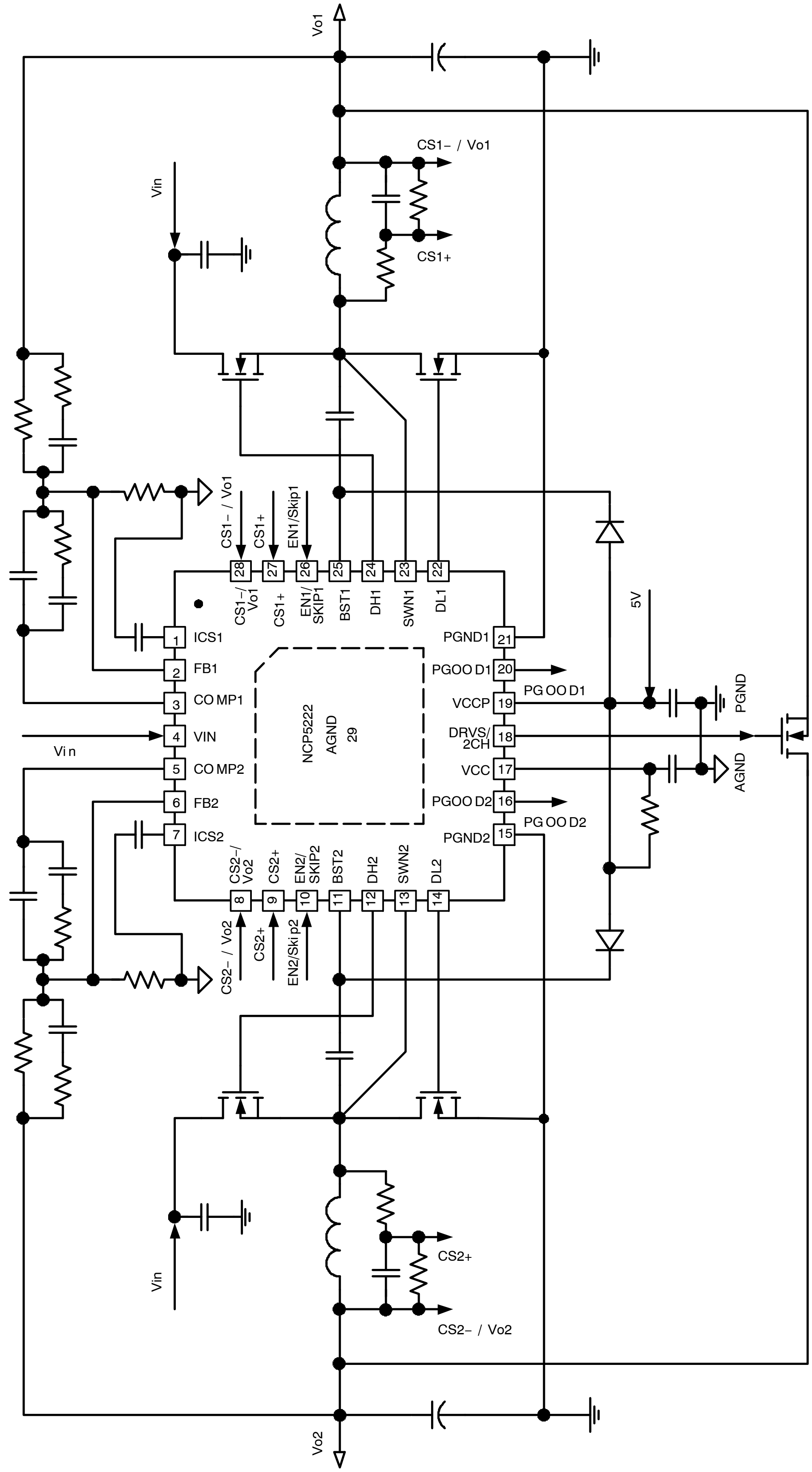


Figure 2. An Application Diagram for A Two−Phase Application

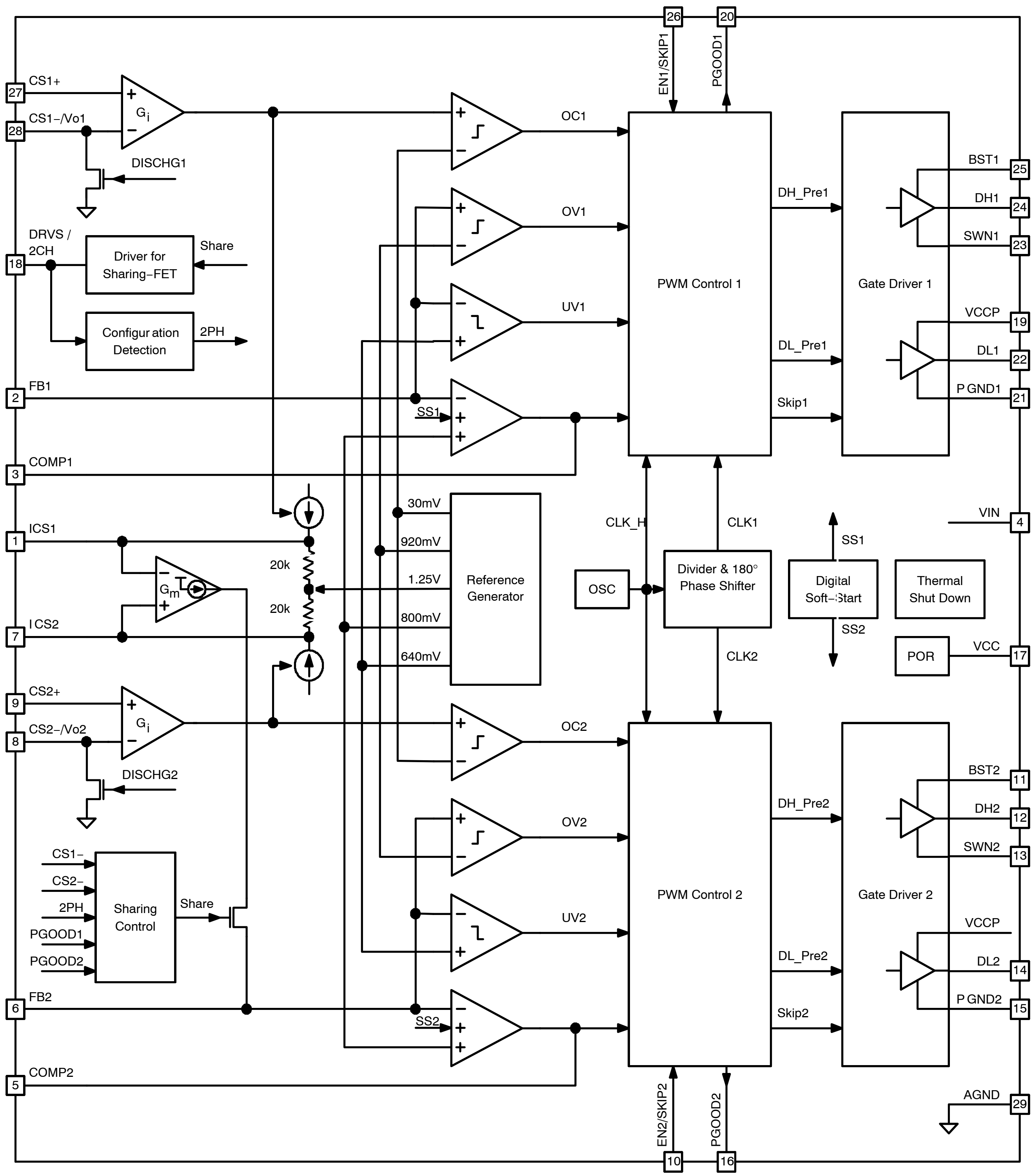


Figure 3. Functional Block Diagram

PIN DESCRIPTION

Pin No.	Symbol	Descriptions
1	ICS1	Current−Sense Output 1. Output of the current−sense amplifier of channel 1.
2	FB1	Feedback 1. Output voltage feedback of channel 1.
3	COMP1	COMP1. Output of the error amplifier of channel 1.
4	VIN	Vin. Input supply voltage monitor input.
5	COMP2	COMP2. Output of the error amplifier of channel 2.
6	FB2	Feedback 2. Output voltage feedback of channel 2.
7	ICS2	Current−Sense Output 2. Output of the current−sense amplifier of channel 2.
8	CS2−/ Vo2	Current Sense 2−. Inductor current differential sense inverting input of Channel 2. Output Voltage 2. Connection to output of Channel 2.
9	CS2+	Current Sense 2+. Inductor current differential sense non−inverting input of Channel 2.
10	EN2 / Skip2	Enable 2. Enable logic input of Channel 2. Skip 2. Power−saving operation (FPWM and Skip) programming pin of Channel 2.
11	BST2	BOOTSTRAP Connection 2.Channel 2 high−side gate driver input supply, a bootstrap capacitor connection between SWN2 and this pin.
12	DH2	High−Side Gate Drive 2. Gate driver output of the high−side N−Channel MOSFET for channel 2.
13	SWN2	Switch Node 2. Switch node between the high−side MOSFET and low−side MOSFET of Channel 2.
14	DL2	Low−Side Gate Drive 2. Gate driver output of the low−side N−Channel MOSFET for channel 2.
15	PGND2	Power Ground 2. Ground reference and high−current return path for the low−side gate driver of channel 2.
16	PGOOD2	Power GOOD 2. Power good indicator of the output voltage of channel 2. (Open drained)
17	VCC	VCC. This pin powers the control section of IC.
18	DRVS / 2CH	Gate Driver for Switch. Gate driver output for the external switch in dual−phase configuration. Dual−Channel. Dual−channel configuration programming pin.
19	VCCP	VCC Power. This pin powers internal gate drivers.
20	PGOOD1	Power GOOD 1. Power good indicator of the output voltage of channel 1. (Open drained)
21	PGND1	Power Ground 1. Ground reference and high−current return path for the low−side gate driver of channel 1.
22	DL1	Low−Side Gate Drive 1. Gate driver output of the low−side N−Channel MOSFET for channel 1.
23	SWN1	Switch Node 1. Switch node between the high−side MOSFET and low−side MOSFET of Channel 1.
24	DH1	High−Side Gate Drive 1. Gate driver output of the high−side N−Channel MOSFET for channel 1.
25	BST1	BOOTSTRAP Connection 1. Channel 1 high−side gate driver input supply, a bootstrap capacitor connection between SWN1 and this pin.
26	EN1 / Skip1	Enable 1. Enable logic input of Channel 1. Skip 1. Power−saving operation (FPWM and Skip) programming pin of Channel 1.
27	CS1+	Current Sense 1+. Inductor current differential sense non−inverting input of Channel 1.
28	CS1−/ Vo1	Current Sense 1−. Inductor current differential sense inverting input of Channel 1. Output Voltage 1. Connection to output of Channel 1.
29	AGND	Analog Ground. Low noise ground for control section of IC.

MAXIMUM RATINGS

Rating	Symbol	Value MIN	Value MAX	Unit
Power Supply Voltages to AGND	V_{CC}, V_{CCP}	−0.3	6.0	V
High−Side Gate Driver Supplies: BST1 to SWN1, BST2 to SWN2 High−Side Gate Driver Voltages: DH1 to SWN1, DH2 to SWN2	$V_{BST1}-V_{SWN1}$, $V_{BST2}-V_{SWN2}$, $V_{DH1}-V_{SWN1}$, $V_{DH2}-V_{SWN2}$	−0.3	6.0	V
Input Supply Voltage Sense Input to AGND	V_{IN}	−0.3	30	V
Switch Nodes	V_{SWN1}, V_{SWN2}	−0.3, $-5_{(<100\ ns)}$	30	V
High−Side Gate Drive Outputs	V_{DH1}, V_{DH2}	−0.3, $-5_{(<100\ ns)}$	36	V
Low−Side Gate Drive Outputs	V_{DL1}, V_{DL2}	−0.3, $-5_{(<100\ ns)}$	6.0	V
Feedback Input to AGND	V_{FB1}, V_{FB2}	−0.3	6.0	V
Error Amplifier Output to AGND	V_{COMP1}, V_{COMP2}	−0.3	6.0	V
Current Sharing Output to AGND	V_{ICS1}, V_{ICS2}	−0.3	6.0	V
Current Sense Input to AGND	V_{CS1+}, V_{CS1-}, V_{CS2+}, V_{CS2-}	−0.3	6.0	V
Mode Program I/O to PGND1	V_{DRVS}	−0.3	6.0	V
Enable Input to AGND	V_{EN1}, V_{EN2}	−0.3	6.0	V
Power Good Output to AGND	V_{PGOOD1}, V_{PGOOD2}	−0.3	6.0	V
PGND1, PGND2 to AGND	V_{GND}	−0.3	0.3	V
Operating Junction Temperature Range	T_J	−40	150	°C
Operating Ambient Temperature Range	T_A	−40	85	°C
Storage Temperature Range	T_{STG}	−55	150	°C
Thermal Characteristics Thermal Resistance Junction to Air (Pad soldered to PCB)	$R_{\theta JA}$	45 (Note 1)		°C/W
Moisture Sensitivity Level	MSL	1		–

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Directly soldered on 4 layer PCB with thermal vias, thermal resistance from junction to ambient with no airflow is around 40~45°C/W (depends on filled vias or not). Directly soldered on 4 layer PCB without thermal vias, thermal resistance from junction to ambient with no air flow is around 56°C/W.
2. This device is sensitive to electrostatic discharge. Follow proper handing procedures.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V, V_{IN} = 12 V, T_A = −40°C to 85°C, unless other noted)

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
SUPPLY VOLTAGE						
Input Voltage	V_{IN}		4.5	–	27	V
V_{CC} Operating Voltage	V_{CC}		4.5	5.0	5.5	V
V_{CCP} Operating Voltage	V_{CCP}		4.5	5.0	5.5	V
SUPPLY CURRENT						
V_{CC} Quiescent Supply Current in FPWM operation	IVCC_FPWM	EN1 = EN2 = 1.95 V, FB1 and FB2 forced above regulation point, DH1, DL1, DH2, and DL2 are open		2.5	5	mA

3. Guaranteed by design, not tested in production.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V, V_{IN} = 12 V, T_A = −40°C to 85°C, unless other noted)

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
SUPPLY CURRENT						
V_{CC} Quiescent Supply Current in power−saving operation	IVCC_PS	EN1 = EN2 = 5 V, FB1 and FB2 forced above regulation point, DH1, DL1, DH2, and DL2 are open		2.5	5	mA
V_{CC} Shutdown Current	IVCC_SD	EN1 = EN2 = 0 V			1	μA
V_{CCP} Quiescent Supply Current in FPWM operation	IVCCP_FPWM	EN1 = EN2 = 1.95 V, FB1 and FB2 forced above regulation point, DH1, DL1, DH2, and DL2 are open			0.3	mA
V_{CCP} Quiescent Supply Current in power−saving operation	IVCCP_PS	EN1 = EN2 = 5 V, FB1 and FB2 forced above regulation point, DH1, DL1, DH2, and DL2 are open			0.3	mA
V_{CCP} Shutdown Current	IVCCP_SD	EN1 = EN2 = 0 V			1	μA
BST Quiescent Supply Current in FPWM operation	IBST_FPWM	EN1 = EN2 = 1.95 V, FB1 and FB2 forced above regulation point, DH1, DL1, DH2, and DL2 are open			0.3	mA
BST Quiescent Supply Current in power−saving operation	IBST_PS	EN1 = EN2 = 5 V, FB1 and FB2 forced above regulation point, DH1, DL1, DH2, and DL2 are open			0.3	mA
BST Shutdown Current	IBST_SD	EN1 = EN2 = 0 V, BST1 = BST2 = 5 V, SWN1 = SWN2 = 0 V			1	μA
V_{IN} Supply Current (Sink)	IVIN	EN1 = EN2 = 5 V			35	μA
V_{IN} Shutdown Current	IVIN_SD	EN1 = EN2 = 0 V			1	μA
VOLTAGE MONITOR						
V_{CC} Start Threshold	VCCUV+	V_{CC} and V_{CCP} are connected to the same voltage source	4.05	4.25	4.48	V
V_{CC} UVLO Hysteresis	VCCHYS		−400	−300	−200	mV
V_{IN} Start Threshold	VINUV+		3.2	3.6	4.0	V
V_{IN} UVLO Hysteresis	VINHYS		−700	−500	−300	mV
Power Good High Threshold	VPGH	PGOOD goes high from higher Vo	105	110	115	%
		Hysteresis		5		%
Power Good Low Threshold	VPGL	PGOOD goes high from lower Vo	85	90	95	%
		Hysteresis		−5		
Power Good High Delay	Td_PGH			150		μs
Power Good Low Delay	Td_PGL			1.5		μs
Output Overvoltage Trip Threshold	FBOVPth	FB compared to 0.8 V	110	115	120	%
		Hysteresis		−5		
Output Overvoltage Fault Latch Delay	OVPTd			1.5		μs
Output Undervoltage Trip Threshold	FBUVPth	FB compared to 0.8 V	75	80	85	%
		Hysteresis		10		
Output Undervoltage Protection Fault Latch Blanking Time	UVPTblk		–	27	–	μs

3. Guaranteed by design, not tested in production.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V, V_{IN} = 12 V, T_A = −40°C to 85°C, unless other noted)

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
INTERNAL REFERENCE						
VFB Regulation Voltage	V_{FB1}, V_{FB2}	T_A = 25°C	0.794	0.8	0.806	V
		T_A = −40°C to 85°C	0.792		0.808	
SWITCHING FREQUENCY						
Normal Operation Frequency	F_{SW}	T_A = 25°C	276	300	324	kHz
		T_A = −40°C to 85°C	270		330	
INTERNAL SOFT−START						
Soft−Start Time	T_{SS}		0.8	1	1.2	ms
SWITCHING REGULATOR						
Ramp Offset Voltage	Vramp_offset	(Note 3)		0.4		V
Ramp Amplitude Voltage	Vramp_V	V_{IN} = 5 V (Note 3)		1.25		V
		V_{IN} = 12 V (Note 3)		3		
Minimum Ton	Ton_min			70		ns
Minimum Toff	Toff_min			360		ns
VOLTAGE ERROR AMPLIFIER						
DC Gain	GAIN_VEA	(Note 3)		88		dB
Unity Gain Bandwidth	Ft_VEA	(Note 3)		15		MHz
Slew Rate	SR_VEA	COMP to GND 100 pF (Note 3)		2.5		V/μs
Output Voltage Swing	Vmax_EA	Isource_EA = 2 mA	3.3	3.6		V
	Vmin_EA	Isink_EA = 2 mA		0.1	0.3	V
DIFFERENTIAL CURRENT SENSE AMPLIFIER						
CS+ and CS−Common−mode Input Signal Range	VCSCOM_MAX	Refer to AGND			3.5	V
V_{CS} to I_{CS} Gain	ICS_GAIN (ICS/VCS)	2PH Mode, V_{CS} = V(CS+) −V(CS−) = 4 mV		0.5		μA/mV
Internal Resistance from ICS to 1.25 V Bias	RICS			20		kΩ
ICS Voltage Dynamic Range	VICS_Dyn	2PH Mode (Note 3)		0.75 ~ 1.75		V
[V(ICS2)−V(ICS1)] to IFB2 Gain	IFB2_GAIN (IFB2/(V(ICS2)−V(ICS1)))	2PH Mode		0.1		μA/mV
Current−Sharing Gain	ISH_GAIN (IFB2/(VCS2−VCS1))	2PH Mode (IFB2/((V(CS2+) −V(CS2−))−(V(CS1+) −V(CS1−)))		1		μA/mV
IFB2 Offset Current	IFB2_offset	2PH Mode, VCS1 = VCS2 = 0 V	−0.5		0.5	μA
IFB2 Current Dynamic Range in 2PH Mode		2PH Mode	−9		9	μA
OVERCURRENT PROTECTION						
OCP Threshold	VTH_OC	V(CS+) − V(CS−), Vo = 0.8 V to 3.3 V	27	30	33	mV
OCP Fault Latch Blanking Time	OCPTblk		−	107	−	μs
SHARING SWITCH GATE DRIVE						
Soft−On Source Current	IDRVS			1		mA
Pull−HIGH Resistance	RH_DRVS			20		Ω
Pull−LOW Resistance	RL_DRVS			10		Ω

3. Guaranteed by design, not tested in production.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V, V_{IN} = 12 V, T_A = −40°C to 85°C, unless other noted)

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
CONFIGURATION DETECTION						
Configuration Detection Time	TCD			53		μs
Pull−LOW Resistance in Detection	RL_CD			2		kΩ
Detection Threshold	VCD	V_{CCP} pin to DRVS/2CH pin		0.5		V
GATE DRIVER						
DH Pull−HIGH Resistance	RH_DH1, RH_DH2			2.5	5	Ω
DH Pull−LOW Resistance	RL_DH1, RL_DH2			1.5	2.5	Ω
DL Pull−HIGH Resistance	RH_DL1, RH_DL2			2	3	Ω
DL Pull−LOW Resistance	RL_DL1, RL_DL2			0.75	1.5	Ω
Dead Time	TLH	DL−off to DH−on (see Figure 4)	10	25	40	ns
	THL	DH−off to DL−on (see Figure 4)	10	25	40	ns
CONTROL LOGIC						
EN Logic Input Voltage Threshold for Disable	VEN_Disable	EN goes low	0.7	1.0	1.3	V
		Hysteresis	150	200	250	mV
EN Logic Input Voltage Threshold for FPWM	VEN_FPWM		1.7	1.95	2.25	V
EN Logic Input Voltage Threshold for Skip	VEN_SKIP	EN goes high	2.4	2.65	2.9	V
		Hysteresis	100	175	250	mV
EN Source Current	IEN_SOURCE	EN = 0 V (Note 3)			0.1	μA
EN Sink Current	IEN_SINK	EN = 5 V (Note 3)			0.1	μA
PGOOD Pin ON Resistance	PGOOD_R	I_PGOOD = 5 mA		70		Ω
PGOOD Pin OFF Current	PGOOD_LK				1	μA
OUTPUT DISCHARGE MODE						
Output Discharge On−Resistance	$R_{discharge}$	EN = 0 V, V_{out} = 0.5 V		25	35	Ω
THERMAL SHUTDOWN						
Thermal Shutdown	T_{sd}	Shutdown Threshold (Note 3)		150		°C
		Hysteresis (Note 3)		−25		°C

3. Guaranteed by design, not tested in production.

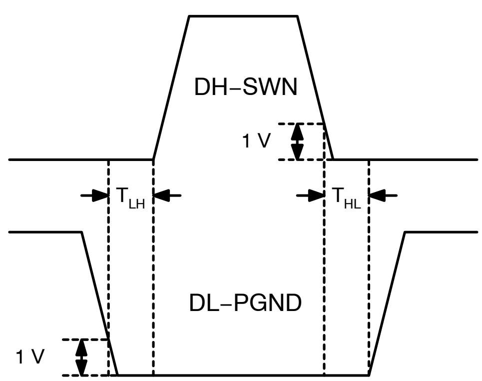


Figure 4. Dead Time between High−Side Gate Drive and Low−Side Gate Drive

General

The NCP5222, a fast−transient−response and high−efficiency dual−channel / two−phase buck controller with builtin gate drivers, provides multifunctional power solutions for notebook power system. 180° interleaved operation between the two channels / phases has a capability of reducing cost of the common input capacitors and improving noise immunity. The interleaved operation also can reduce cost of the output capacitors with the two−phase configuration. Input supply voltage feedforward control is employed to deal with wide input voltage range. On−line programmable and automatic power−saving control ensures high efficiency over entire load range. Fast transient response reduces requirement on the output filters. In the dual−channel operation mode, the two output power rails are regulated individually. In the two−phase operation mode, the two output power rails are connected together by an external switch and current−sharing control is enabled to balance power delivery between phases.

Dual−Channel Mode or Two−Phase Mode

The NCP5222 can be externally configured to be working in dual−channel operation mode or two−phase operation mode. In the dual−channel operation mode, the two output power rails are regulated individually. In the two−phase operation mode, the two output power rails are connected together by an external switch and current−sharing control is enabled to balance power delivery between phases.

Figure 5 shows two typical external configurations. In Figure 5(a), the controller is configured to operate in the dual−channel mode by connecting the pin DRVS with the pin V_{CCP}. In Figure 5(b), the controller is configured to operate in the two−phase mode. In this mode, an external MOSFET SSH is employed to connect the two output power rails together, and the pin DRVS of the NCP5222 provides driving signal to SSH. Two filter capacitors CCS1 and CICS2 are connected with two current−sense output pins ICS1 and ICS2, respectively. A typical timing diagram is shown in Figure 6.

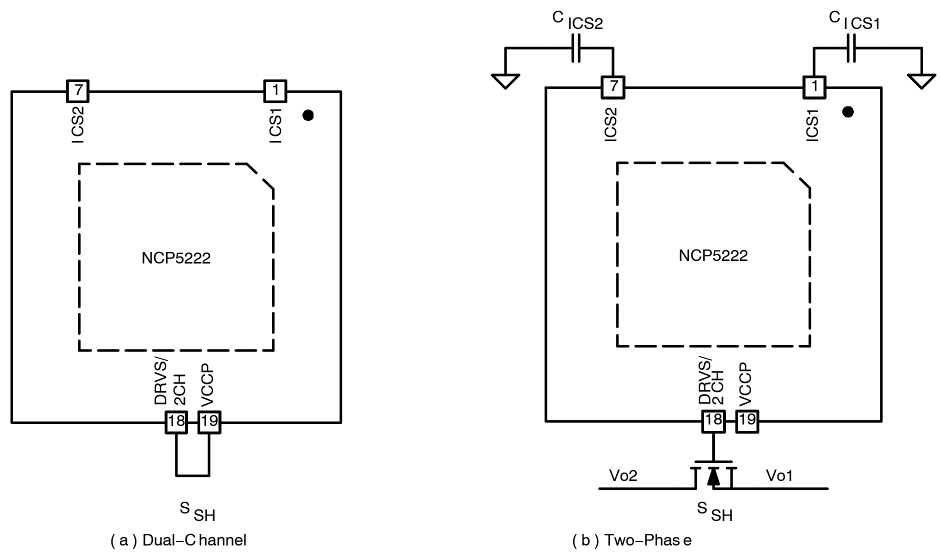


Figure 5. Mode Configurations

Mode Detection

In the initial stage of the IC powering up, there is mode detection period to read the external setup just after V_{IN} and V_{CC} are both ready and at least one of ENs is enabled. In Figure 6, V_{IN} and V_{CC} are powered up first. At 3.5 us after EN2 goes high, a 53 μs mode detection period starts. The DRVS pin is pulled down by an internal 2 kΩ. At the end of the mode detection, if the DRVS is higher than V_{CCP} − 0.5 V the system goes to the dual−channel mode and leaves DRVS high impedance. If the DRVS is lower than V_{CCP} − 0.5 V, the system goes to the two−phase mode and the DRVS pin is pulled down to PGND1 by an internal 10 Ω FET.

DRVS Softstart in Two−Phase Mode

In the two−phase mode, the DRVS softstart begins after the both PGOOD1 and PGOOD2 become valid. During the DRVS softstart, 1 mA current is sourced out from the DRVS pin and thus voltage in DRVS is ramping up. The DRVS soft−start is complete after the DRVS voltage is higher than V_{CCP} − 0.2 V, and then the DRVS pin is pulled up to V_{CCP} by an internal 20 Ω FET.

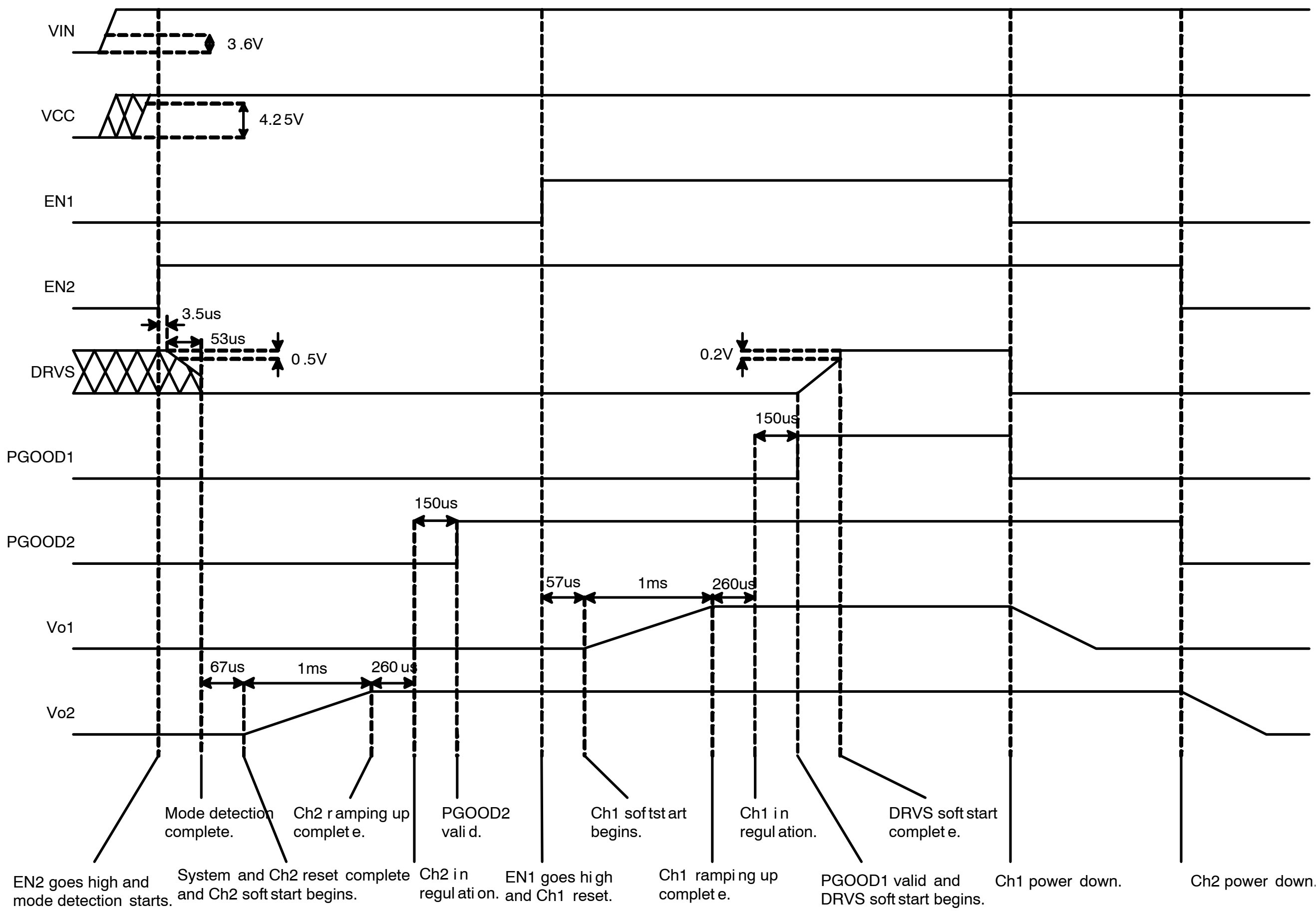


Figure 6. Timing Diagram in Two−Phase Mode

Control Logic

The NCP5222 monitors V_{CC} with undervoltage lockout (UVLO) function. If V_{CC} is in normal operation range, the converter has a soft−start after EN signal goes high. The internal digital soft−start time is fixed to 1 ms. The two channels share one DAC ramping−up circuit. If the two ENs become high at the same time (within 5 μs), the two channels start soft−start together; If one channel's EN comes when the other channel is powering up, the channel starts powering up after the other channel completes soft start. If one channel's EN comes when the other channel is in any fault condition, the channel does not start powering up until the fault is cleared. The NCP5222 has output discharge operation through one internal 20 Ω MOSFET per channel connected from CS−/Vo pin to PGND pin, when EN is low or the channel is under any fault condition.

Current−Sense Network

In the NCP5222, the output current of each channel is sensed differentially. A high gain and low offset−voltage differential amplifier in each channel allows low−resistance current−sense resistor or low−DCR inductor to be used to minimize power dissipation. For lossless inductor current sensing as shown in Figure 7, the sensing RC network should satisfy:

$$\frac{L}{DCR} = \frac{R_{CS1} \cdot R_{CS2}}{R_{CS1} + R_{CS2}} \cdot C_{CS} = k_{CS} \cdot R_{CS1} \cdot C_{CS} \quad \text{(eq. 1)}$$

where the dividing−down ratio k_{CS} is

$$k_{CS} = \frac{R_{CS2}}{R_{CS1} + R_{CS2}} \quad \text{(eq. 2)}$$

DCR is a DC resistance of an inductor, and normally CCS is selected to be around 0.1 μF. The current−sense input voltage across CS+ and CS− is

$$V_{CS} = k_{CS} \cdot I_L \cdot DCR \quad \text{(eq. 3)}$$

If there is a need to compensate measurement error caused by temperature, an additional resistance network including a negative−temperature−coefficient (NTC) thermistor may be connected with C_{CS} in parallel.

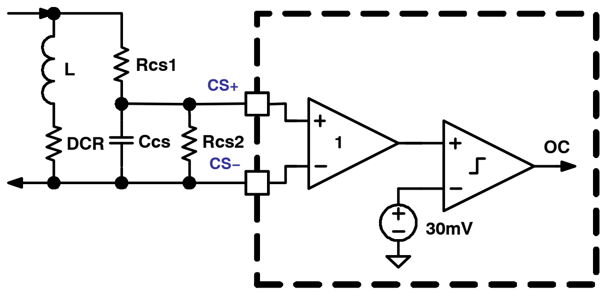


Figure 7. Current Sensing Network and Overcurrent Protection

Output Regulation

As shown in Figure 8, with a high gain error amplifier and an accurate internal reference voltage, the NCP5222 regulates average DC value of the output voltage to a design target by error integration function. The output has good accuracy over full−range operation conditions and external component variations.

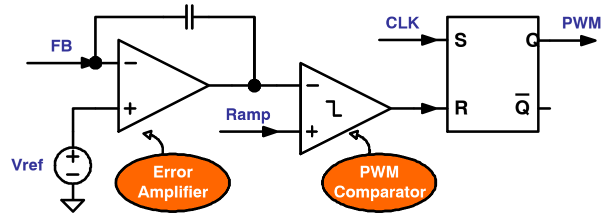


Figure 8. PWM Output Regulation

Output Regulation in Dual−Channel Mode

In dual−channel operation mode, the two channels regulate their output voltage individually. As shown in Figure 9, the output voltage is programmed by external feedback resistors.

$$V_o = \left(1 + \frac{R_1}{R_4}\right) \cdot V_{ref} \qquad \text{(eq. 4)}$$

where Vref is an internal 0.8 V reference voltage.

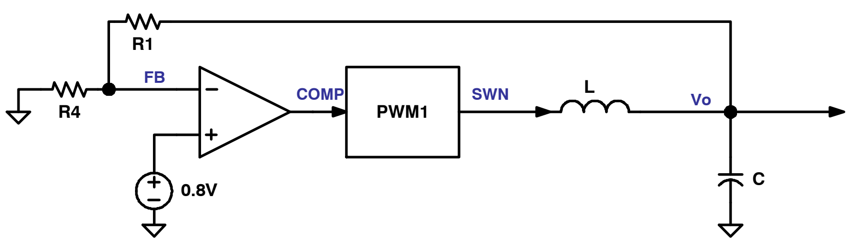


Figure 9. PWM Output Regulation in Dual−Channel Mode

Output Regulation in Two−Phase Mode

Figure 10 shows a block diagram for explanation of the output regulation in the two−phase mode. Under the two−phase configuration, a MOSFET SSH called sharing switch is employed to connect two power rails V_{O1} and V_{O2}.

$$I_{Share} = \frac{V_{O2} - V_{O1}}{R_{ON\_S}} \qquad \text{(eq. 5)}$$

where R_{ON_S} is on resistance of S_{SH}.

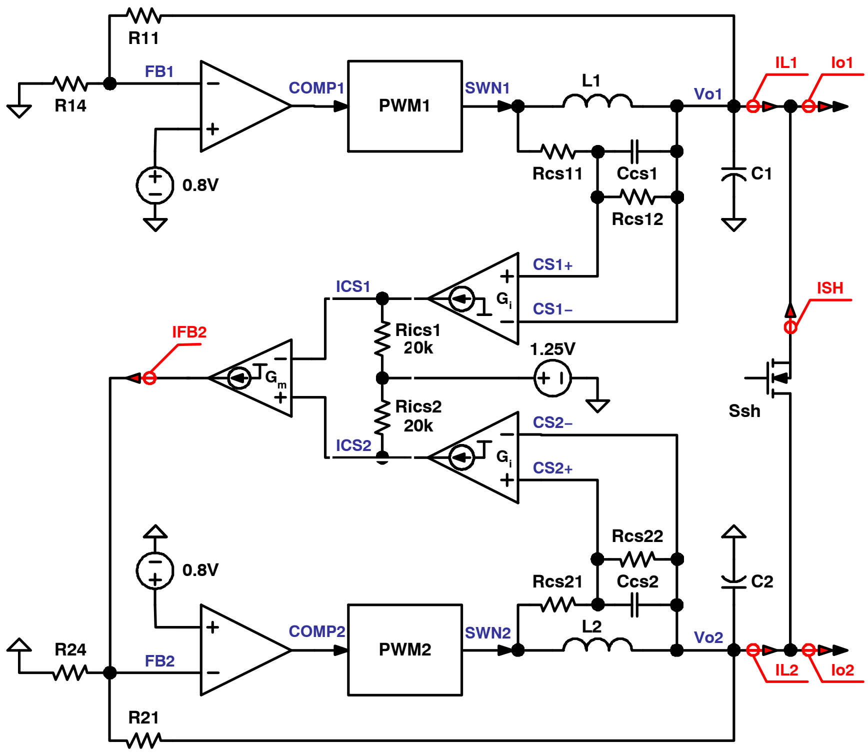


Figure 10. PWM Output Regulation in Two−Phase Mode

In the two−phase operation, the phase 1 has the same output regulation control as what is in the dual−channel operation. The output voltage is

$$V_{O1} = \left(1 + \frac{R_{11}}{R_{14}}\right) \cdot V_{ref1} = \left(1 + \frac{R_{11}}{R_{14}}\right) \cdot 0.8 \quad \text{(eq. 6)}$$

However, in order to achieve current−sharing function, the output voltage in phase 2 is adjusted to be higher or lower than V_{O1} to balance the power delivery in the two phases, by means of an injection current I_{FB2} into the phase 2 error amplifier's non−inverting node. Thus output voltage of the phase 2 is

$$\begin{aligned} V_{O2} &= \left(1 + \frac{R_{21}}{R_{24}}\right) \cdot V_{ref2} - I_{FB2} \cdot R_{21} \\ &= \left(1 + \frac{R_{21}}{R_{24}}\right) \cdot 0.8 - I_{FB2} \cdot R_{21} \end{aligned} \quad \text{(eq. 7)}$$

The injection current I_{FB2} is proportional to the difference between the two current−sense output signals V_{ICS2} and V_{ICS1}, that is

$$\begin{aligned} I_{FB2} &= G_{IFB2} \cdot \left(V_{ICS2} - V_{ICS1}\right) \\ &= 1x10^{-4} \cdot \left(V_{ICS2} - V_{ICS1}\right) \\ &= 1x10^{-3} \cdot \left(V_{CS2} - V_{CS1}\right) \\ &= 1x10^{-3} \cdot \left(k_{CS2} \cdot DCR_2 \cdot I_{L2} - k_{CS1} \cdot DCR_1 \cdot I_{L1}\right) \end{aligned} \quad \text{(eq. 8)}$$

where

$$\begin{aligned} V_{ICS1} &= G_{ICS1} \cdot R_{ICS1} \cdot V_{CS1} + V_{ICS\_Offset} \\ &= 10 \cdot V_{CS1} + 1.25 \end{aligned} \quad \text{(eq. 9)}$$

$$\begin{aligned} V_{ICS2} &= G_{ICS2} \cdot R_{ICS2} \cdot V_{CS2} + V_{ICS\_Offset} \\ &= 10 \cdot V_{CS2} + 1.25 \end{aligned} \quad \text{(eq. 10)}$$

$$V_{CS1} = k_{CS1} \cdot I_{L1} \cdot DCR_1 \quad \text{(eq. 11)}$$

$$V_{CS2} = k_{CS2} \cdot I_{L2} \cdot DCR_2 \quad \text{(eq. 12)}$$

and

$$k_{CS1} = \frac{R_{CS12}}{R_{CS11} + R_{CS12}} \quad \text{(eq. 13)}$$

$$k_{CS2} = \frac{R_{CS22}}{R_{CS21} + R_{CS22}} \quad \text{(eq. 14)}$$

Based on understanding of the power stage connection, the current distribution in the two phases can be calculated by

$$I_{L1} = I_{O1} - I_{Share} \quad \text{(eq. 15)}$$

and

$$I_{L2} = I_{O2} - I_{Share} \quad \text{(eq. 16)}$$

Where I_{O1} is the loading current in the power rail V_{O1}, and I_{O2} is the loading current in the power rail V_{O2}. Using of Equations 5, 6, 7, 8, 15, and 16 gives:

$$I_{FB2} = k_{IL2\_IFB2} \cdot I_{O2} - k_{IL1\_IFB2} \cdot I_{O1} + \left(k_{IL1\_IFB2} + k_{IL2\_IFB2}\right) \cdot \frac{\left(1 + \frac{R_{21}}{R_{24}}\right) \cdot V_{ref2} - \left(1 + \frac{R_{11}}{R_{14}}\right) \cdot V_{ref1} + R_{21} \cdot \left(k_{IL1\_IFB2} \cdot I_{O1} - k_{IL2\_IFB2} \cdot I_{O2}\right)}{R_{ON\_S} + R_{21} \cdot \left(k_{IL1\_IFB2} + k_{IL2\_IFB2}\right)} \qquad \text{(eq. 17)}$$

where

$$k_{IL1\_IFB2} = G_{IFB2} \cdot G_{ICS1} \cdot R_{ICS1} \cdot k_{CS1} \cdot DCR_1 = 1\text{x}10^{-3} \cdot \frac{R_{CS12}}{R_{CS11} + R_{CS12}} \cdot DCR_1 \qquad \text{(eq. 18)}$$

$$k_{IL2\_IFB2} = G_{IFB2} \cdot G_{ICS2} \cdot R_{ICS2} \cdot k_{CS2} \cdot DCR_2 = 1\text{x}10^{-3} \cdot \frac{R_{CS22}}{R_{CS21} + R_{CS22}} \cdot DCR_2 \qquad \text{(eq. 19)}$$

To maintain the output voltage V_{O2} of the phase 2 in certain regulation window in case of any fault or non−ideal conditions, such as the sharing switch is broken or has too high on resistance, the injection current I_{FB2} has magnitude limits as $\pm 9\ \mu A$. As a result, V_{O2} has a limited adjustable range as

$$\left(1 + \frac{R_{21}}{R_{24}}\right) \cdot 0.8 - 8 \cdot 10^{-6} \cdot R_{21} \le V_{O2} \le \left(1 + \frac{R_{21}}{R_{24}}\right) \cdot 0.8 + 9 \cdot 10^{-6} \cdot R_{21} \qquad \text{(eq. 20)}$$

In an Ideal case that the sharing switch has very small on resistance and the two phases matches perfectly, the current−sense input voltages in the two phases are equal, that is

$$I_{L1} \cdot DCR_1 \cdot k_{CS1} = I_{L2} \cdot DCR_2 \cdot k_{CS2} \qquad \text{(eq. 21)}$$

Using of Equations 15, 16, and 21 gives

$$I_{L1} = \frac{DCR_2 \cdot k_{CS2} \cdot \left(I_{O1} + I_{O2}\right)}{DCR_1 \cdot k_{CS1} + DCR_2 \cdot k_{CS2}} \qquad \text{(eq. 22)}$$

$$I_{L2} = \frac{DCR_1 \cdot k_{CS1} \cdot \left(I_{O1} + I_{O2}\right)}{DCR_1 \cdot k_{CS1} + DCR_2 \cdot k_{CS2}} \qquad \text{(eq. 23)}$$

$$I_{Share} = \frac{DCR_1 \cdot k_{CS1} \cdot I_{O1} - DCR_2 \cdot k_{CS2} \cdot I_{O2}}{DCR_1 \cdot k_{CS1} + DCR_2 \cdot k_{CS2}} \qquad \text{(eq. 24)}$$

PWM Operation

There are two available operation modes, which are forced PWM mode and power−saving skip mode, selected by two different voltage levels at EN pin for each channel, respectively. The operation modes can be external preset or on−line programmed.

The two channels / phases controlled by the NCP5222 share one input power rail. The both channels / phases operate at a fixed 300 kHz normal switching frequency in continuous−conduction mode (CCM). To reduce the common input ripple and capacitors, the two channels / phases operate 180° interleaved in CCM. To speed up transient response and increase system sampling rate, an internal 1.2 MHz high−frequency oscillator is employed. A digital circuitry divides down the high−frequency clock CLK_H and generates two interleaved 300 kHz clocks (CLK1 and CLK2), which are delivered to the two PWM control blocks as normal operation clocks.

Forced−PWM Operation (FPWM Mode)

If the voltage level at the EN pin is a medium level around 1.95 V, the corresponding channel of the NCP5222 works under forced−PWM mode with fixed 300 kHz switching frequency. In this mode, the low−side gate−drive signal is forced to be the complement of the high−side gate−drive signal and thus the converter always operates in CCM. This mode allows reverse inductor current, in such a way that it provides more accurate voltage regulation and fast transient response. During soft−start operation, the NCP5222 automatically runs in FPWM mode regardless of the EN pin's setting to guarantee smooth powering up.

Pulse−Skipping Operation (Skip Mode)

Skip mode is enabled by pulling EN pin higher than 2.65 V, and then the corresponding channel works in pulse−skipping enabled operation. In medium and high load range, the converter still runs in CCM, and the switching frequency is fixed to 300 kHz. If the both channels run in CCM, they operate interleaved. In light load range, the converter automatically enters diode emulation and skip mode to maintain high efficiency. The PWM on−time in discontinuous−conduction mode (DCM) is adaptively controlled to be similar to the PWM on−time in CCM.

Transient Response Enhancement (TRE)

For a conventional trailing−edge PWM controller in CCM, the minimum response delay time is one switching period in the worst case. To further improve transient response, a transient response enhancement circuitry is introduced to the NCP5222. The controller continuously monitors the COMP signal, which is the output voltage of the error amplifier, to detect load transient events. A desired stable close−loop system with the NCP5222 has a ripple voltage in the COMP signal, which peak−to−peak value is normally in a range from 200 mV to 500 mV. There is a threshold voltage in each channel made in a way that a filtered COMP signal pluses an offset voltage. Once a large load transient occurs, the COMP signal is possible to exceed the threshold and then TRE is tripped in a short period, which is typically around one normal switching cycle. In this short period, the controller runs at higher frequency and therefore has faster response. After that the controller comes back to normal operation.

Protection Funtions

The NCP5222 provides comprehensive protection functions for the power system, which include input power supply undervoltage lock out, output overcurrent protection, output overvoltage protection, output undervoltage protection, and thermal shutdown protection. The priority of the protections from high to low as: 1. Thermal protection and input power supply undervoltage lockout; 2. Output overvoltage protection; 3. Output overcurrent protection and output undervoltage protection.

Input Power Supply Undervoltage Lock Out (UVLO)

The NCP5222 provides UVLO functions for both input power supplies (V_{IN} and V_{CC}) of the power stage and controller itself. The two UVLO functions make it possible to have flexible power sequence between V_{IN} and V_{CC} for the power systems. The start threshold of V_{IN} is 3.6 V, and the starting threshold of V_{CC} is 4.25 V.

Output Overcurrent Protection (OCP)

The NCP5222 protects converter if overcurrent occurs. The current through each channel is continuously monitored with differential current sense. If inductor current exceeds the current threshold, the high−side gate drive will be turned off cycle−by−cycle. In the meanwhile, an internal OC fault timer will be triggered. If the fault still exists after about 53 μs, the corresponding channel latches off, both the high−side MOSFET and the low−side MOSFET are turned off. The fault remains set until the system has shutdown and re−applied V_{CC} and/or the enable signal EN has toggled states.

Current limit threshold V_{TH_OC} between CS+ and CS−is internally fixed to 30 mV. The current limit can be programmed by the inductor's DCR and the current−sense resistor divider with R_{CS1} and R_{CS2}. The inductor peak current limit is

$$I_{OC(Peak)} = \frac{V_{TH\_OC}}{k_{CS} \cdot DCR} \quad \text{(eq. 25)}$$

The DC current limit is

$$I_{OC} = I_{OC(Peak)} - \frac{V_O \cdot \left(V_{IN} - V_O\right)}{2 \cdot V_{IN} \cdot f_{SW} \cdot L} \quad \text{(eq. 26)}$$

where V_{IN} is input supply voltage of the power stage, and f_{SW} is 300 kHz normal switching frequency.

In the dual−channel mode, the steady−state inductor DC current is equal to output loading current I_{Omax} per channel, so that the overcurrent threshold I_{OC} is the maximum loading current I_{Omax} per channel.

$$I_{OC1} = I_{O1max} \quad \text{(eq. 27)}$$

$$I_{OC2} = I_{O2max} \quad \text{(eq. 28)}$$

In two−phase operation mode, to make sure the OCP is not triggered in the normal operation, the worst case need to be considered, in which the maximum load step in one power rail comes just after the two phases are sharing the maximum load from the other power rail. In this case, the two overcurrent thresholds need to be set as

$$I_{OC1} = I_{O1max} + \frac{DCR_2 \cdot k_{CS2}}{DCR_1 \cdot k_{CS1} + DCR_2 \cdot k_{CS2}} \quad \text{(eq. 29)}$$

and

$$I_{OC2} = I_{O2max} + \frac{DCR_1 \cdot k_{CS1}}{DCR_1 \cdot k_{CS1} + DCR_2 \cdot k_{CS2}} \quad \text{(eq. 30)}$$

The both phases also has the same internal overcurrent current−sense threshold V_{TH_OC} = 30 mV, that means

$$I_{OC1} \cdot DCR_1 \cdot k_{CS1} = I_{OC2} \cdot DCR_2 \cdot k_{CS2} = V_{TH\_OC} \quad \text{(eq. 31)}$$

Use of Equations 29, 30, and 31 leads to:

$$I_{OC1} = I_{O1max} \cdot \left(1 + \frac{I_{O2max}}{I_{O1max} + I_{O2max}}\right) \quad \text{(eq. 32)}$$

$$I_{OC2} = I_{O2max} \cdot \left(1 + \frac{I_{O1max}}{I_{O1max} + I_{O2max}}\right) \quad \text{(eq. 33)}$$

Output Overvoltage Protection (OVP)

An OVP circuit monitors the feedback voltages to prevent loads from over voltage. OVP limit is typically 115% of the nominal output voltage level, and the hysteresis of the OV detection comparator is 5% of the nominal output voltage. If the OV event lasts less than 1.5 μs, the controller remains normal operation when the output of the OV comparator is released, otherwise an OV fault is latched after 1.5 μs. After the fault is latched, the high−side MOSFET is latched off and the low−side MOSFET will be on and off responding to the output of the OV detection comparator. The fault remains set until the system has shutdown and re−applied V_{CC} and/or the enable signal EN has toggled states.

Output Undervoltage Protection (UVP)

A UVP circuit monitors the feedback voltages to detect undervoltage. UVP limit is typically 80% of the nominal output voltage level. If the output voltage is below this threshold, a UV fault is set. If an OV protection is set before, the UV fault will be masked. If no OV protection set, an internal fault timer will be triggered. If the fault still exists after about 27 μs, the corresponding channel is latches off, both the high−side MOSFET and the low−side MOSFET are turned off. The fault remains set until the system has shutdown and re−applied V_{CC} and/or the enable signal EN has toggled states.

Thermal Protection

The NCP5222 has a thermal shutdown protection to protect the device itself from overheating when the die temperature exceeds 150°C. After the thermal protection is triggered, the fault state can be ended by re−applying V_{CC} or EN when the die temperature drops down below 125°C.

Layout Guidelines

Figures 11 and 12 show exemplary layout of the power stage components for dual−channel configuration and two−phase configuration, respectively.

In the two−phase mode, after the sharing switch is turned on, the voltage difference across the sharing−switch will cause a current flow through it, which is used to balance power delivery between the two phases. The smaller $R_{DS(on)}$ of the sharing switch (R_{on_ssh}), the better the current balance and the smaller output voltage deviation in V_{O2}. Actually, the current through the sharing switch can be calculated by $I_{ssh} = (V_{O2} - V_{O1}) / R_{on\_effective}$, in which $R_{on\_effective} = R_{on\_ssh} + R_{pcb}$, and R_{pcb} is the copper resistance between the two output sensing points. So that too large R_{pcb} effectively wastes $R_{DS(on)}$ of the sharing switch, and thus reduces the power sharing capability and enlarges V_{O2} deviation.

In a real application, to make sure the CH1 has perfect voltage regulation, the V_{O1} sensing point and AGND can be designed like remote sensing. In the meantime, to fully use the sharing switch for the current sharing operation and reduce V_{O2} deviation, the distance between the two sensing points V_{O1} and V_{O2} should be arranged to be as close as possible.

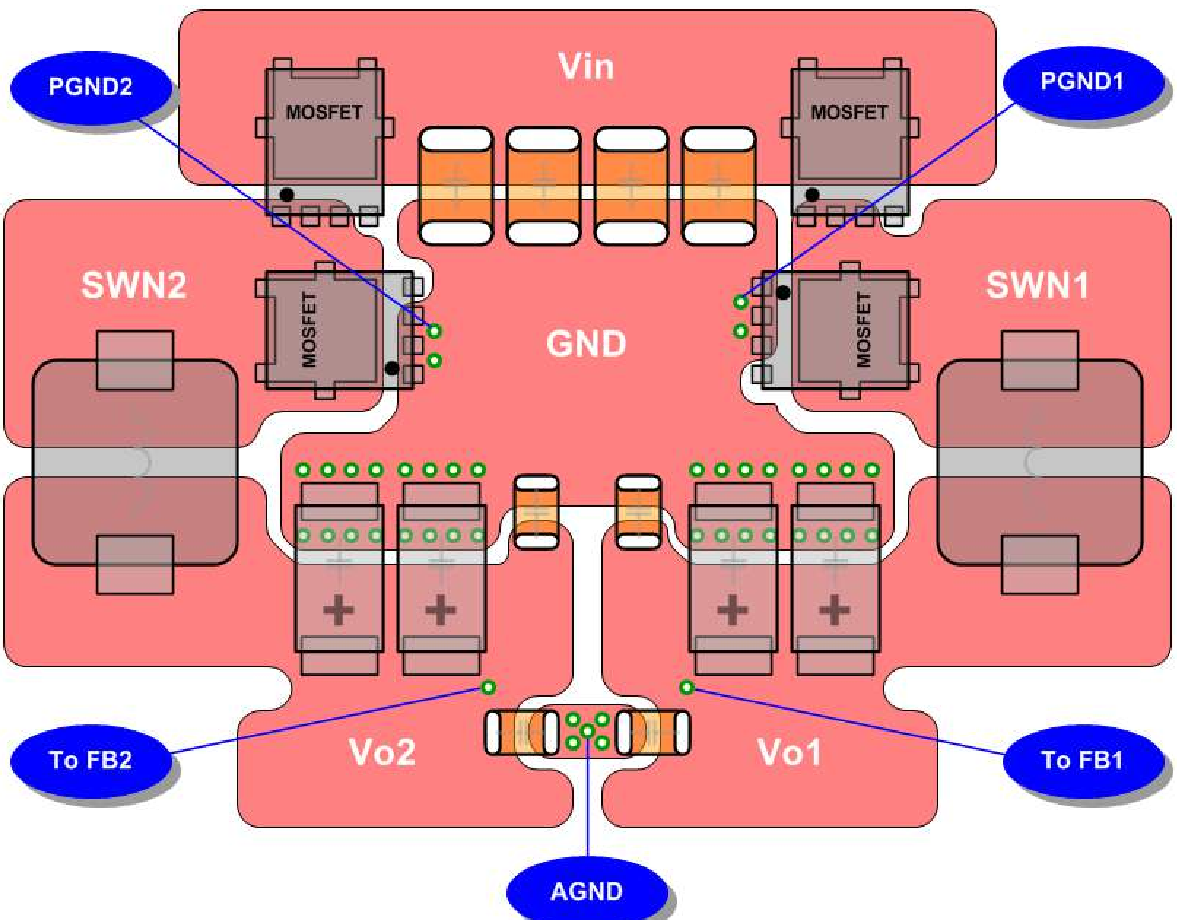


Figure 11. Layout Guidelines in Dual−Channel Mode

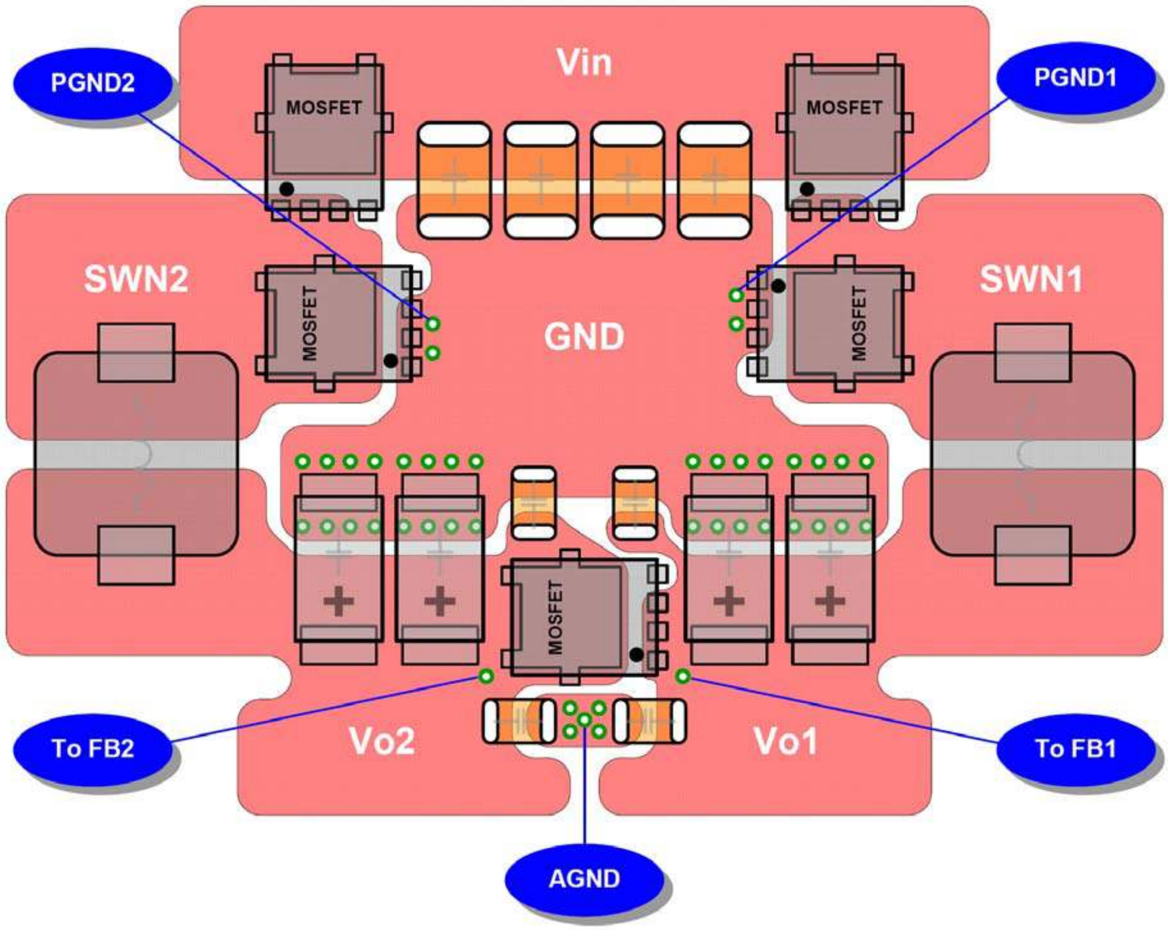


Figure 12. Layout Guidelines in Two−Phase Mode

TYPICAL OPERATING CHARACTERISTICS

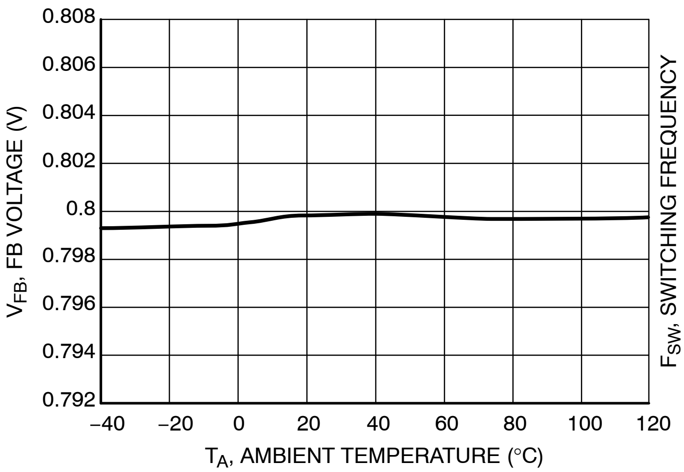


Figure 13. Reference Voltage V_{FB} vs. Ambient Temperature

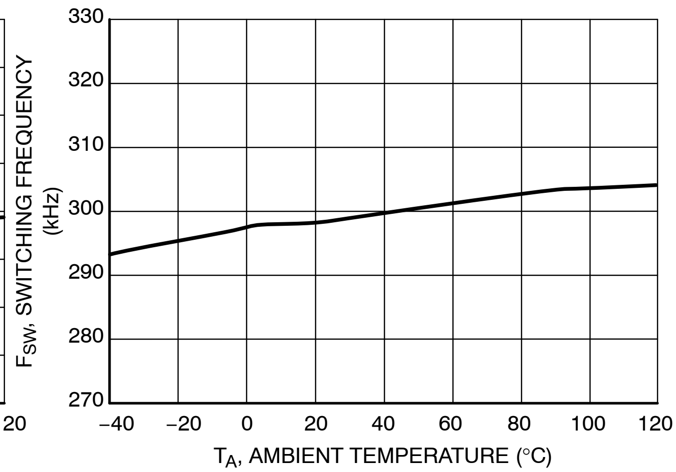


Figure 14. Switching Frequency vs. Ambient Temperature

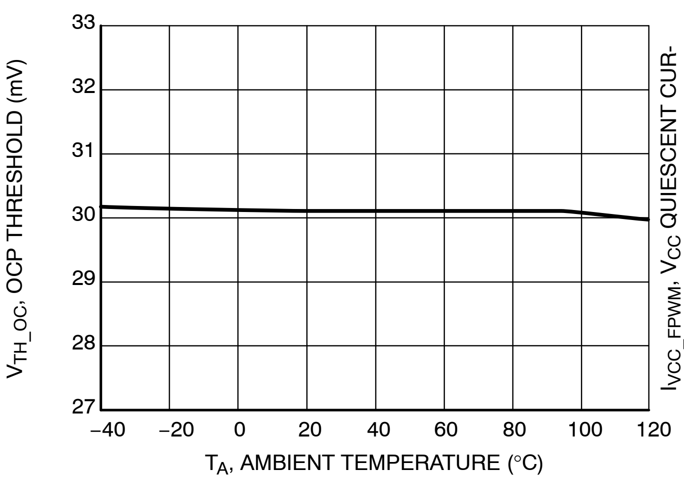


Figure 15. OCP Threshold vs. Ambient Temperature

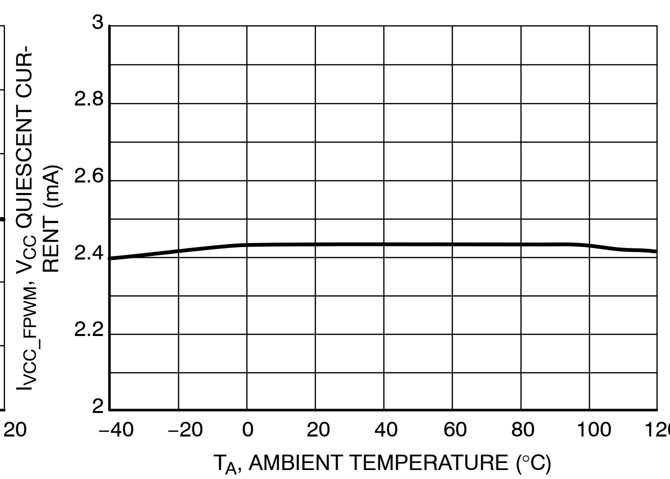


Figure 16. V_{CC} Quiescent Current vs. Ambient Temperature in FPWM Mode

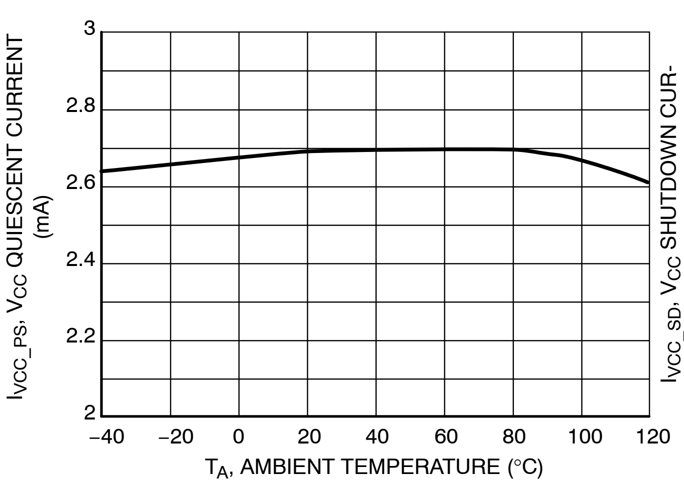


Figure 17. V_{CC} Quiescent Current vs. Ambient Temperature in Skip Mode

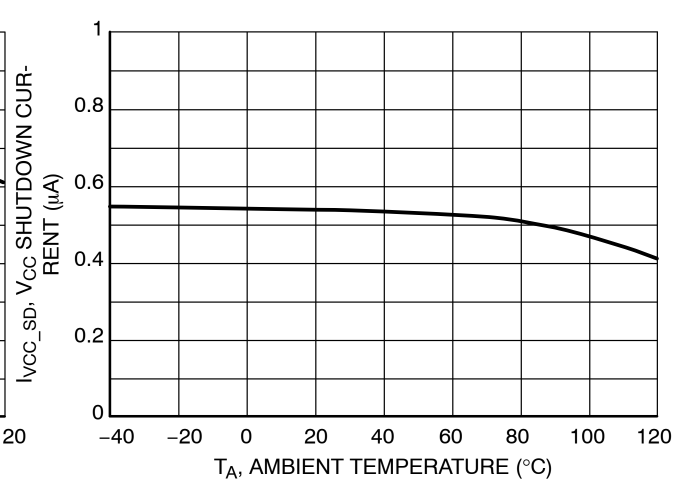


Figure 18. V_{CC} Shutdown Current vs. Ambient Temperature

TYPICAL OPERATING CHARACTERISTICS

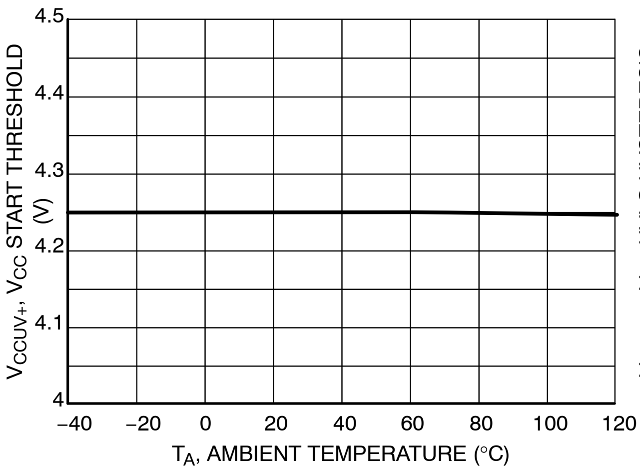


Figure 19. V_{CC} Start Threshold VCCUV+ vs. Ambient Temperature

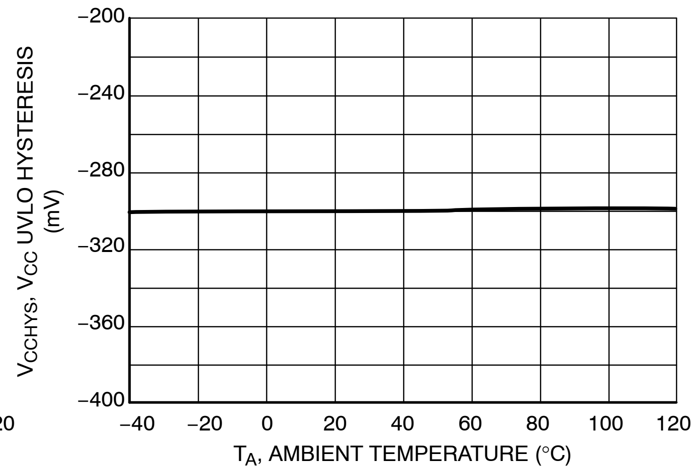


Figure 20. V_{CC} UVLO Hysteresis VCCHYS vs. Ambient Temperature

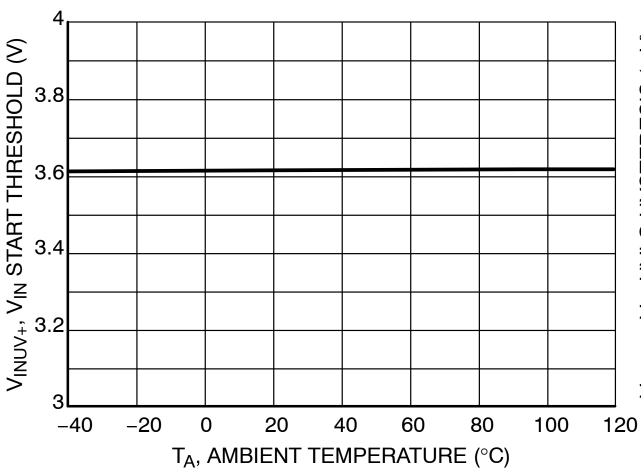


Figure 21. V_{IN} Start Threshold VINUV+ vs. Ambient Temperature

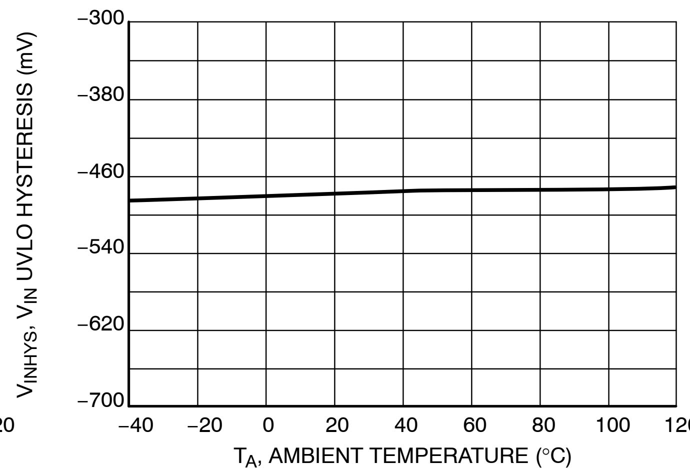


Figure 22. V_{IN} UVLO Hysteresis VINHYS vs. Ambient Temperature

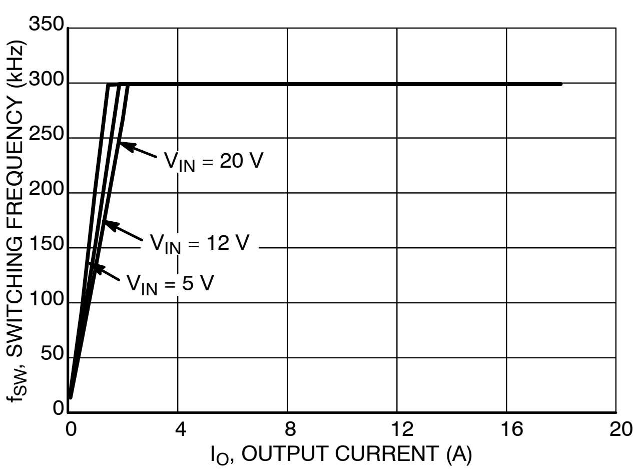


Figure 23. Switching Frequency vs. Output Current in Skip Mode

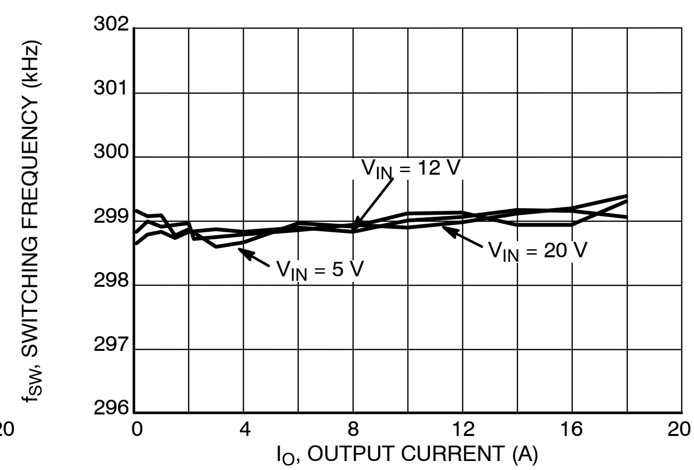


Figure 24. Switching Frequency vs. Output Current in FPWM Mode

TYPICAL OPERATING CHARACTERISTICS

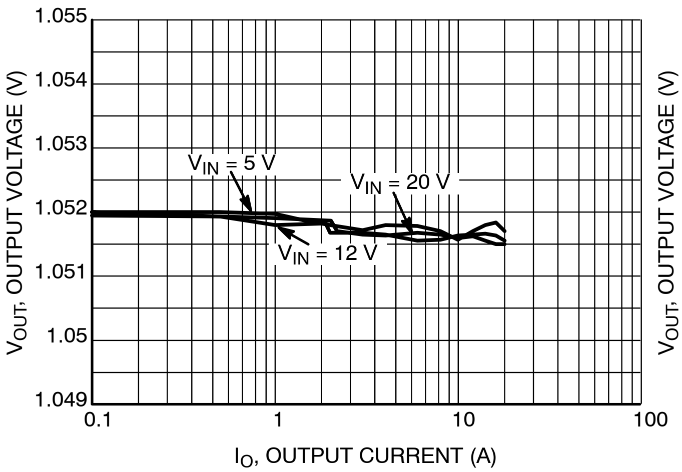


Figure 25. Output Voltage vs. Output Current in Skip Mode

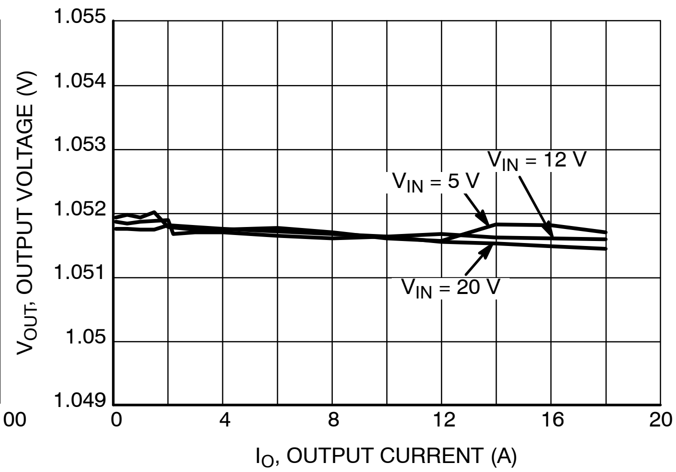


Figure 26. Output Voltage vs. Output Current in FPWM Mode

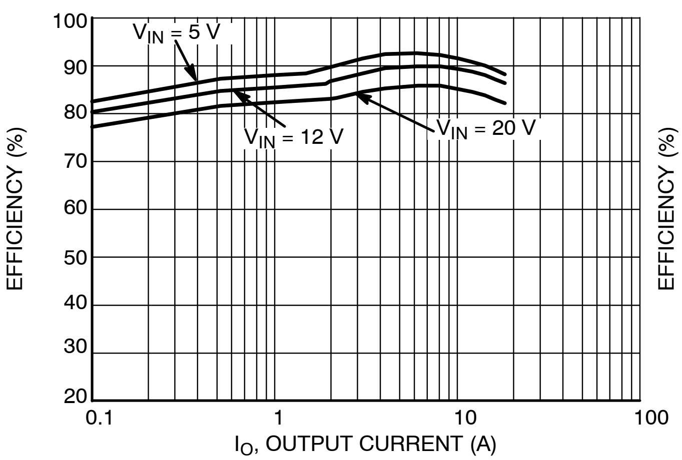


Figure 27. Efficiency vs. Output Current in Skip Mode

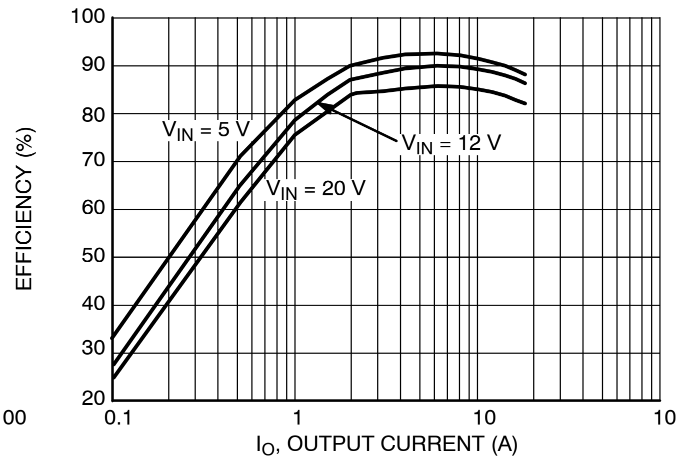


Figure 28. Efficiency vs. Output Current in FPWM Mode

TYPICAL OPERATING CHARACTERISTICS

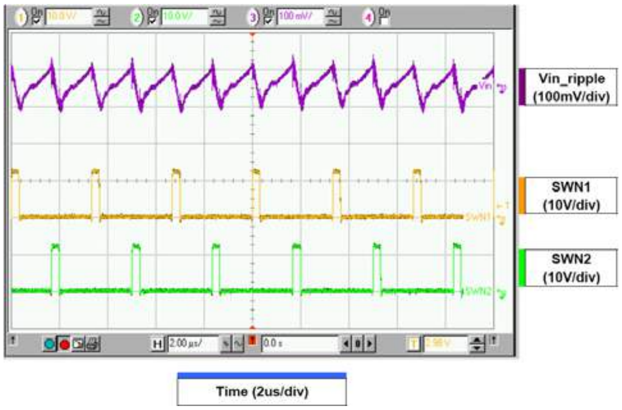


Figure 29. Input Voltage Ripple (V_{IN} = 12 V, C_{IN} = 10 μF * 4, V_{O1} = 1.05 V, I_{O1} = 10 A, L1 = 0.56 μH, C_{O1} = 470 μF * 2, V_{O2} = 1.05 V, I_{O2} = 10 A, L2 = 0.56 μH, C_{O2} = 470 μF * 2, Dual−Channel Operation)

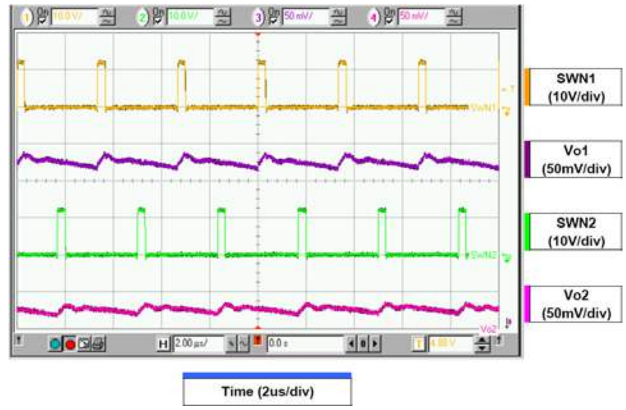


Figure 30. Output Voltage Ripple (V_{IN} = 12 V, V_{O1} = 1.05 V, I_{O1} = 10 A, L1 = 0.56 μH, C_{O1} = 470 μF * 2, V_{O2} = 1.05 V, I_{O2} = 10 A, L2 = 0.56 μH, C_{O2} = 470 μF * 2, Dual−Channel Operation)

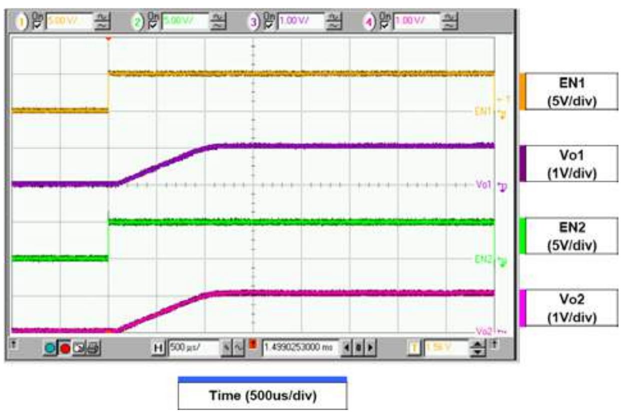


Figure 31. Powerup with Two ENs Together (V_{IN} = 12 V, V_{O1} = 1.05 V, I_{O1} = 0 A, V_{O2} = 1.05 V, I_{O2} = 0 A, Dual−Channel Operation)

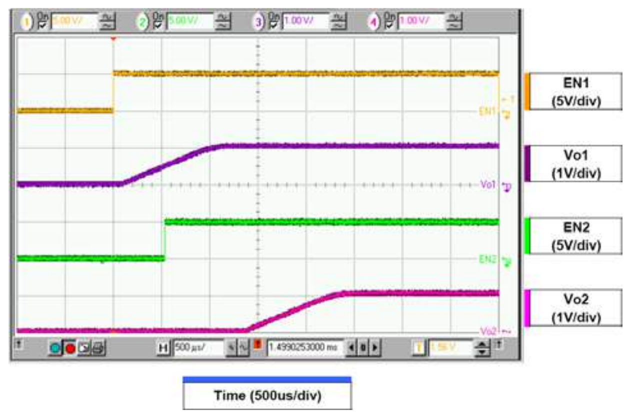


Figure 32. Powerup with EN2 Comes before CH1 Completes Soft−Start (V_{IN} = 12 V, V_{O1} = 1.05 V, I_{O1} = 0 A, V_{O1} = 1.05 V, I_{O2} = 0 A, Dual−Channel Operation)

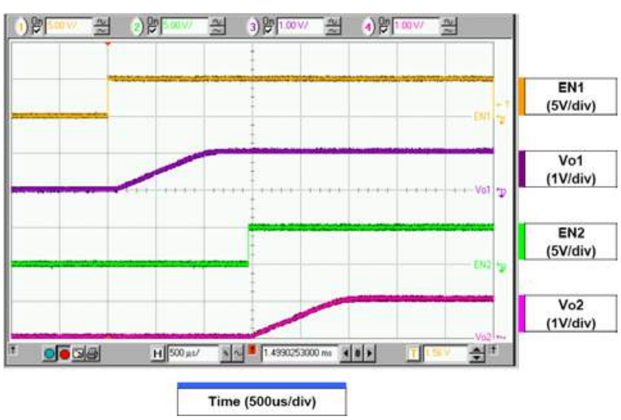


Figure 33. Powerup with EN2 Comes after CH1 Completes Soft−Start (V_{IN} = 12 V, V_{O1} = 1.05 V, I_{O1} = 0 A, V_{O2} = 1.05 V, I_{O2} = 0 A, Dual−Channel Operation)

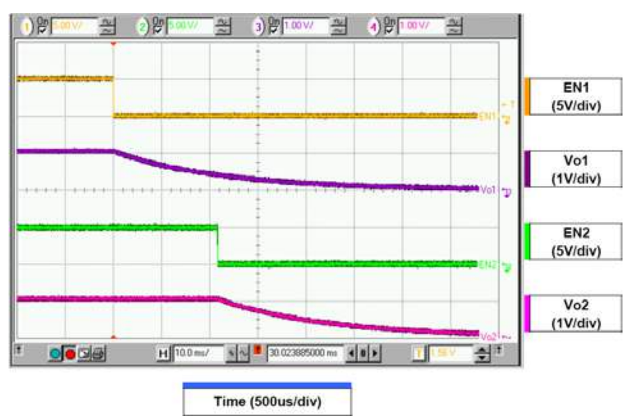


Figure 34. Powerdown and Soft−Stop (V_{IN} = 12 V, V_{O1} = 1.05 V, I_{O1} = 0 A, V_{O2} = 1.05 V, I_{O2} = 0 A, Dual−Channel Operation)

TYPICAL OPERATING CHARACTERISTICS

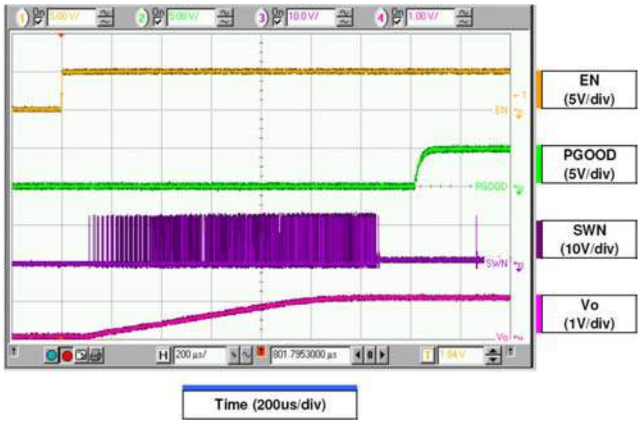


Figure 35. Powerup Operation without Biased Output (V_{IN} = 12 V, V_O = 1.05 V, I_O = 0 A, Skip Mode)

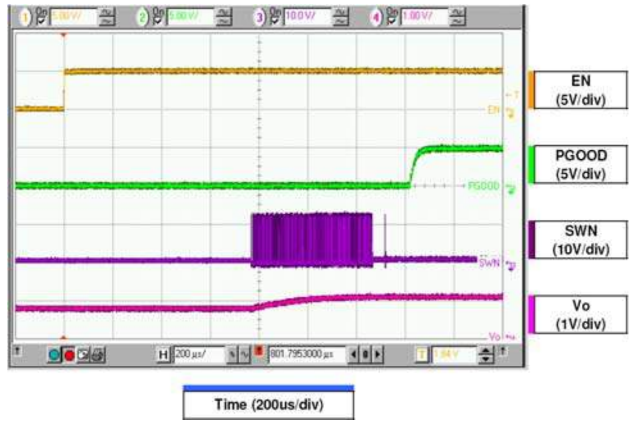


Figure 36. Powerup Operation with Biased Output (V_{IN} = 12 V, V_O = 1.05 V, I_O = 0 A, Skip Mode)

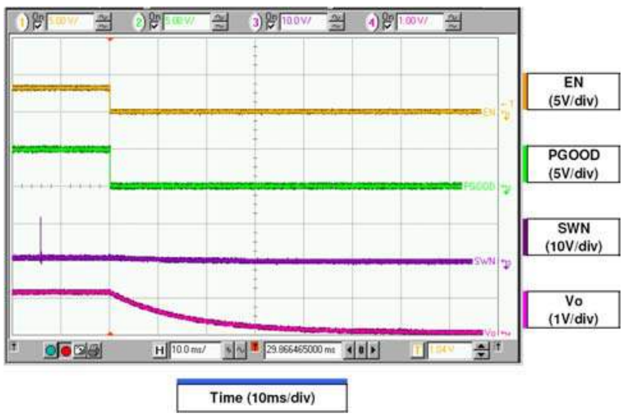


Figure 37. Power−Down Operation (V_{IN} = 12 V, V_O = 1.05 V, I_O = 0 A, Skip Mode)

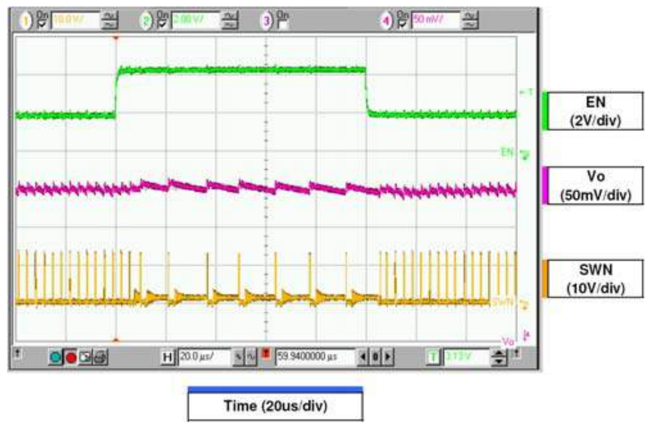


Figure 38. On−Line Mode Transition (V_{IN} = 12 V, V_O = 1.05 V, I_O = 0.5 A, FPWM − Skip − FPWM Mode)

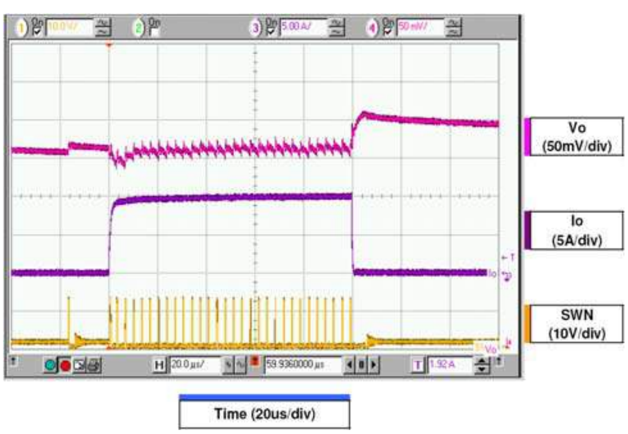


Figure 39. Load Transient Response in Skip Mode (V_{IN} = 12 V, V_O = 1.05 V, I_O = 0.1 A to 10 A to 0.1 A, L = 0.56 μH, C_O = 470 μF * 2)

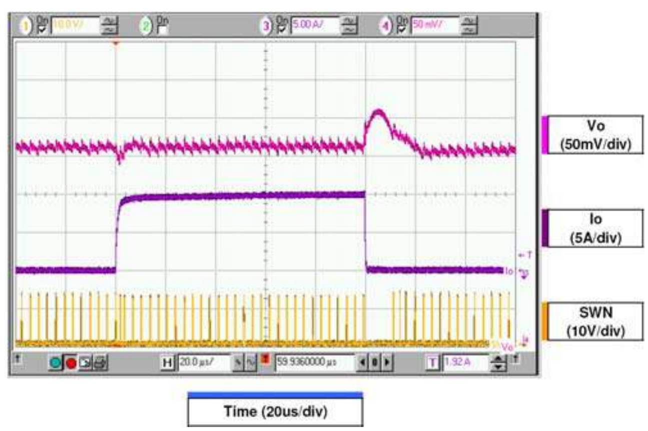


Figure 40. Load Transient Response in FPWM Mode (V_{IN} = 12 V, V_O = 1.05 V, I_O = 0.1 A to 10 A to 0.1 A, L = 0.56 μH, C_O = 470 μF * 2)

TYPICAL OPERATING CHARACTERISTICS

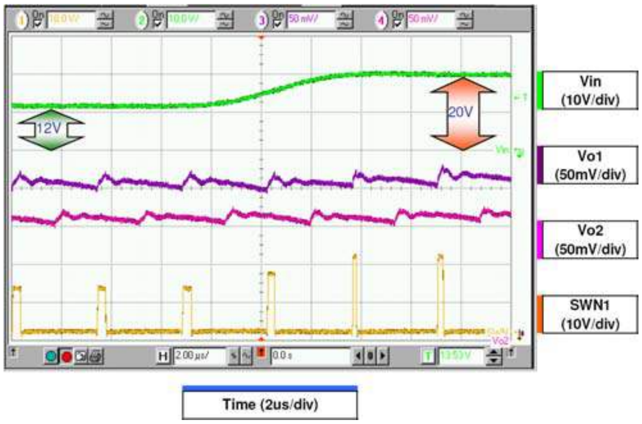


Figure 41. Line Transient Response (V_{IN} = 12 V to 20 V, V_{O1} = 1.05 V, I_{O1} = 9 A, L1 = 0.56 μH, C_{O1} = 470 μF * 2, V_{O2} = 1.05 V, I_{O2} = 9 A, L2 = 0.56 μH, C_{O2} = 470 μF * 2, Dual−Channel Mode)

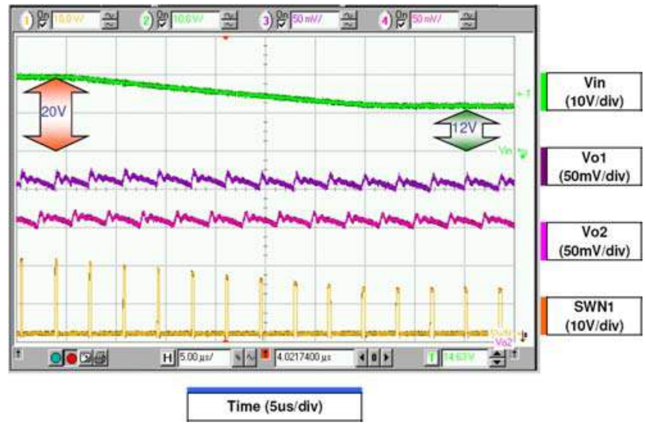


Figure 42. Line Transient Response (V_{IN} = 20 V to 12 V, V_{O1} = 1.05 V, I_{O1} = 9 A, L1 = 0.56 μH, C_{O1} = 470 μF * 2, V_{O2} = 1.05 V, I_{O2} = 9 A, L2 = 0.56 μH, C_{O2} = 470 μF * 2, Dual−Channel Mode)

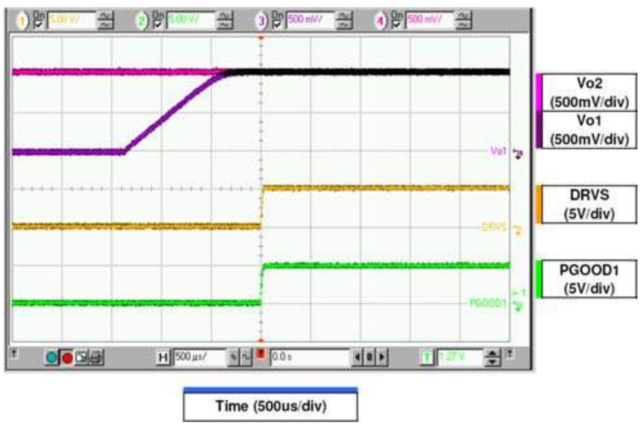


Figure 43. Powerup with EN1 in Two−Phase Mode (V_{IN} = 12 V, V_{O1} = 1.05 V, I_{O1} = 0 A, V_{O2} = 1.05 V, I_{O2} = 0 A)

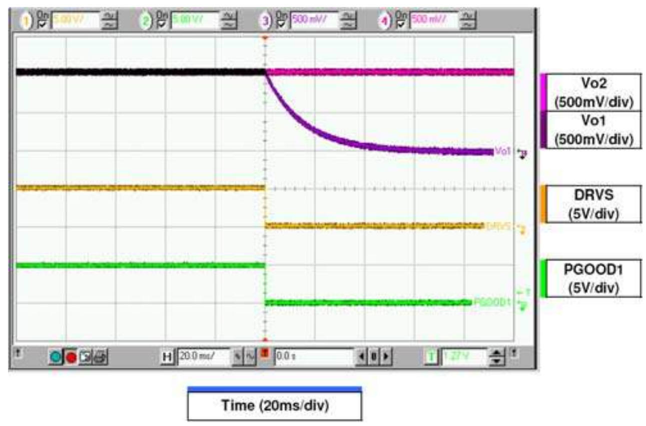


Figure 44. Powerdown with EN1 in Two−Phase Mode (V_{IN} = 12 V, V_{O1} = 1.05 V, I_{O1} = 0 A, V_{O2} = 1.05 V, I_{O2} = 0 A)

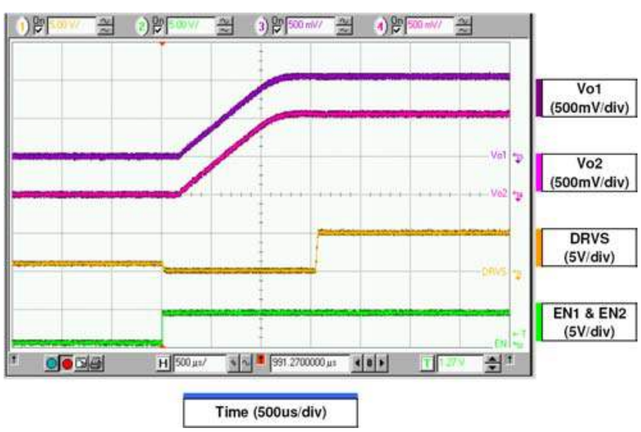


Figure 45. Powerup with Two ENs together in Two−Phase Mode (V_{IN} = 12 V, V_{O1} = 1.05 V, I_{O1} = 0 A, V_{O2} = 1.05 V, I_{O2} = 0 A)

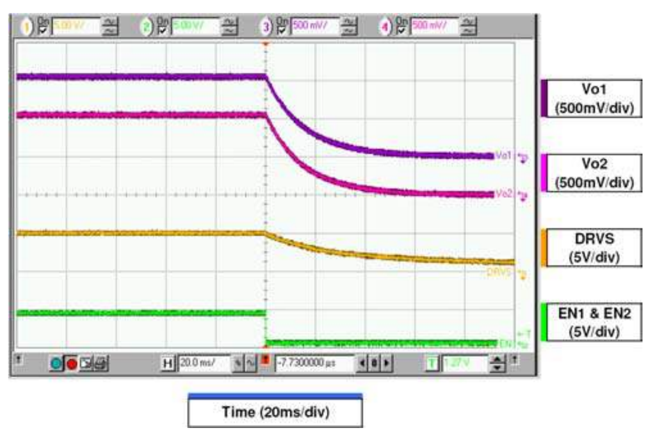


Figure 46. Powerdown with Two ENs together in Two−Phase Mode (V_{IN} = 12 V, V_{O1} = 1.05 V, I_{O1} = 0 A, V_{O2} = 1.05 V, I_{O2} = 0 A)

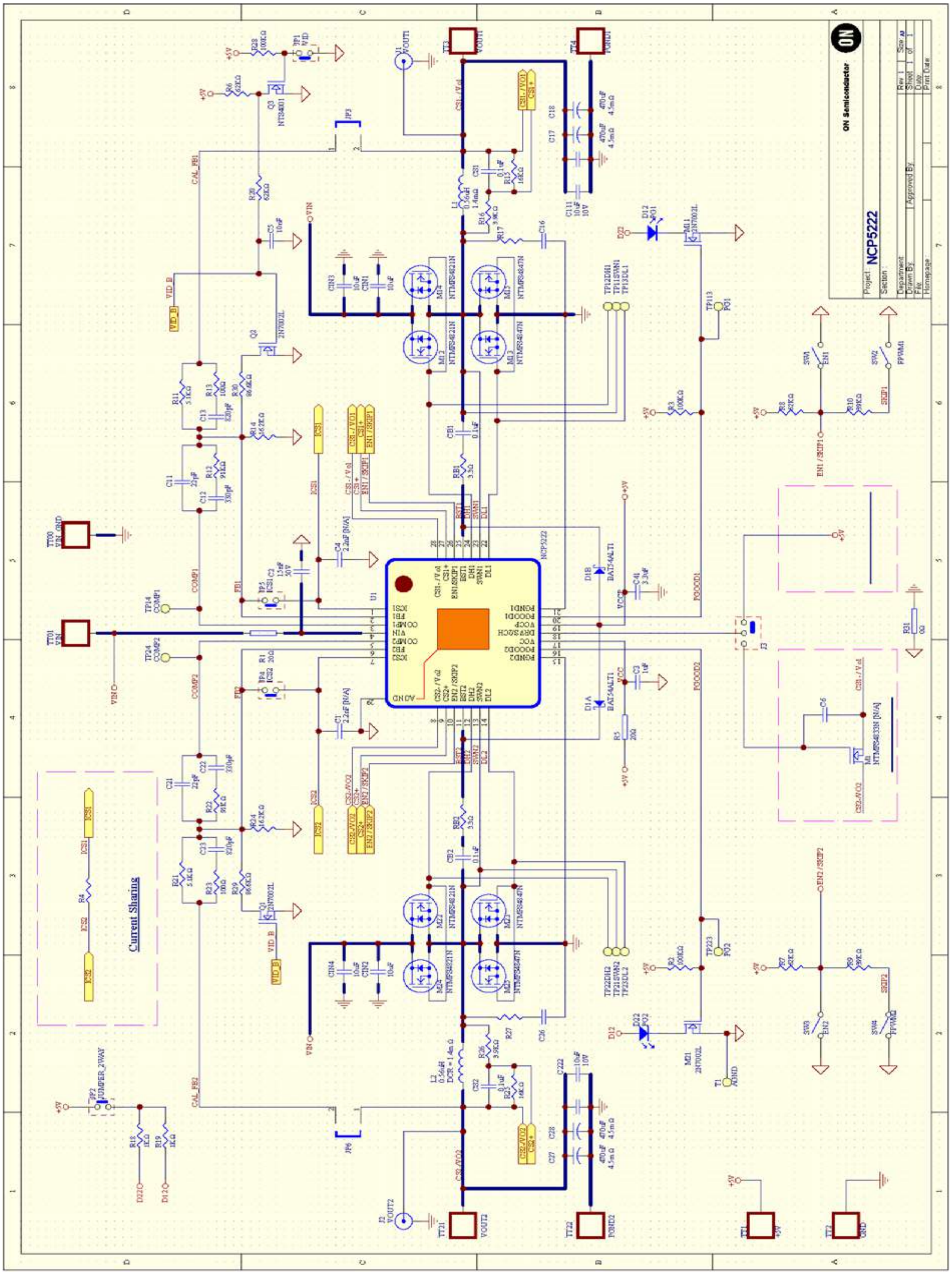


Figure 47. Schematic of Evaluation Board

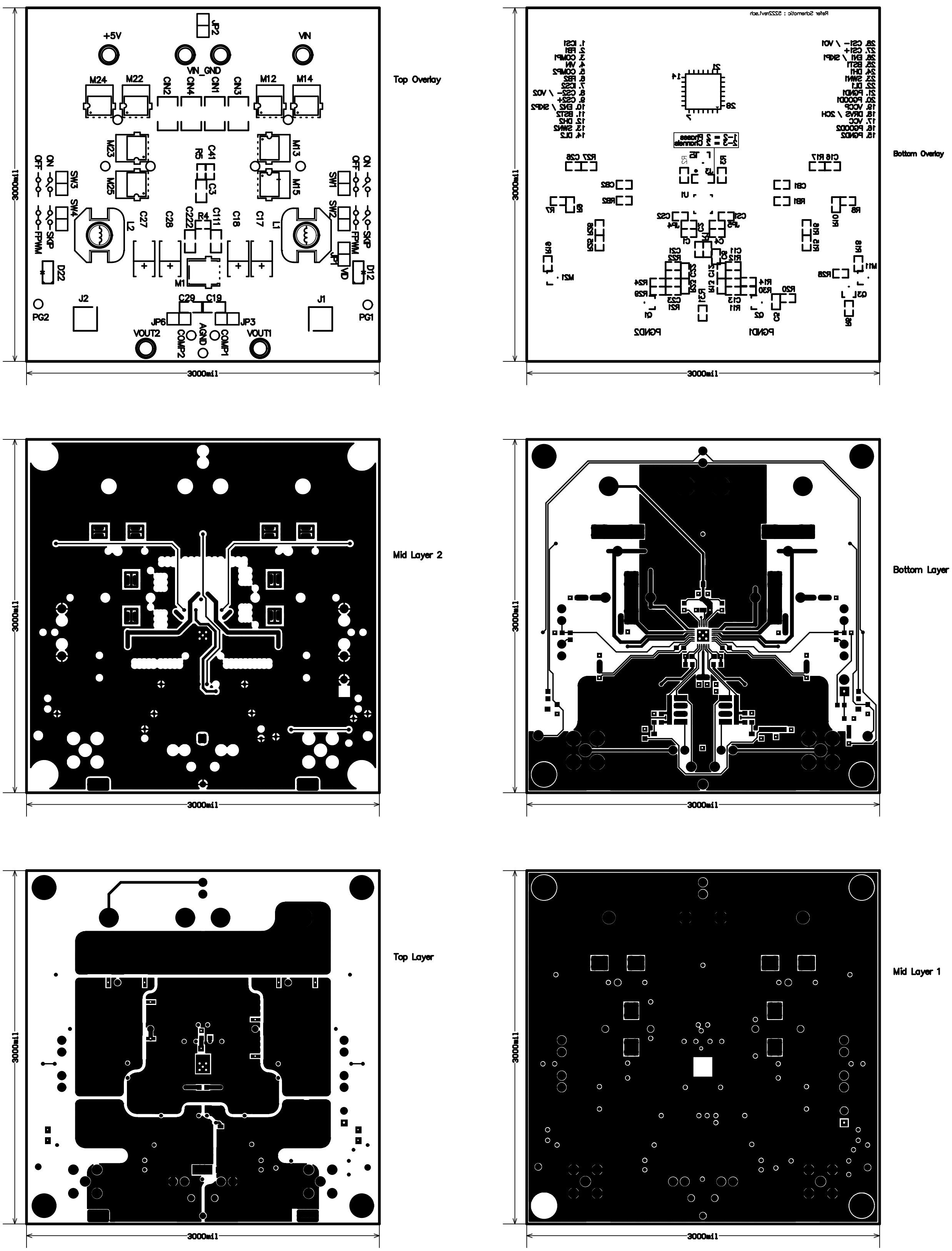


Figure 48. Layout of Evaluation Board

BILL OF MATERIALS FOR EVALUATION BOARD

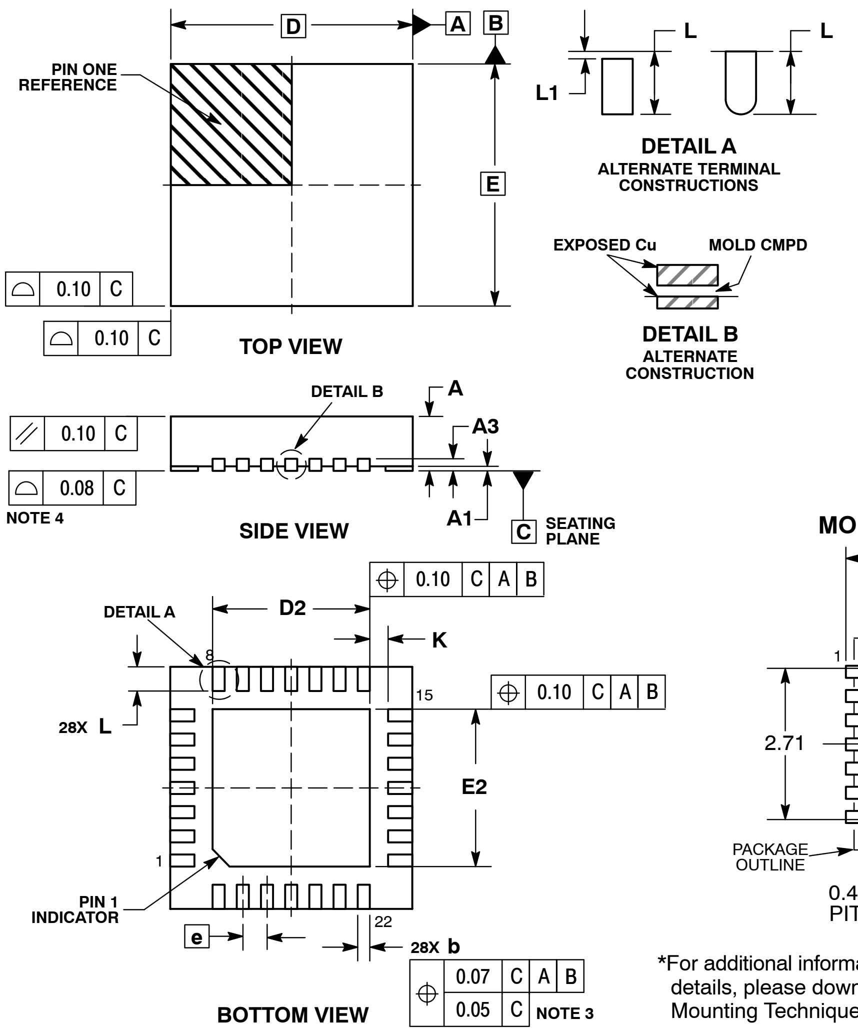
Item	Part Reference	Description	Package	Part Number	Manufacturer	Qty
1	U1	Dual−Channel / Two−Phase Synchronous Buck Controller	QFN28 (4x4 mm)	NCP5222MNR2G	ON Semiconductor	1
2	M11 M21 Q1 Q2	Small Signal MOSFET 60 V, 115 mA, N−Channel	SOT−23	2N7002LT1G	ON Semiconductor	4
3	Q3	Small Signal MOSFET 30 V, 270 mA, N−Channel	SC−70	NTS4001NT1G	ON Semiconductor	1
4	M12 M14 M22 M24	Power MOSFET 30 V, 58.5 A, Single N−Channel	SO−8 Flat Lead	NTMFS4821NT1G	ON Semiconductor	4
5	M13 M15 M23 M25	Power MOSFET 30 V, 85 A, Single N−Channel	SO−8 Flat Lead	NTMFS4847NT1G	ON Semiconductor	4
6	M1	Power MOSFET 30 V, 191 A, Single N−Channel	SO−8 Flat Lead	NTMFS4833NT1G	ON Semiconductor	0
7	D1	Schottky Diode, dual, common anode, 30 V	SOT−23	BAT54ALT1G	ON Semiconductor	1
8	D12 D22	LED, SMT, 2 mm, GRN	0805	L−0170GCT	PARA Light	2
9	C11 C21	MLCC Cap 50 V, 22 pF, ±5%, Char: COG	0603	C1608C0G1H220J	TDK	2
10	C12 C22	MLCC Cap 50 V, 330 pF, ±5%, Char: COG	0603	C1608C0G1H331J	TDK	2
11	C13 C23	MLCC Cap 50 V, 820 pF, ±5%, Char: COG	0603	C1608C0G1H821J	TDK	2
12	C1 C4	MLCC Cap 50 V, 2.2 nF, ±5%, Char: COG	0603	C1608C0G1H222J	TDK	0
13	C5	MLCC Cap 50 V, 10 nF, ±5%, Char: COG	0603	C1608C0G1H103J	TDK	1
14	C2	MLCC Cap 50 V, 15 nF, ±10%, Char: X7R	0603	C1608X7R1H153K	TDK	1
15	CB1 CB2 CS1 CS2	MLCC Cap 50 V, 0.1 μF, ±10%, Char: X7R	0603	C1608X7R1H104K	TDK	4
16	C3	MLCC Cap 16 V, 1 μF, ±10%, Char: X5R	0805	C2012X7R1C105K	TDK	1
17	C41	MLCC Cap 6.3 V, 3.3 μF, ±10%, Char: X5R	0603	C1608JB0J335KT	TDK	1
18	C6 C16 C26		0603			0
19	C111 C222	MLCC Cap 6.3 V, 10 μF, ±10%, Char: X5R	0805	ECJ2FB0J106M	Panasonic	2
20	CIN1 CIN2 CIN3 CIN4	MLCC Cap 25V, 10 μF, ±20%, Char: X5R	1812	C4532X7R1E106M	TDK	4
21	C17 C18 C27 C28	SP−Capacitors, 2 V, 470 μF, ESR = 4.5 mΩ	7.3mm x 4.3mm	EEFSX0D471XR	Panasonic	4
22	RB1 RB2	Thick Film Chip Resistors, 3.3 Ω, ±1%, 0.1 W	0603	ERJ3BSF3R3V	Panasonic	2
23	R1 R5	Thick Film Chip Resistors, 20 Ω, ±1%, 0.1 W	0603	ERJ3EKF20R0V	Panasonic	2
24	R13 R23	Thick Film Chip Resistors, 100 Ω, ±1%, 0.1 W	0603	ERJ3EKF1000V	Panasonic	2
25	R18 R19	Thick Film Chip Resistors, 1 kΩ, ±1%, 0.1 W	0603	ERJ3EKF1001V	Panasonic	2
26	R16 R26	Thick Film Chip Resistors, 3.9 kΩ, ±1%, 0.1 W	0603	ERJ3EKF3901V	Panasonic	2

BILL OF MATERIALS FOR EVALUATION BOARD

Item	Part Reference	Description	Package	Part Number	Manufacturer	Qty
27	R11 R21	Thick Film Chip Resistors, 5.1 kΩ, ±1%, 0.1 W	0603	ERJ3EKF5101V	Panasonic	2
28	R15 R25	Thick Film Chip Resistors, 16 kΩ, ±1%, 0.1 W	0603	ERJ3EKF1602V	Panasonic	2
29	R14 R24	Thick Film Chip Resistors, 16.2 kΩ, ±1%, 0.1 W	0603	PCF0603R 16K2BI	WELWTN	2
30	R9 R10	Thick Film Chip Resistors, 39 kΩ, ±1%, 0.1 W	0603	ERJ3EKF3902V	Panasonic	2
31	R6 R7 R8 R20	Thick Film Chip Resistors, 62 kΩ, ±1%, 0.1 W	0603	ERJ3EKF6202V	Panasonic	4
32	R12 R22	Thick Film Chip Resistors, 91 kΩ, ±1%, 0.1 W	0603	ERJ3EKF9102V	Panasonic	2
33	R29 R30	Thick Film Chip Resistors, 86.6 kΩ, ±1%, 0.1 W	0603	PCF0603R 86K6BI	WELWTN	2
34	R2 R3 R28	Thick Film Chip Resistors, 100 kΩ, ±1%, 0.1 W	0603	ERJ3EKF1003V	Panasonic	3
35	R4 R17 R27		0603			0
36	L1 L2	Power Choke 0.56 μH, DCRtyp=1.4 mΩ, ISAT = 22.9 A	11.2mm x 10.0mm	FDU1040D−R56M	TOKO	2
37	TT1, TT2, TT3, TT4, TT00, TT01, TT21, TT22	PCB Terminal	7.54mm, f = 3.18 mm	H−2121	HARWIN	8
38	TP11 TP12 TP13 TP14, TP21 TP22 TP23 TP24, JP1 JP2 JP4 JP5, T3 T4 T5 T6 J3	THT Header Pitch = 2.54 mm; Height = 12 mm		547−3302	RS Components	17
39	J1 J2	SMB−Connectors, Impedance = 50 W		295−5665	RS Components	2
40	SW1 SW2 SW3 SW4				NKK	4

PACKAGE DIMENSIONS

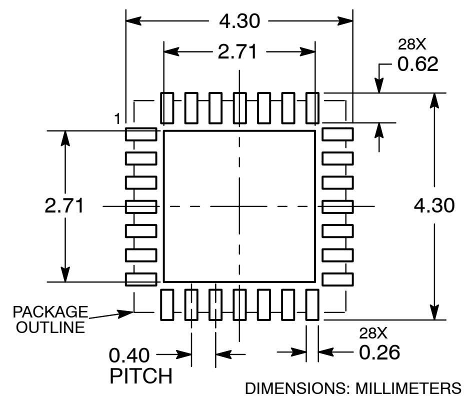
QFN28 4x4, 0.4P
CASE 485AR−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.15	0.25
D	4.00 BSC	
D2	2.50	2.70
E	4.00 BSC	
E2	2.50	2.70
e	0.40 BSC	
K	0.30 REF	
L	0.30	0.50
L1	---	0.15

RECOMMENDED MOUNTING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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