

# SN54LVT16952, SN74LVT16952

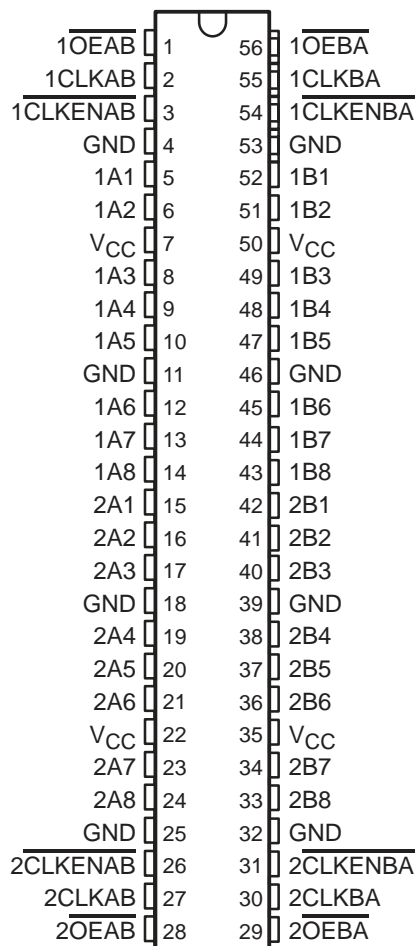
## 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS

### WITH 3-STATE OUTPUTS

SCBS151D – MAY 1992 – REVISED AUGUST 1996

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments *Widebus*™ Family
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Support Unregulated Battery Operation Down to 2.7 V
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200$  pF,  $R = 0$ )
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVT16952 . . . WD PACKAGE  
SN74LVT16952 . . . DGG OR DL PACKAGE  
(TOP VIEW)



### description

The 'LVT16952 are 16-bit registered transceivers designed for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable ( $\overline{\text{CLKENAB}}$  or  $\overline{\text{CLKENBA}}$ ) input is low. Taking the output-enable ( $\overline{\text{OEAB}}$  or  $\overline{\text{OEBA}}$ ) input low accesses the data on either port.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down,  $\overline{\text{OE}}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT16952 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.



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 **TEXAS  
INSTRUMENTS**

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# SN54LVT16952, SN74LVT16952

## 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS

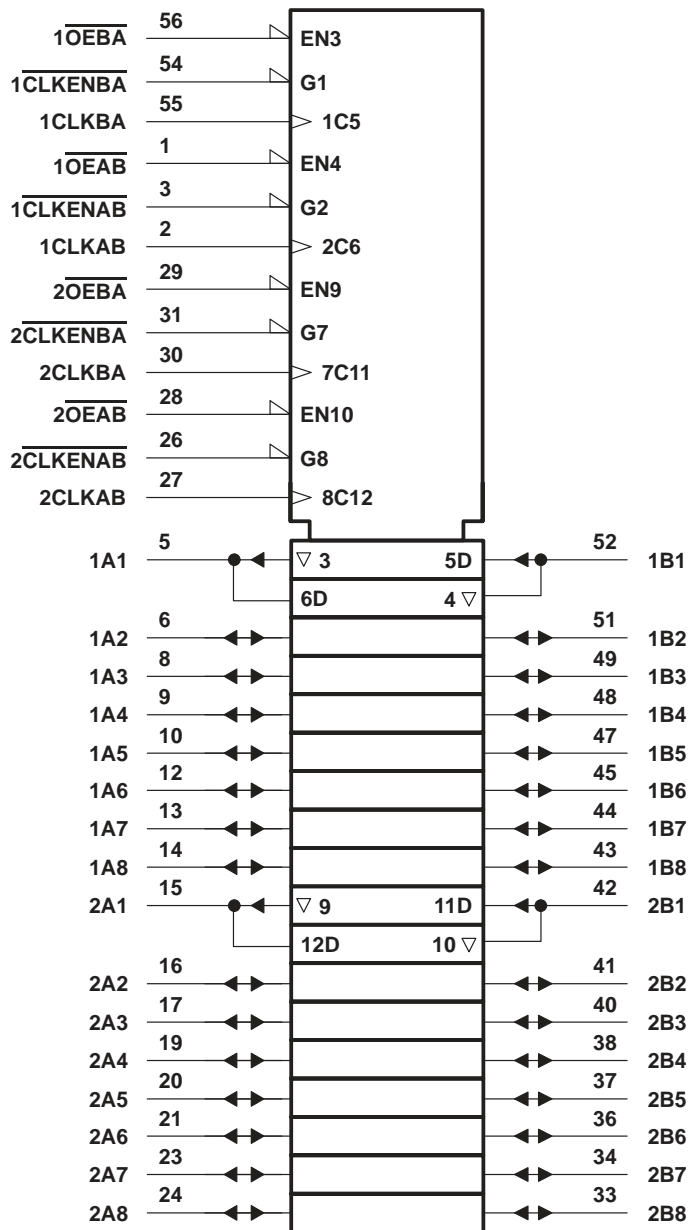
### WITH 3-STATE OUTPUTS

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#### description (continued)

The SN54LVT16952 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .  
 The SN74LVT16952 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

#### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# SN54LVT16952, SN74LVT16952 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

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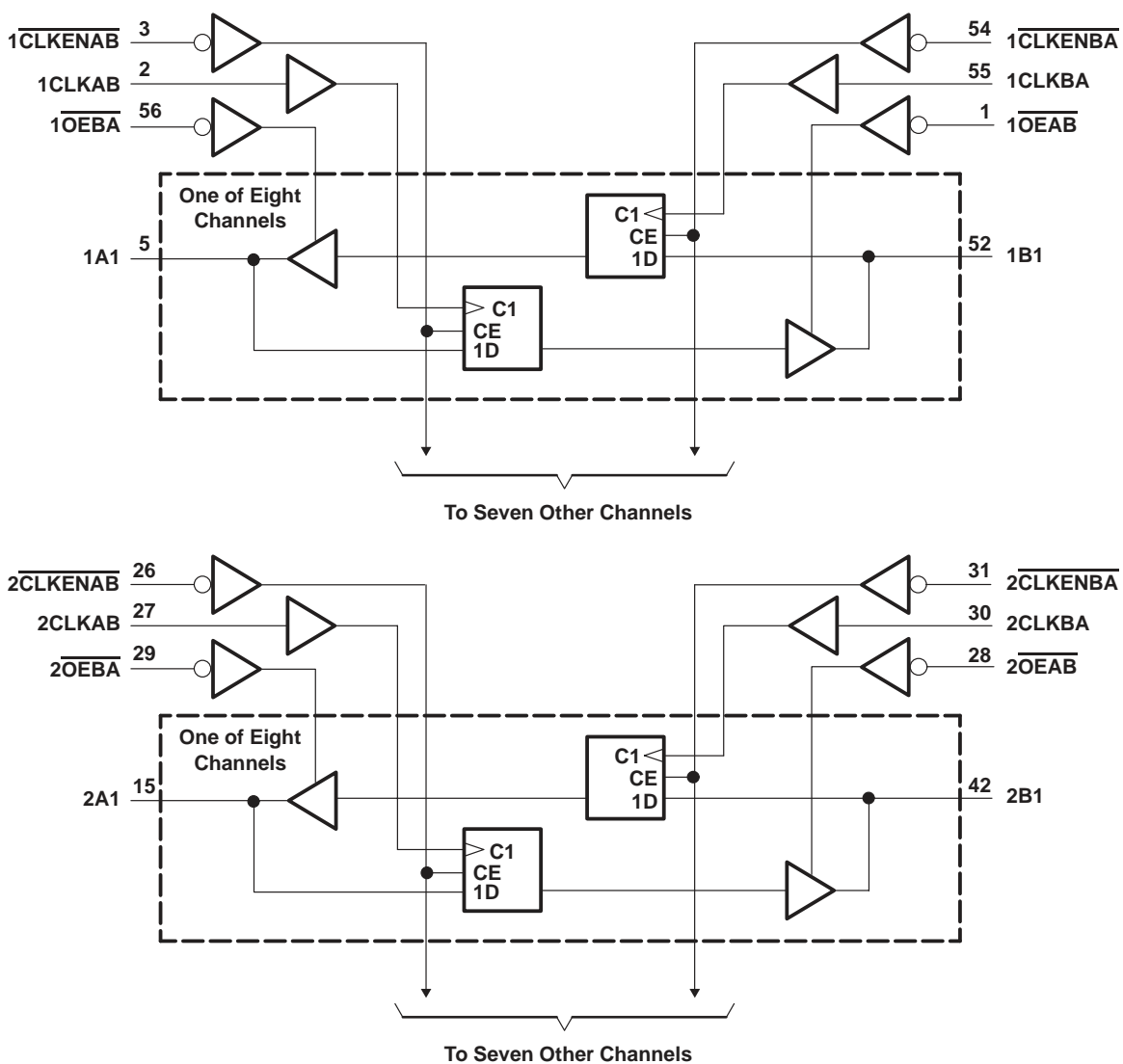
FUNCTION TABLE†

INPUTS				OUTPUT B
$\overline{\text{CLKENAB}}$	CLKAB	$\overline{\text{OEAB}}$	A	
H	X	L	X	$B_0^\ddagger$
X	L	L	X	$B_0^\ddagger$
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses  $\overline{\text{CLKENBA}}$ , CLKBA, and  $\overline{\text{OEBA}}$ .

‡ Level of B before the indicated steady-state input conditions were established

## logic diagram (positive logic)



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## 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS

### WITH 3-STATE OUTPUTS

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$ (see Note 1) ....	-0.5 V to 7 V
Current into any output in the low state, $I_O$ : SN54LVT16952 .....	96 mA
SN74LVT16952 .....	128 mA
Current into any output in the high state, $I_O$ (see Note 2): SN54LVT16952 .....	48 mA
SN74LVT16952 .....	64 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DGG package .....	1 W
DL package .....	1.4 W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .  
 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

#### recommended operating conditions (see Note 4)

		SN54LVT16952		SN74LVT16952		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2.7	3.6	2.7	3.6	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage		5.5		5.5	V
$I_{OH}$	High-level output current		-24		-32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$T_A$	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

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## 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS

### WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT16952		SN74LVT16952		UNIT	
			MIN	TYP†	MAX	MIN		TYP†
$V_{IK}$	$V_{CC} = 2.7\text{ V}$ , $I_I = -18\text{ mA}$		-1.2		-1.2		V	
$V_{OH}$	$V_{CC} = \text{MIN to MAX}^\ddagger$ , $I_{OH} = -100\ \mu\text{A}$		$V_{CC}-0.2$		$V_{CC}-0.2$		V	
	$V_{CC} = 2.7\text{ V}$ ,	$I_{OH} = -8\text{ mA}$	2.4		2.4			
	$V_{CC} = 3\text{ V}$	$I_{OH} = -24\text{ mA}$	2					
$I_{OH} = -32\text{ mA}$				2				
$V_{OL}$	$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\ \mu\text{A}$	0.2		0.2		V	
		$I_{OL} = 24\text{ mA}$	0.5		0.5			
	$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$	0.4		0.4			
		$I_{OL} = 32\text{ mA}$	0.5		0.5			
		$I_{OL} = 48\text{ mA}$	0.55					
		$I_{OL} = 64\text{ mA}$			0.55			
$I_I$	$V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}$ or GND		Control inputs		$\pm 1$		$\mu\text{A}$	
	$V_{CC} = 0$ or $\text{MAX}^\ddagger$ , $V_I = 5.5\text{ V}$		A or B ports $^\S$		10			
	$V_{CC} = 3.6\text{ V}$	$V_I = 5.5\text{ V}$		100		20		
		$V_I = V_{CC}$		1		1		
		$V_I = 0$		-5		-5		
$I_{off}$	$V_{CC} = 0$ , $V_I$ or $V_O = 0$ to $4.5\text{ V}$				$\pm 100$		$\mu\text{A}$	
$I_I(\text{hold})$	$V_{CC} = 3\text{ V}$	$V_I = 0.8\text{ V}$	A or B ports		75		$\mu\text{A}$	
		$V_I = 2\text{ V}$			-75			
$I_{OZH}$	$V_{CC} = 3.6\text{ V}$ , $V_O = 3\text{ V}$		1		1		$\mu\text{A}$	
$I_{OZL}$	$V_{CC} = 3.6\text{ V}$ , $V_O = 0.5\text{ V}$		-1		-1		$\mu\text{A}$	
$I_{CC}$	$V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}$ or GND, $I_O = 0$ ,		Outputs high		0.12		mA	
			Outputs low		5			
			Outputs disabled		0.12			0.12
$\Delta I_{CC}^\parallel$	$V_{CC} = 3\text{ V to }3.6\text{ V}$ , One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}$ or GND		0.2		0.2		mA	
$C_i$	$V_I = 3\text{ V or }0$		4		4		pF	
$C_{io}$	$V_O = 3\text{ V or }0$		13		13		pF	

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ Unused pins at  $V_{CC}$  or GND¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

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## 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS

### WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		SN54LVT16952				SN74LVT16952				UNIT
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency	0	150	0	150	0	150	0	150	MHz
$t_w$	Pulse duration	CLKEN high		3.3	3.3	3.3	3.3	3.3	3.3	ns
		CLK high or low		3.3	3.3	3.3	3.3	3.3	3.3	
$t_{\text{su}}$	Setup time	A or B before CLK		2.6	3.3	2.1	2.9	2.1	2.9	ns
		CLKEN before CLK		1.2	1.6	1.2	1.6	1.2	1.6	
$t_h$	Hold time	A or B after CLK		0.7	0.7	0.7	0.7	0.7	0.7	ns
		CLKEN after CLK		1.4	1.5	1.4	1.5	1.4	1.5	

switching characteristics over recommended operating free-air temperature range,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)

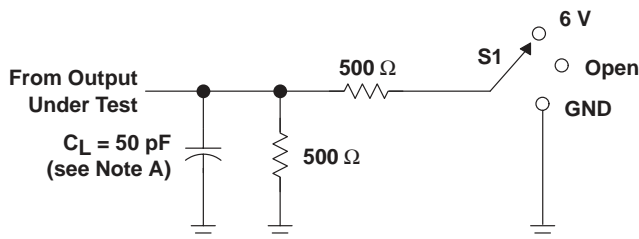
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT16952				SN74LVT16952				UNIT	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
$f_{\text{max}}$			150		150			150			150	MHz
$t_{\text{PLH}}$	CLKBA or CLKAB	A or B	1.6	5.7		7.4	2	3.4	5.8		7.1	ns
$t_{\text{PHL}}$			2	6		7	2	3.4	5.8		6.9	
$t_{\text{PZH}}$	$\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$	A or B	1	5		7.3	1	2.7	5.6		6.7	ns
$t_{\text{PZL}}$			1.2	5.2		5.9	1.2	2.7	6.5		8	
$t_{\text{PHZ}}$	$\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$	A or B	1.8	6.7		7.3	2.3	3.9	6.3		6.9	ns
$t_{\text{PLZ}}$			1.2	5.8		6	2.2	3.9	5.1		5.3	

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

SN54LVT16952, SN74LVT16952  
3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS  
WITH 3-STATE OUTPUTS

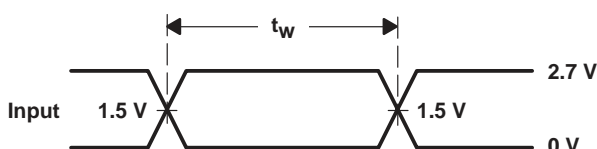
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PARAMETER MEASUREMENT INFORMATION

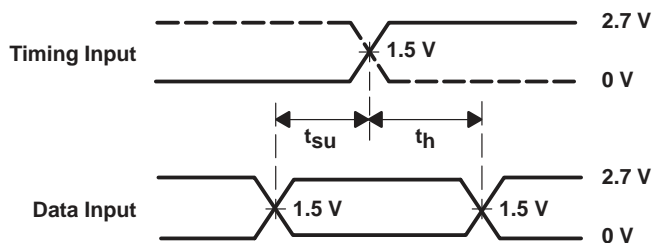


TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND

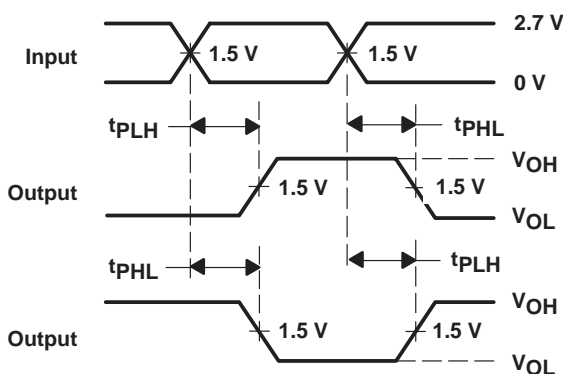
LOAD CIRCUIT



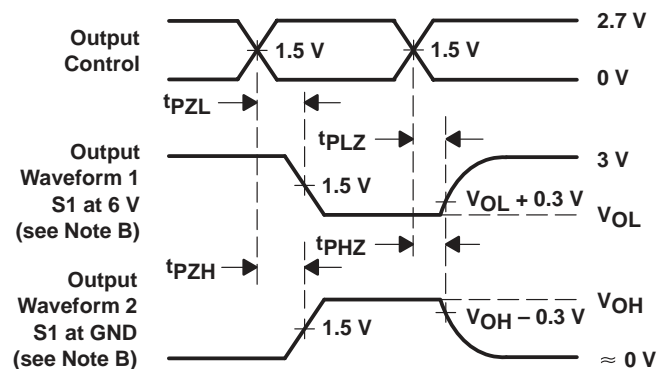
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVT16952DGGR	NRND	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT16952	
SN74LVT16952DL	NRND	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT16952	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

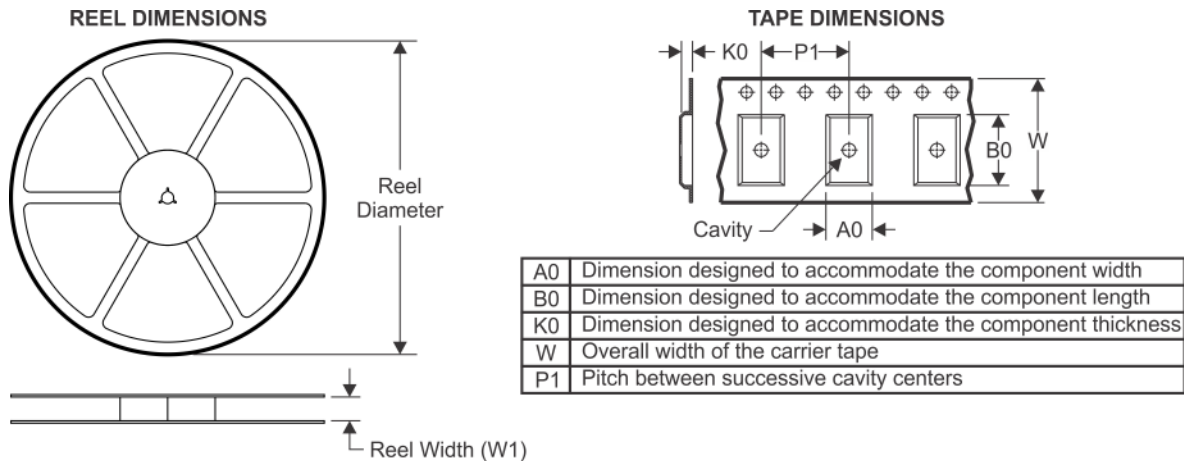
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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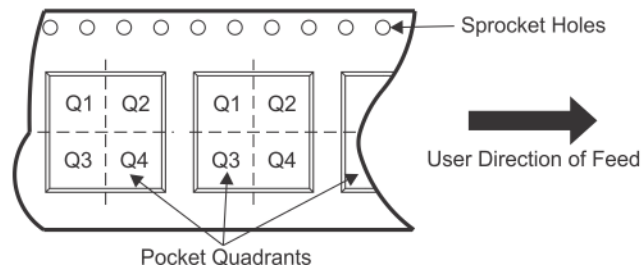


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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVT16952DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

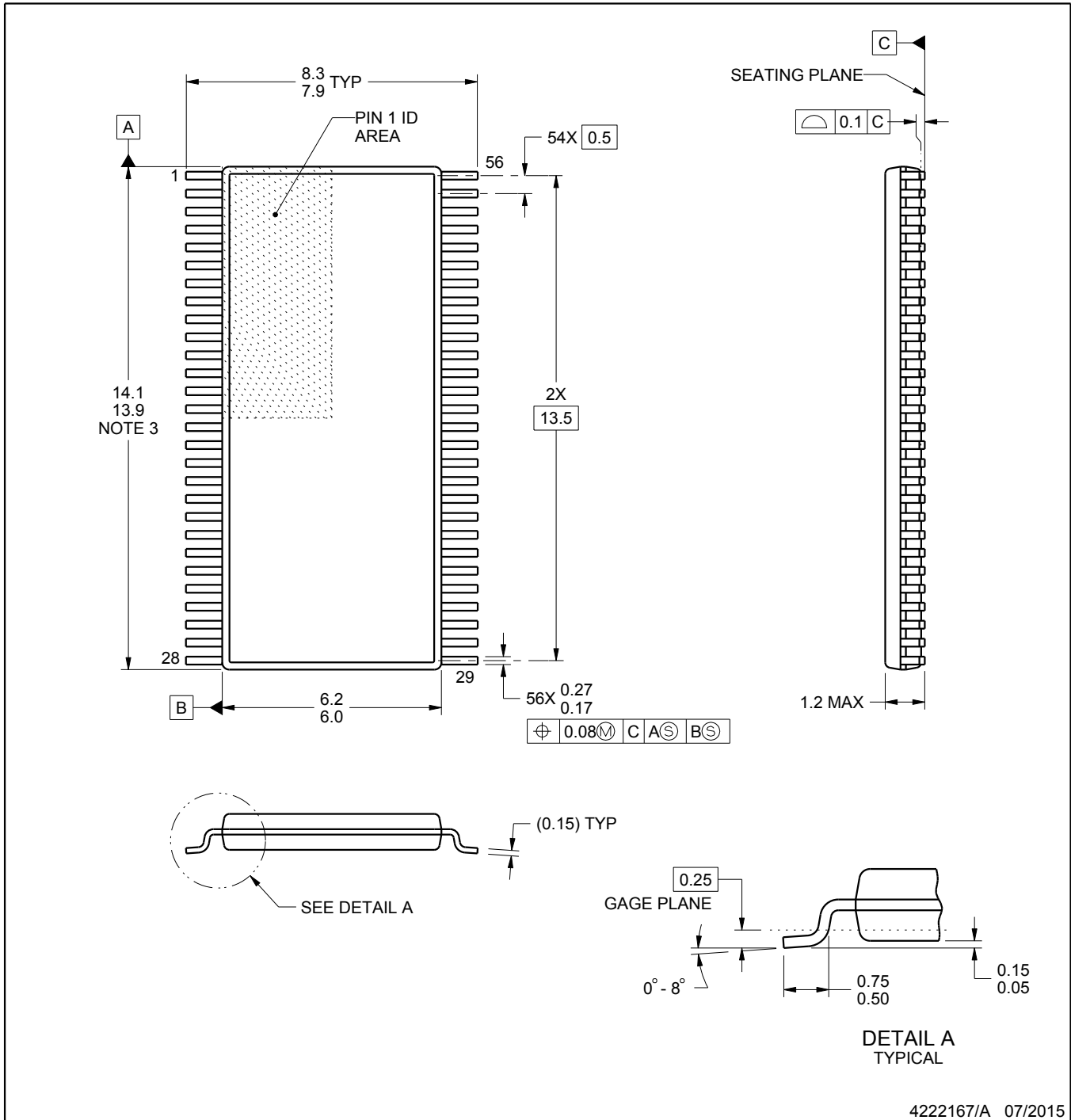
TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVT16952DGGR	TSSOP	DGG	56	2000	367.0	367.0	45.0





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NOTES:

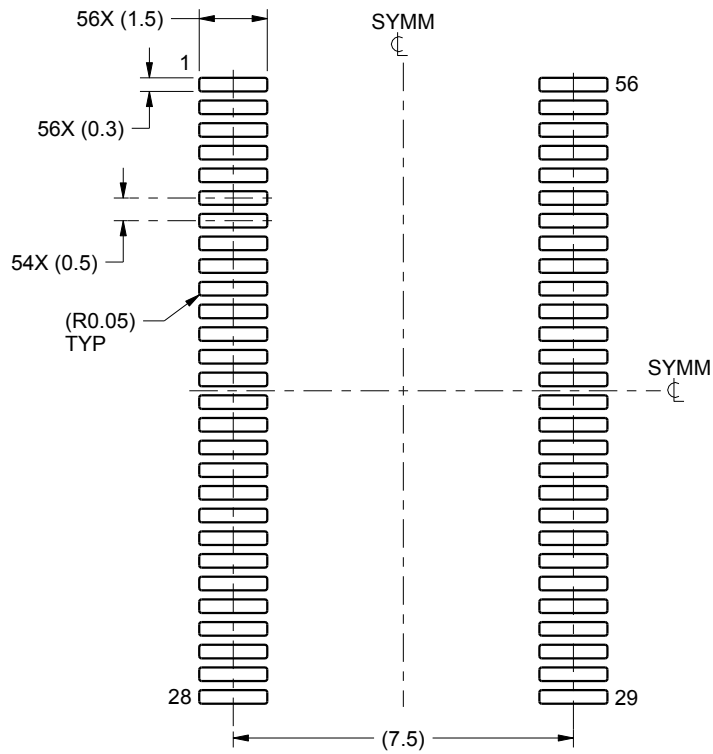
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

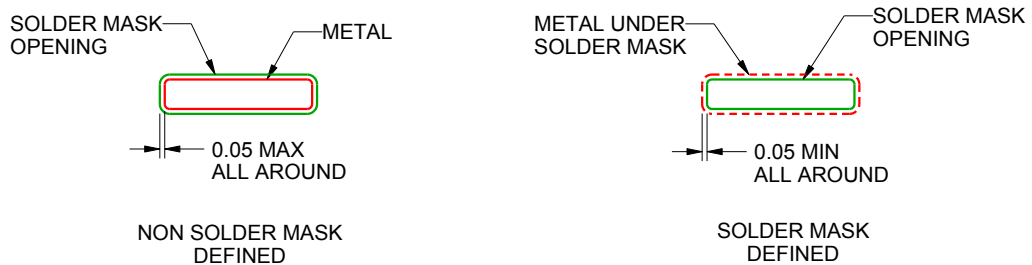
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

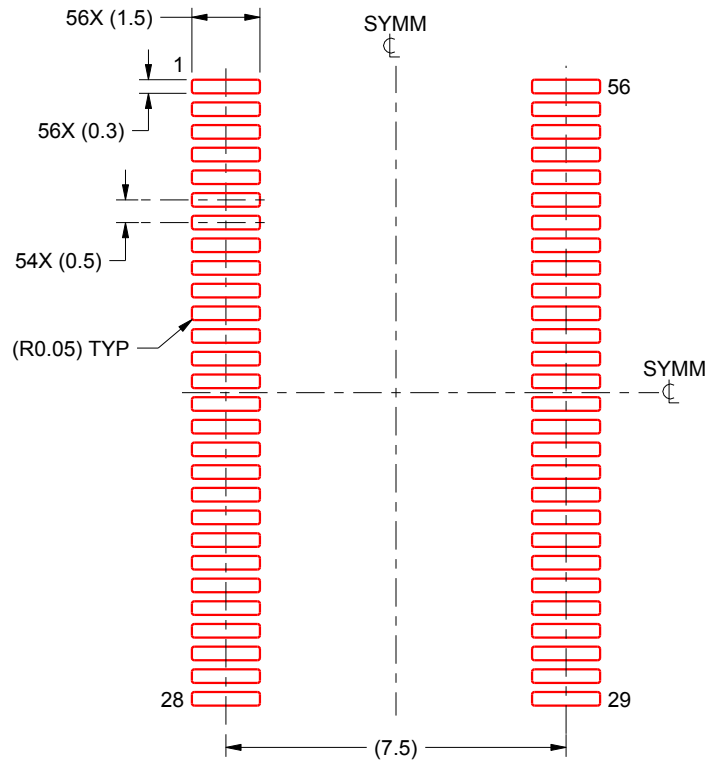
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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