



STP52N25M5

N-channel 250 V, 0.055 Ω , 28 A, TO-220
MDmesh™ V Power MOSFET

Features

| Type | V _{DSS} | R _{DS(on)} max | I _D |
|------------|------------------|----------------------------|----------------|
| STP52N25M5 | 250 V | < 0.065 Ω | 28 A |

- Amongst the best R_{DS(on)}* area
- High dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested

Application

- Switching applications

Description

This device is an N-channel MDmesh™ V Power MOSFET based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

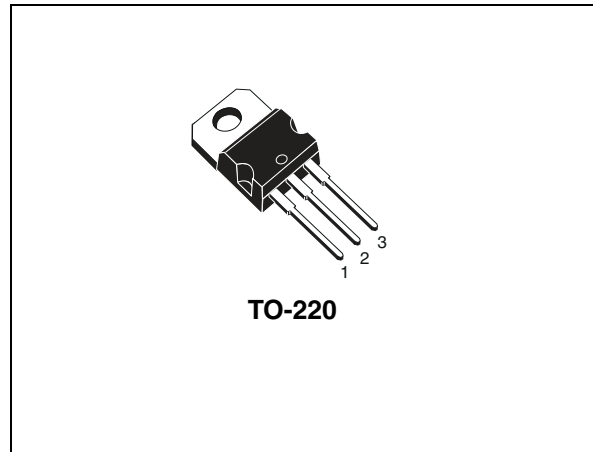


Figure 1. Internal schematic diagram

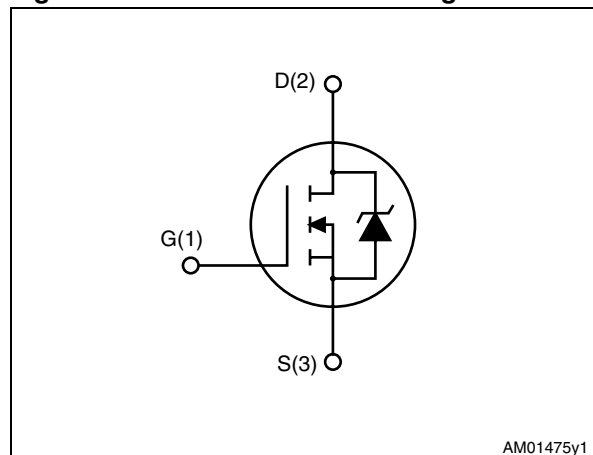


Table 1. Device summary

| Order code | Marking | Package | Packaging |
|------------|---------|---------|-----------|
| STP52N25M5 | 52N25M5 | TO-220 | Tube |

Contents

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1 Electrical ratings

Table 2. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|--------------------|--|------------|------|
| V_{GS} | Gate- source voltage | 25 | V |
| I_D | Drain current (continuous) at $T_C = 25\text{ °C}$ | 28 | A |
| I_D | Drain current (continuous) at $T_C = 100\text{ °C}$ | 18 | A |
| $I_{DM}^{(1)}$ | Drain current (pulsed) | 112 | A |
| P_{TOT} | Total dissipation at $T_C = 25\text{ °C}$ | 110 | W |
| I_{AR} | Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max) | 10 | A |
| E_{AS} | Single pulse avalanche energy (starting $T_J = 25\text{ °C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$) | 230 | mJ |
| $dv/dt^{(2)}$ | Peak diode recovery voltage slope | 15 | V/ns |
| T_J T_{stg} | Operating junction temperature Storage temperature | -55 to 150 | °C |

1. Pulse width limited by safe operating area.

2. $I_{SD} \leq 28\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{Peak} < V_{(BR)DSS}$.

Table 3. Thermal data

| Symbol | Parameter | Value | Unit |
|----------------|--|-------|------|
| $R_{thj-case}$ | Thermal resistance junction-case max | 1.14 | °C/W |
| $R_{thj-amb}$ | Thermal resistance junction-pcb max | 62.5 | °C/W |
| T_J | Maximum lead temperature for soldering purpose | 300 | °C/W |

2 Electrical characteristics

(T_{case} = 25°C unless otherwise specified).

Table 4. On /off states

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------------|---|---|------|-------|----------|----------|
| V _{(BR)DSS} | Drain-source breakdown voltage | I _D = 1 mA, V _{GS} = 0 | 250 | | | V |
| I _{DSS} | Zero gate voltage drain current (V _{GS} = 0) | V _{DS} = Max rating V _{DS} = Max rating, T _C = 125 °C | | | 1 100 | μA μA |
| I _{GSS} | Gate-body leakage current (V _{DS} = 0) | V _{GS} = ± 25 V | | | 100 | nA |
| V _{GS(th)} | Gate threshold voltage | V _{DS} = V _{GS} , I _D = 100 μA | 3 | 4 | 5 | V |
| R _{DS(on)} | Static drain-source on-resistance | V _{GS} = 10 V, I _D = 14 A | | 0.055 | 0.065 | Ω |

Table 5. Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------------------------|--|---|------|------|------|------|
| C _{iss} | Input capacitance | V _{DS} = 50 V, f = 1 MHz, V _{GS} = 0 | - | 1770 | - | pF |
| C _{oss} | Output capacitance | | | 110 | | pF |
| C _{rss} | Reverse transfer capacitance | | | 17 | | pF |
| C _{o(er)} ⁽¹⁾ | Equivalent output capacitance energy related | V _{GS} = 0, V _{DS} = 0 to 80% V _{(BR)DSS} | - | 93 | - | pF |
| C _{o(tr)} ⁽²⁾ | Equivalent output capacitance time related | V _{GS} = 0, V _{DS} = 0 to 80% V _{(BR)DSS} | - | 178 | - | pF |
| R _g | Gate input resistance | f = 1 MHz open drain | - | 2 | - | Ω |
| Q _g | Total gate charge | V _{DD} = 200 V, I _D = 28 A, | - | 47 | - | nC |
| Q _{gs} | Gate-source charge | V _{GS} = 10 V | | 10 | | nC |
| Q _{gd} | Gate-drain charge | (see Figure 14) | | 24 | | nC |

1. C_{o(er)} is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
2. C_{o(tr)} is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

Table 6. Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max | Unit |
|--------------|--------------------|---|------|------|-----|------|
| $t_{d(V)}$ | Voltage delay time | $V_{DD} = 125\text{ V}$, $I_D = 14\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13) | | 40 | | ns |
| $t_{r(V)}$ | Voltage rise time | | - | 18 | - | ns |
| $t_{f(I)}$ | Current fall time | | | | 64 | ns |
| $t_{c(off)}$ | Crossing time | | | | 82 | ns |

Table 7. Source drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max | Unit |
|-----------------|-------------------------------|---|------|------|------|---------------|
| I_{SD} | Source-drain current | | | | 28 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | - | | 112 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $I_{SD} = 28\text{ A}$, $V_{GS} = 0$ | - | | 1.6 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 28\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_J = 25\text{ }^\circ\text{C}$ (see Figure 15) | | 168 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 1.2 | | μC |
| I_{RRM} | Reverse recovery current | | | | 14.5 | A |
| t_{rr} | Reverse recovery time | $I_{SD} = 28\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 15) | | 196 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 1.7 | | μC |
| I_{RRM} | Reverse recovery current | | | | 17 | A |

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

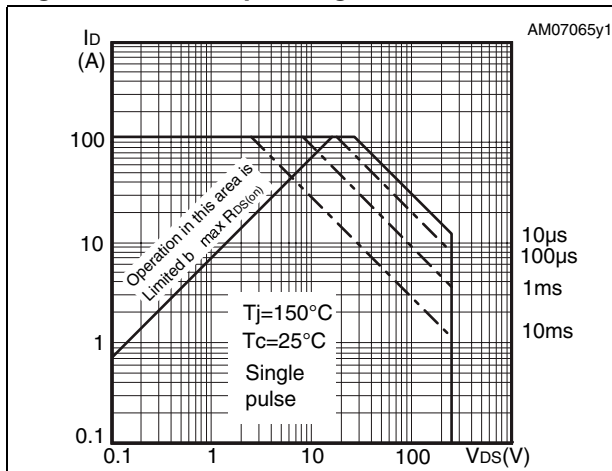


Figure 3. Thermal impedance

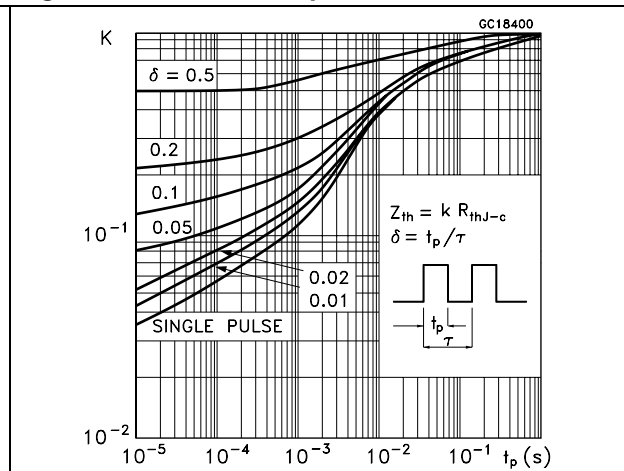


Figure 4. Output characteristics

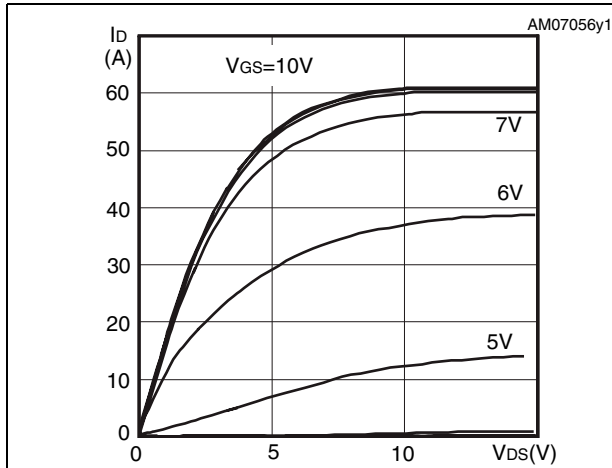


Figure 5. Transfer characteristics

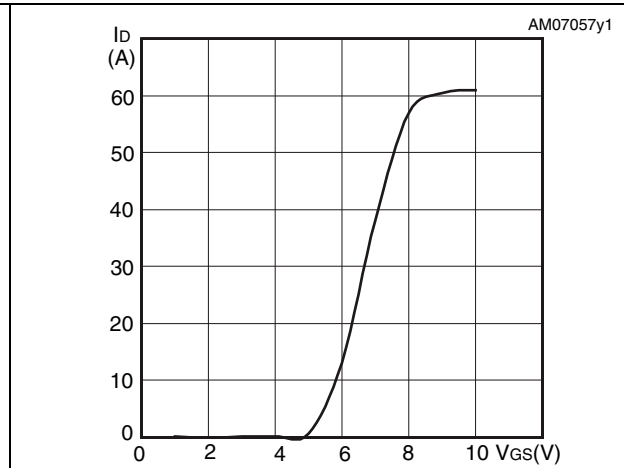


Figure 6. Gate charge vs gate-source voltage

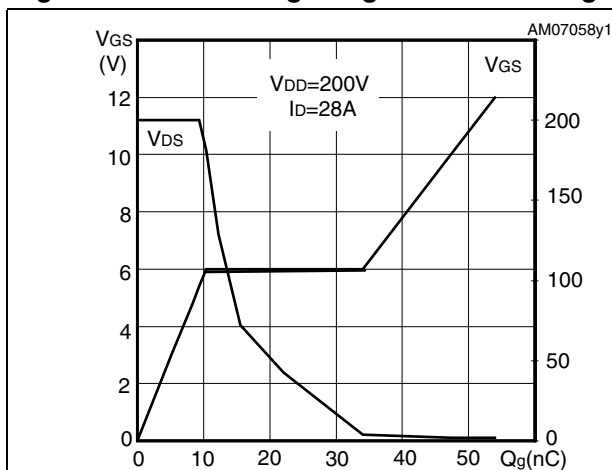


Figure 7. Static drain-source on resistance

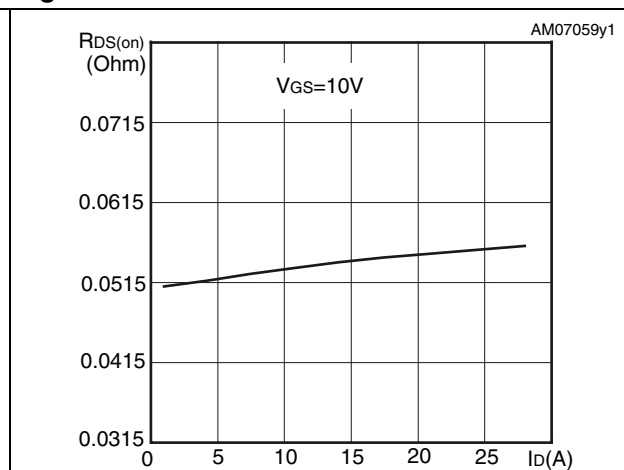


Figure 8. Capacitance variations

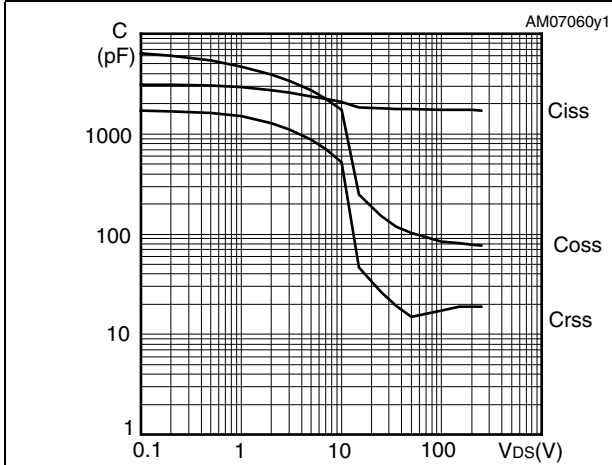


Figure 9. Output capacitance stored energy

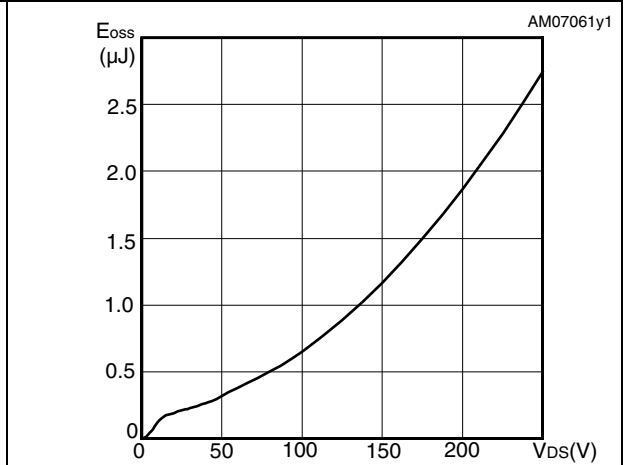


Figure 10. Normalized gate threshold voltage vs temperature

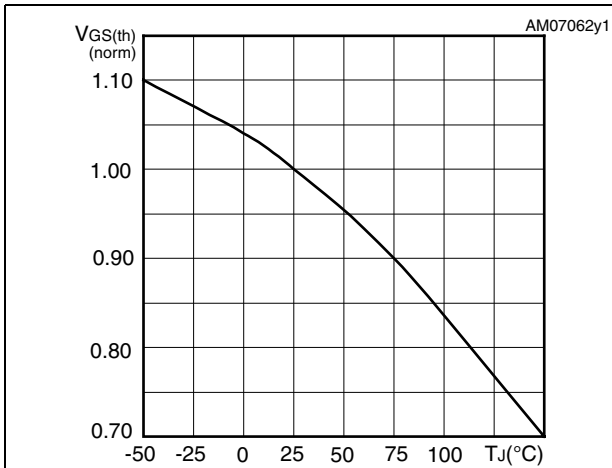


Figure 11. Normalized on resistance vs temperature

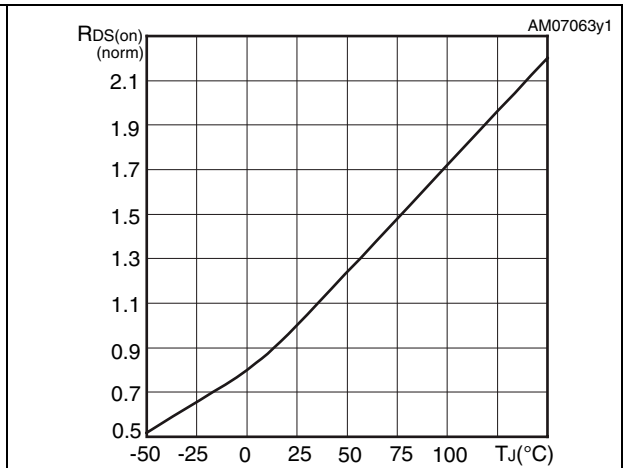
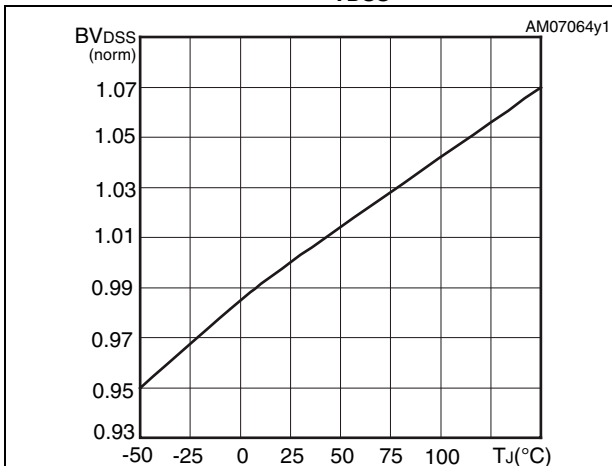


Figure 12. Normalized B_{VDS} vs temperature



3 Test circuits

Figure 13. Switching times test circuit for resistive load

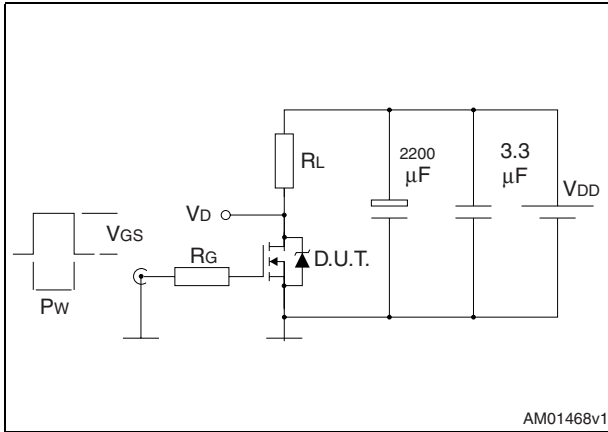


Figure 14. Gate charge test circuit

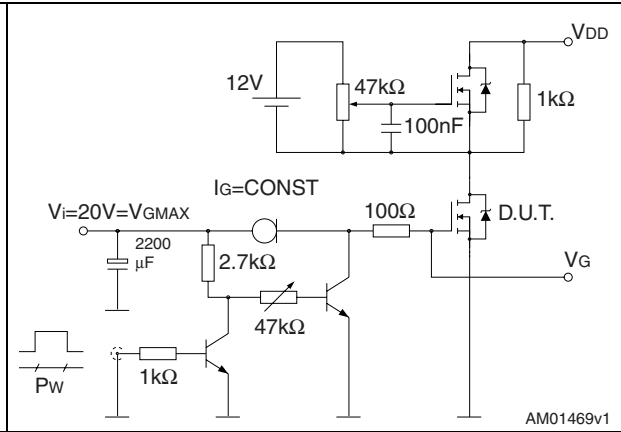


Figure 15. Test circuit for inductive load switching and diode recovery times

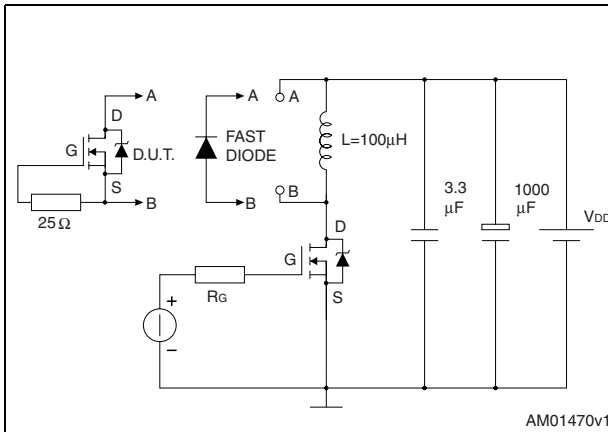


Figure 16. Unclamped inductive load test circuit

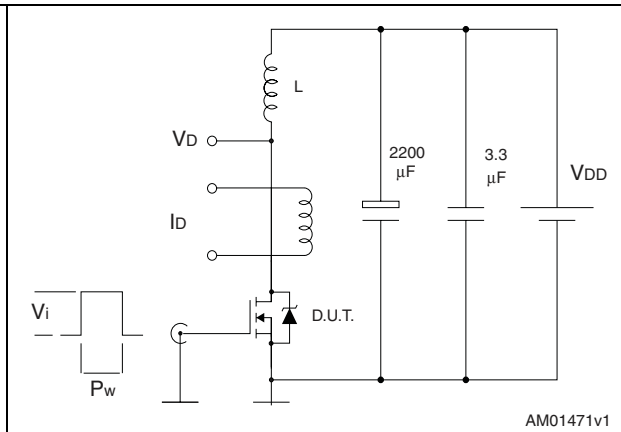


Figure 17. Unclamped inductive waveform

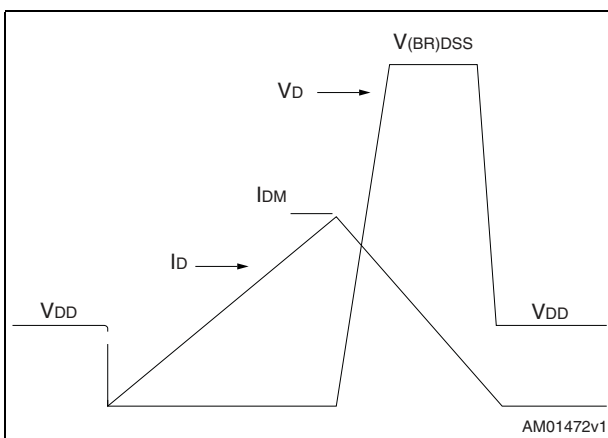
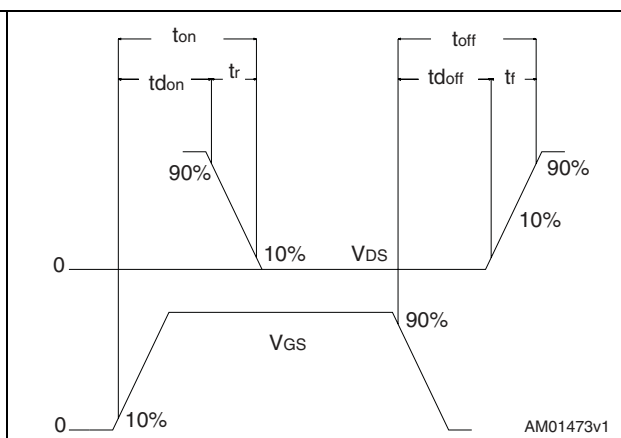


Figure 18. Switching time waveform

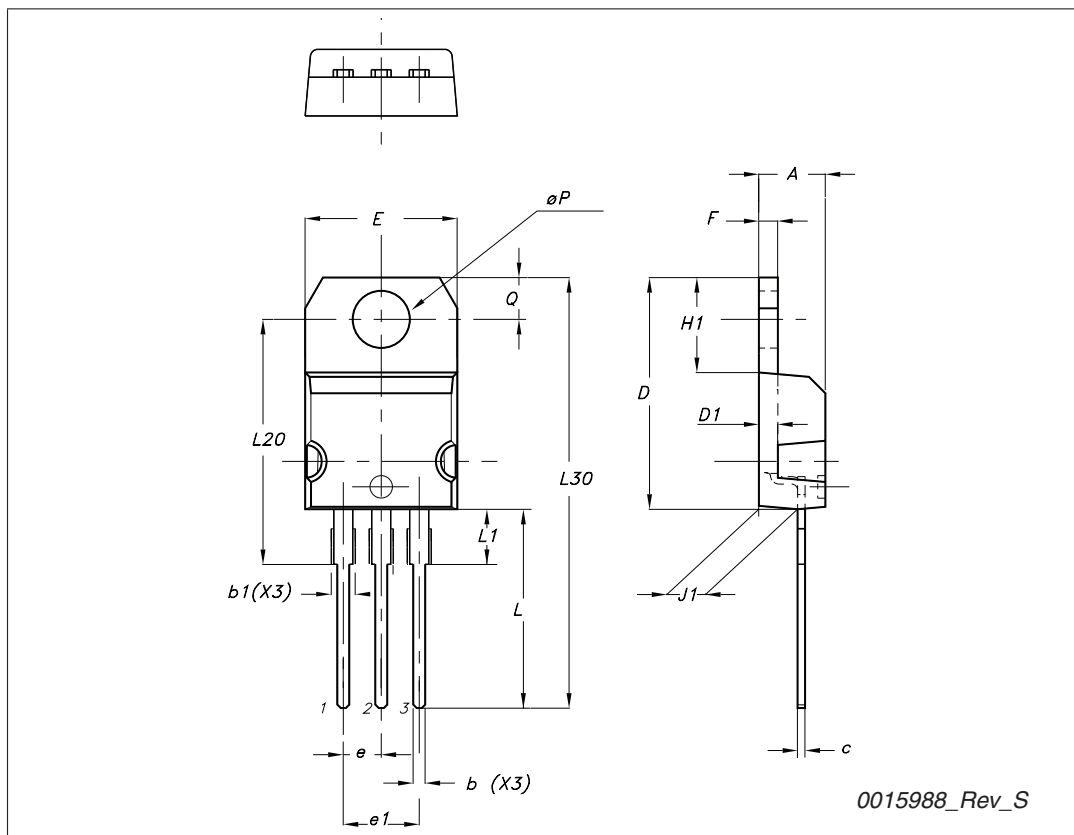


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

TO-220 type A mechanical data

| Dim | mm | | |
|-----|-------|-------|-------|
| | Min | Typ | Max |
| A | 4.40 | | 4.60 |
| b | 0.61 | | 0.88 |
| b1 | 1.14 | | 1.70 |
| c | 0.48 | | 0.70 |
| D | 15.25 | | 15.75 |
| D1 | | 1.27 | |
| E | 10 | | 10.40 |
| e | 2.40 | | 2.70 |
| e1 | 4.95 | | 5.15 |
| F | 1.23 | | 1.32 |
| H1 | 6.20 | | 6.60 |
| J1 | 2.40 | | 2.72 |
| L | 13 | | 14 |
| L1 | 3.50 | | 3.93 |
| L20 | | 16.40 | |
| L30 | | 28.90 | |
| ∅P | 3.75 | | 3.85 |
| Q | 2.65 | | 2.95 |



5 Revision history

Table 8. Document revision history

| Date | Revision | Changes |
|-------------|----------|---------------|
| 29-Jul-2010 | 1 | First release |

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