MAX4896

Space-Saving, 8-Channel Relay/Load Driver

General Description

The MAX4896 8-channel relay and load driver is designed for medium voltage applications up to 50V. This device is offered in a 20-pin, 5mm x 5mm TQFN package, resulting in substantial board-space savings.

The MAX4896 8-channel relay driver offers built-in inductive kickback protection, drive for latching/nonlatching or dual-coil relays, and open-load and short-circuit fault detection. The MAX4896 also protects against overcurrent conditions. Each independent open-drain output features a 3Ω (typ) on-resistance, and is guaranteed to sink 200mA of load current ($V_S \geq 4.5V$).

A built-in overvoltage-protection clamp handles kickback-voltage transients, which are common when driving inductive loads. Thermal-shutdown circuitry shuts off all outputs (OUT_) when the junction temperature exceeds +160°C. The MAX4896 employs a reset input that allows the user to turn off all outputs simultaneously with a single control line.

The MAX4896 includes a 10MHz SPI™-/QSPI™-/MICROWIRE™-compatible serial interface. The serial interface is compatible with TTL-/CMOS-logic voltage levels and operates with a single +2.7V to +5.5V supply. In addition, the SPI output data can be used for diagnostics purposes including open-load and short-circuit fault detection.

The MAX4896 is offered in the extended (-40°C to +85°C) and (-40°C to +125°C) operating temperature ranges.

Applications

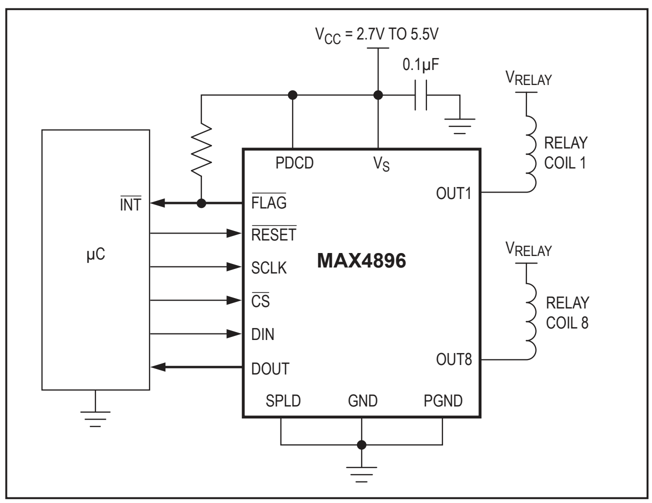
- Industrial Equipment
- White Goods
- Power-Grid Monitoring and Protection Equipment
- ATE

***Ordering Information* appears at end of data sheet.**

Benefits and Features

- Relay Driver Supports Medium Voltage Applications
    - Up to 50V Continuous Drain-to-Source Voltage
    - +2.7V to +5.5V Logic Supply Voltage
    - Guaranteed Drive Current:
      $V_S \geq 4.5V$: 200mA (All Channels On)/410mA (Individual Channels)
      $V_S \leq 3.6V$: 100mA
- Integration and Small Packages Save Board Space
    - 5mm x 5mm, 20-Pin TQFN Package
- Built-In Protection Circuitry Increases Safety
    - Built-In Output Clamp Protects Against Inductive Kickback
    - Open-Load and Short-Circuit Detection and Protection
    - Thermal Shutdown
    - $\overline{\text{RESET}}$ Input Turns Off All Outputs Simultaneously
    - $\overline{\text{FLAG}}$ Output for µP Interrupt
    - Built-in Power-On Reset
    - Temperature Range (-40°C to +125°C)
- Serial Port Supports Most Microcontroller Architectures
    - SPI-/QSPI-/MICROWIRE-Compatible Serial Interface
    - Serial Digital Output for Daisy-Chaining and Diagnostics
- Low Power Consumption Reduces Power Supply Requirements Saving System Cost
- Low 100µA (Max) Quiescent Supply Current

Typical Operating Circuit



Absolute Maximum Ratings

(All voltages referenced to GND.)
V_S ....-0.3V to +7.0V
OUT_ .... (-0.3V to +50V)
Continuous OUT_ Voltage ....+50V
$\overline{CS}$, SCLK, DIN, $\overline{RESET}$, SPLD, PDCD ....-0.3V to +7.0V
DOUT ....-0.3V to (V_S + 0.3V)
PGND to GND .... (-0.3V to +0.3V)
Continuous OUT_ Current, T_A = +25°C (Note 1)
All Outputs On 210mA
Single Output On 420mA

Continuous Power Dissipation (T_A = +70°C)
20-Pin TQFN (derate 21.3mW/°C above +70°C) 1702mW
Maximum Output Clamp Energy ($E_{OUT\_}$).................... 30mJ
Operating Temperature Range.................... -40°C to +125°C
Junction Temperature....................+150°C
Storage Temperature Range.................... -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Maximum continuous current at a given temperature must be calculated such that the maximum continuous power dissipation for the package is not exceeded.

Package Information

20-Pin TQFN

Package Code	T2055+5
Outline Number	**21-0140**
Land Pattern Number	**90-0010**
Thermal Resistance	
Junction to Ambient (θ_{JA})	29ºC/W
Junction to Case (θ_{JC})	2ºC/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_S = +2.7V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage	V_S			2.7		5.5	V
Quiescent Current	I_{CC}	$I_{OUT\_}$ = 0, logic inputs = 0 or V_S, $\overline{RESET}$ = low	V_S = 3.6V		5	70	µA
			V_S = 5V		10	100	
Dynamic Average Supply Current	I_S	f_{SCLK} = 10MHz, f_{DIN} = 0.5 x f_{CLK}, C_{OUT} = 50pF, V_S = 5.5V				6	mA
Thermal Shutdown	T_{SHD}				+160		°C
Thermal-Shutdown Hysteresis	T_{SHDH}				20		°C
Power-On Reset	V_{RST}	V_S falling		1.8	2.05	2.3	V
Power-On-Reset Hysteresis	V_{RSTH}				140		mV
DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$, $\overline{RESET}$, PDCD, SPLD)							
Input Logic-High Voltage	V_{IH}	V_S = 2.7V to 3.6V		2.0			V
		V_S = 4.5V to 5.5V		2.4			
Input Logic-Low Voltage	V_{IL}	V_S = 2.7V to 3.6V				0.6	V
		V_S = 4.5V to 5.5V				0.8	
Input Logic Hysteresis	V_{HYST}				230		mV
Input Leakage Currents	I_{LEAK}	Input voltages = 0 or +5.5V		-1		+1	µA
Input Capacitance	C_{IN}				10		pF
RELAY OUTPUT DRIVERS (OUT1–OUT8)							
OUT_ ON Resistance	R_{ON}	I_{OUT} = 50mA, V_S = 2.7V	T_J = +25°C		5	6	Ω
			T_J = +125°C			11	
			T_J = +150°C			12	
		I_{OUT} = 100mA, V_S = 4.5V	T_J = +25°C		3	4	
			T_J = +125°C			7	
			T_J = +150°C			8	
I_{OUT} Off-Leakage Current	I_{LEAK}	PDCD = high or $\overline{RESET}$ = low, all outputs Off		-1		+1	µA
OUT Clamping Voltage	V_{CLAMP}	(Note 3)		50		75	V
OUT Current-Limit Threshold	I_{LIM}	$V_S \geq$ 4.5V		400		960	mA
OUT Capacitance		V_{OUT} = 16V, f = 1MHz			30		pF

Electrical Characteristics (continued)

(V_S = +2.7V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIAGNOSTIC						
Open-Load Detection Voltage Threshold	$V_{DS(OL)}$	OUT_ falling	0.75	1	1.15	V
Open-Load Detection-Voltage-Threshold Hysteresis	$V_{DS(OLH)}$			40		mV
OUT_ Pulldown Current	$I_{PD(OL)}$	PDCD = low	150	300	500	µA
Fault Delay/Filtering Time	$t_{D(FAULT)}$	From rising edge at $\overline{CS}$ at 50% to valid diagnostic data	30	90	280	µs
DIGITAL OUTPUT (DOUT, $\overline{FLAG}$)						
DOUT Low Voltage	V_{OL}	2.7V ≤ V_S ≤ 3.6V, I_{SINK} = 0.3mA			0.4	V
		4.5V ≤ V_S ≤ 5.5V, I_{SINK} = 0.5mA			0.4	
DOUT High Voltage	V_{OH}	2.7V ≤ V_S ≤ 3.6V, I_{SOURCE} = 0.25mA	V_S - 0.5			V
		4.5V ≤ V_S ≤ 5.5V, I_{SOURCE} = 0.4mA	V_S - 0.5			
$\overline{FLAG}$ Low Voltage		I_{SINK} = 0.5mA			0.4	V
$\overline{FLAG}$ Off-Leakage Current		4.5V ≤ V_S ≤ 5.5V, $V_{\overline{FLAG}}$ = 5.5V	-1		+1	µA
TIMING						
Turn-On Time (OUT_)	t_{ON}	From rising edge of $\overline{CS}$ at 50% to $V_{OUT\_}$ = 90%VP, VP = 15V, R_L = 300Ω, C_L = 50pF, 2.7V ≤ V_S < 3.6V			20	µs
		From rising edge of $\overline{CS}$ at 50% to $V_{OUT\_}$ = 90%VP, VP =16V, R_L = 150Ω, C_L = 50pF, 4.5V ≤ V_S ≤ 5.5V			10	
Turn-Off Time (OUT_)	t_{OFF}	From rising edge of $\overline{CS}$ at 50% to $V_{OUT\_}$ = 10%VP, VP = 15V, R_L = 300Ω, C_L = 50pF, 2.7V ≤ V_S < 3.6V			15	µs
		From rising edge of $\overline{CS}$ at 50% to $V_{OUT\_}$ = 90%VP, VP = 16V, R_L = 150Ω, C_L = 50pF, 4.5V < V_S ≤ 5.5V			10	
SCLK Frequency	f_{SCLK}	T_A = +85°C, 2.7V ≤ V_S < 3.6V	0		6	MHz
		T_A = +85°C, 4.5V ≤ V_S ≤ 5.5V			11	
		T_A = +125°C, 2.7V ≤ V_S ≤ 3.6V	0		5	
		T_A = +125°C, 4.5V ≤ V_S ≤ 5.5V			10	
Cycle Time	t_{CH} + t_{CL}	2.7V ≤ V_S ≤ 3.6V	200			ns
		4.5V ≤ V_S ≤ 5.5V	100			
$\overline{CS}$ Fall-to-SCLK Rise Setup	t_{CSS}	2.7V ≤ V_S ≤ 3.6V	100			ns
		4.5V ≤ V_S ≤ 5.5V	50			

Electrical Characteristics (continued)

(V_S = +2.7V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

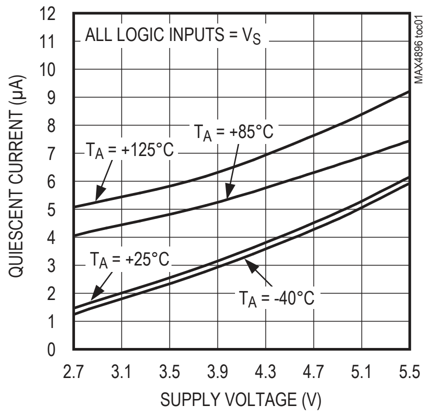
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{CS}$ Rise-to-SCLK Hold	t_{CSH}	2.7V ≤ V_S ≤ 3.6V		100			ns
		4.5V ≤ V_S ≤ 5.5V		50			
SCLK High Time	t_{CH}	2.7V ≤ V_S ≤ 3.6V		80			ns
		4.5V ≤ V_S ≤ 5.5V		40			
SCLK Low Time	t_{CL}	2.7V ≤ V_S ≤ 3.6V		80			ns
		4.5V ≤ V_S ≤ 5.5V		40			
Data Setup Time	t_{DS}	2.7V ≤ V_S ≤ 3.6V		40			ns
		4.5V ≤ V_S ≤ 5.5V		20			
Data Hold Time	t_{DH}	2.7V ≤ V_S ≤ 3.6V		5			ns
		4.5V ≤ V_S ≤ 5.5V		0			
SCLK Fall-to-DOUT Valid	t_{DO}	50% of SCLK to 20% of V_S falling edge, C_L = 50pF, 50% at SCLK to 80% of VS rising edge	2.7V ≤ V_S ≤ 3.6V			70	ns
			4.5V ≤ V_S ≤ 5.5V			30	
Rise Time (DIN, SCLK, $\overline{CS}$, $\overline{RESET}$)	t_{SCR}	20% of V_S to 70% of V_S, C_L = 50pF (Note 4)	2.7V ≤ V_S ≤ 3.6V			2	µs
			4.5V ≤ V_S ≤ 5.5V			2	
Fall Time (DIN, SCLK, $\overline{CS}$, $\overline{RESET}$)	t_{SCF}	20% of V_S to 70% of V_S, C_L = 50pF (Note 4)	2.7V ≤ V_S ≤ 3.6V			2	µs
			4.5V ≤ V_S ≤ 5.5V			2	
$\overline{RESET}$ Min Pulse Width	t_{RW}			70			ns

Note 2: Specifications at -40°C are guaranteed by design and not production tested.
Note 3: The output stages are compliant with the transient immunity requirements, as specified in ISO 7637 Part 3 with test pulses 1, 2, 3a, and 3b.
Note 4: Guaranteed by design.

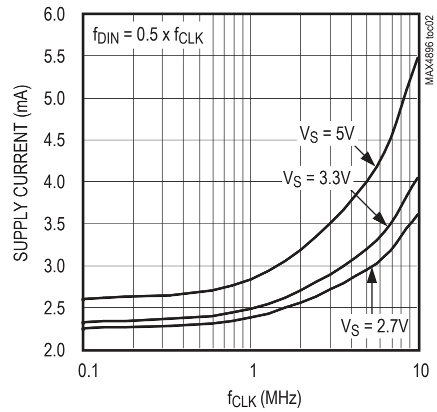
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

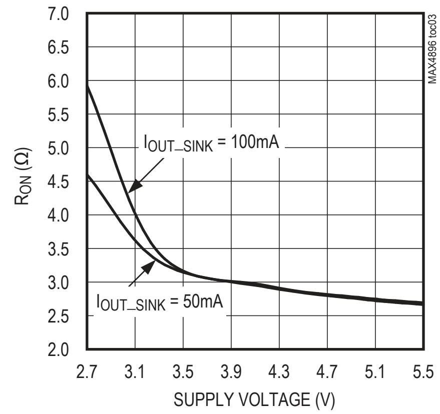
QUIESCENT CURRENT vs. SUPPLY VOLTAGE



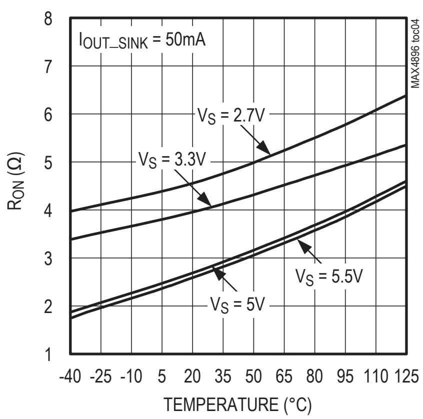
SUPPLY CURRENT vs. fCLK



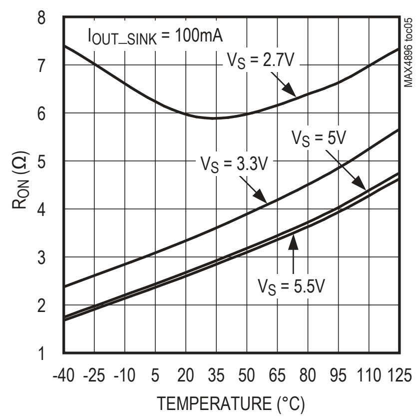
ON-RESISTANCE vs. SUPPLY VOLTAGE



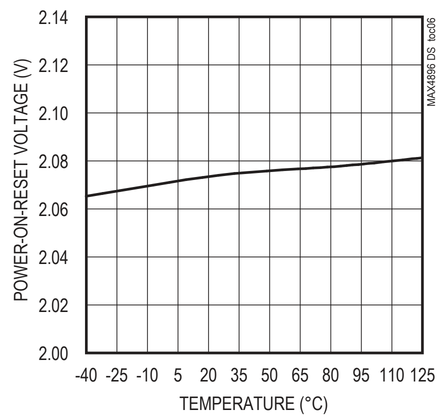
ON-RESISTANCE vs. TEMPERATURE



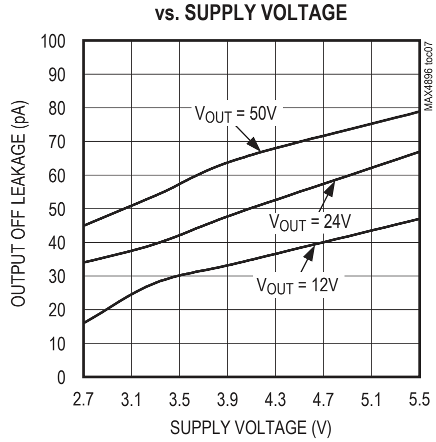
ON-RESISTANCE vs. TEMPERATURE



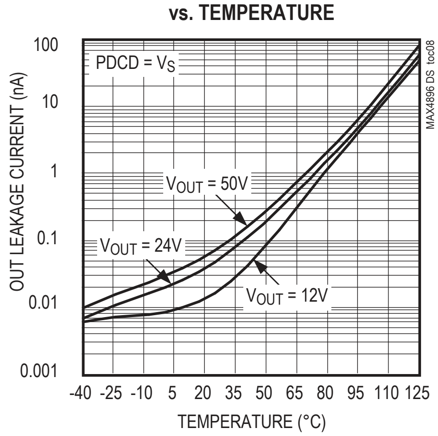
POWER-ON RESET VOLTAGE vs. TEMPERATURE



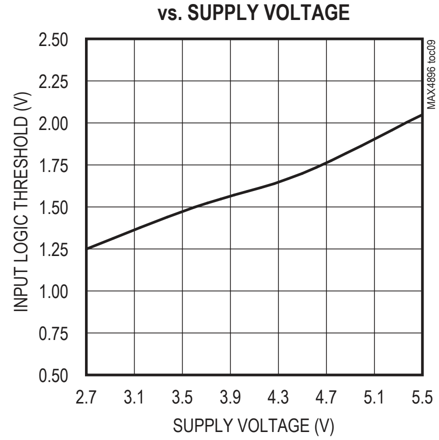
OUTPUT OFF LEAKAGE CURRENT vs. SUPPLY VOLTAGE



OUT LEAKAGE CURRENT vs. TEMPERATURE



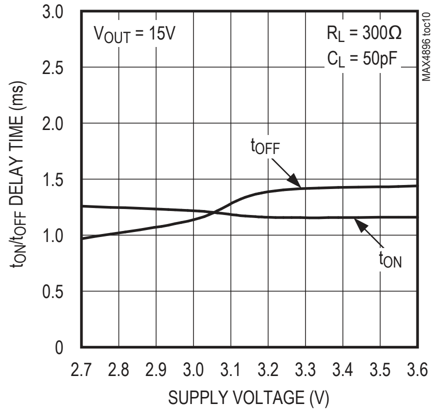
INPUT LOGIC THRESHOLD vs. SUPPLY VOLTAGE



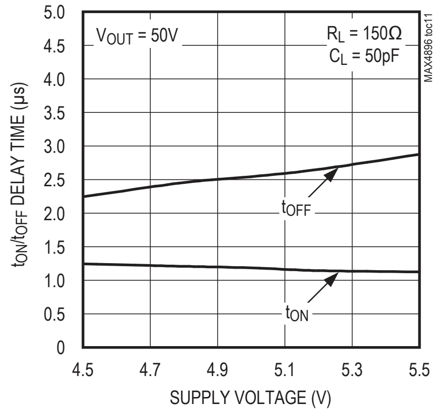
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

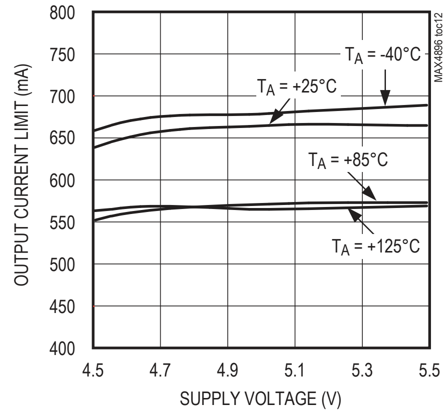
TURN-ON/TURN-OFF DELAY TIME vs. SUPPLY VOLTAGE



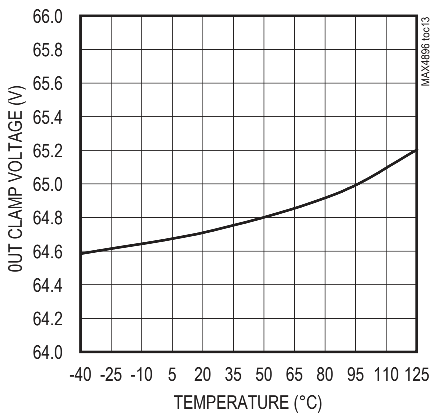
TURN-ON/TURN-OFF DELAY TIME vs. SUPPLY VOLTAGE



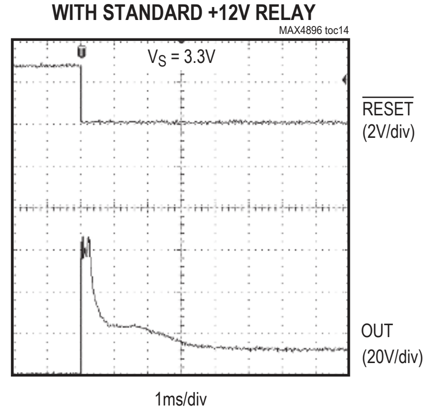
OUT_ CURRENT LIMIT vs. SUPPLY VOLATGE



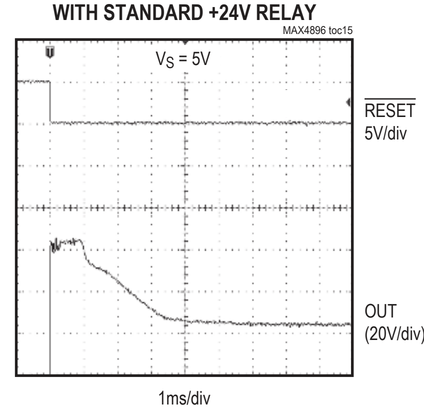
OUT CLAMP VOLTAGE vs. TEMPERATURE



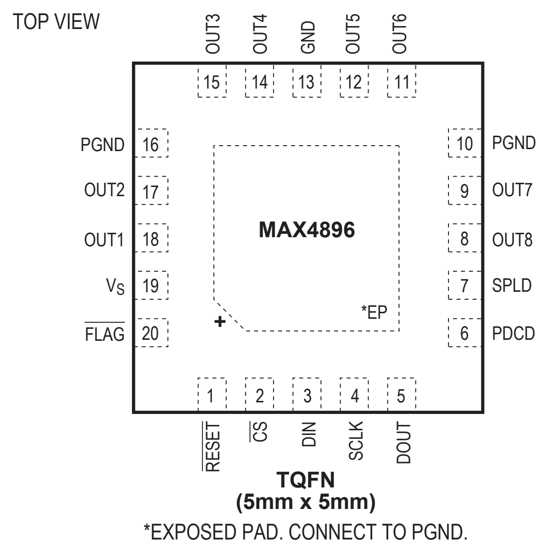
BACK-EMF CLAMPING WITH STANDARD +12V RELAY



BACK-EMF CLAMPING WITH STANDARD +24V RELAY



Pin Configuration



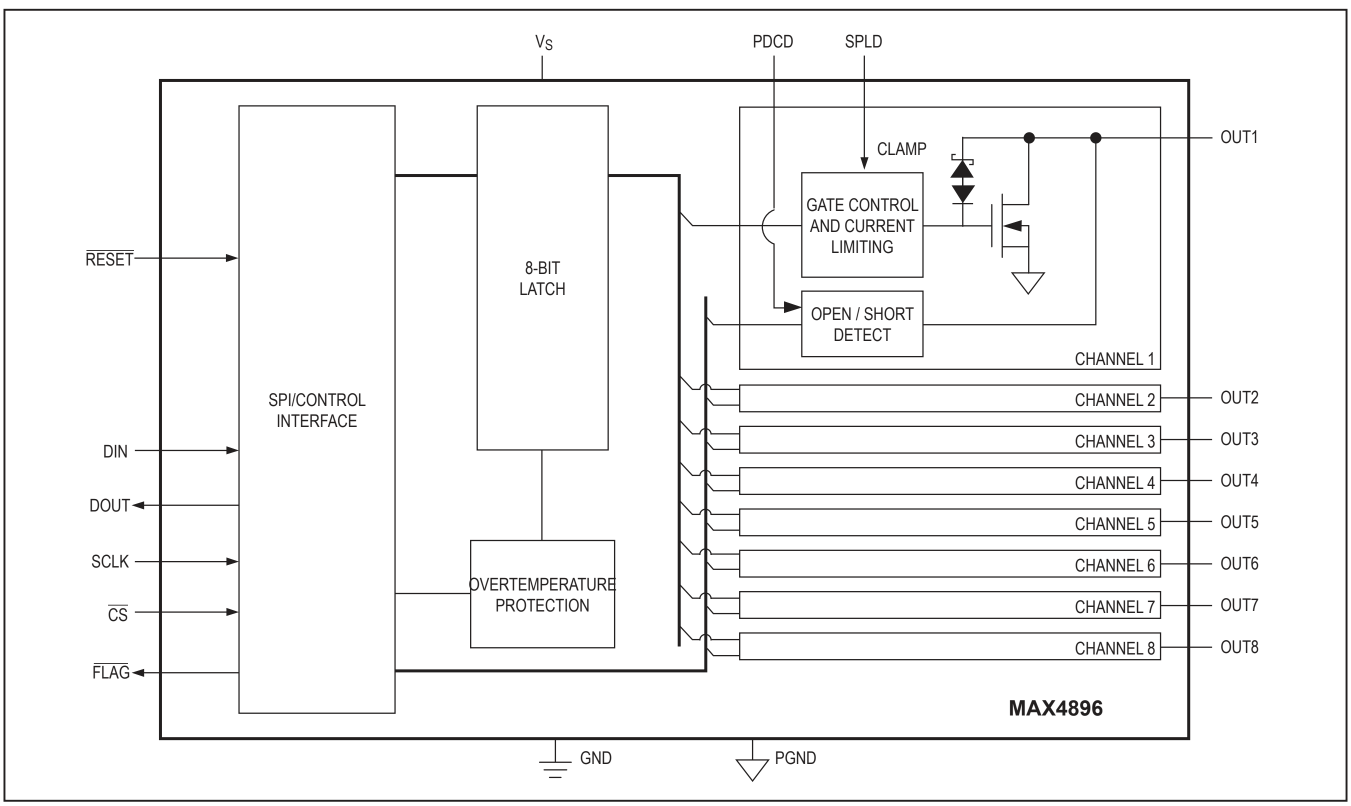
Pin Description

PIN	NAME	FUNCTION
1	RESET	Reset Input. Drive RESET low to clear all latches and registers (all outputs are turned off). All OUT pulldown currents are disabled when RESET = low.
2	CS	Chip Select Input. Drive CS low to select the device. When CS is low, data at DIN is clocked into the 8-bit shift register on SCLK's rising edge. Drive CS from low to high to latch the data to the registers.
3	DIN	Serial Data Input
4	SCLK	Serial Clock Input
5	DOUT	Serial Data Output. DOUT is the output of the 8-bit shift register. This output can be used to daisy chain multiple MAX4896s. The data at DOUT appears synchronous to SCLK's falling edge.
6	PDCD	Pulldown Current Disable. Drive PDCD high to disable OUT's pulldown current source. Drive PDCD low to enable OUT_ pulldown current source. PDCD must be low to detect an open-load fault.
7	SPLD	Short-Protection Latch-Off Disable Input. Drive SPLD high to disable the built-in short-circuit protection latch-off feature. When SPLD is low, an overloaded channel is turned off immediately. See the *Output Short-Circuit/Current-Limiting Protection* section.
8	OUT8	Open-Drain Output 8. Connect OUT8 to the low side of a relay coil. OUT8 is pulled to PGND when activated and is otherwise high impedance.
9	OUT7	Open-Drain Output 7. Connect OUT7 to the low side of a relay coil. OUT7 is pulled to PGND when activated and is otherwise high impedance.
10, 16	PGND	Power Ground. PGND is the ground return path for the output sinks. Connect PGND pins together and to GND.

Pin Description (continued)

11	OUT6	Open-Drain Output 6. Connect OUT6 to the low side of a relay coil. OUT6 is pulled to PGND when activated and is otherwise high impedance.
12	OUT5	Open-Drain Output 5. Connect OUT5 to the low side of a relay coil. OUT5 is pulled to PGND when activated and is otherwise high impedance.
13	GND	Ground
14	OUT4	Open-Drain Output 4. Connect OUT4 to the low side of a relay coil. OUT4 is pulled to PGND when activated and is otherwise high impedance.
15	OUT3	Open-Drain Output 3. Connect OUT3 to the low side of a relay coil. OUT3 is pulled to PGND when activated and is otherwise high impedance.
17	OUT2	Open-Drain Output 2. Connect OUT2 to the low side of a relay coil. OUT2 is pulled to PGND when activated and is otherwise high impedance.
18	OUT1	Open-Drain Output 1. Connect OUT1 to the low side of a relay coil. OUT1 is pulled to PGND when activated and is otherwise high impedance.
19	V_S	Input Supply Voltage. Bypass V_S to GND with a 0.1µF capacitor.
20	$\overline{FLAG}$	Open-Drain Fault Output. $\overline{FLAG}$ asserts low when a fault occurs at OUT1–OUT8.
—	EP	Exposed Paddle. Internally connected to GND. Connect to a large PCB ground plane to improve thermal dissipation. Enhances thermal conductivity; not intended as an electrical connection point.

Functional Diagram



Detailed Description

The MAX4896 is an 8-channel relay and load driver for medium voltage applications up to 50V. The MAX4896 features built-in inductive kickback protection, drive for latching/nonlatching, or dual-coil relays and an internal register for detecting open-load and short-circuit faults. Each independent open-drain output features a 3Ω on-resistance and is guaranteed to sink 400mA at $V_S \geq 4.5V$, and 100mA at $V_S \leq 3.6V$.

The MAX4896 also incorporates a logic input (SPLD) that allows the device to continue operating when an overcurrent condition lasts longer than the 280µs (max) fault delay time. A built-in overvoltage protection clamp handles kickback voltage transients, which are common when driving inductive loads. Thermal-shutdown circuitry shuts off all outputs (OUT_) when the junction temperature exceeds +160°C.

The MAX4896 employs a reset input that allows the user to turn off all outputs simultaneously with a single control line.

The MAX4896 includes a 10MHz SPI-/QSPI-/MICROWIRE compatible serial interface. The serial interface is compatible with TTL-/CMOS-logic voltage levels and operates with a single +2.7V to +5.5V supply.

Serial Interface

The serial interface consists of an 8-bit input shift register, a parallel latch (output control register) controlled by SCLK and $\overline{CS}$, and an output status register containing diagnostics information. The input to the shift register is an 8-bit word. Each data bit controls one of the eight outputs, with the most significant bit (D7) corresponding to OUT8, and the least significant bit (D0) corresponding to OUT1 (see Table 1). When $\overline{CS}$ is low, data at DIN is clocked into the shift register synchronously with SCLK's rising edge. Driving $\overline{CS}$ from low to high latches the data in the shift register to the output control register.

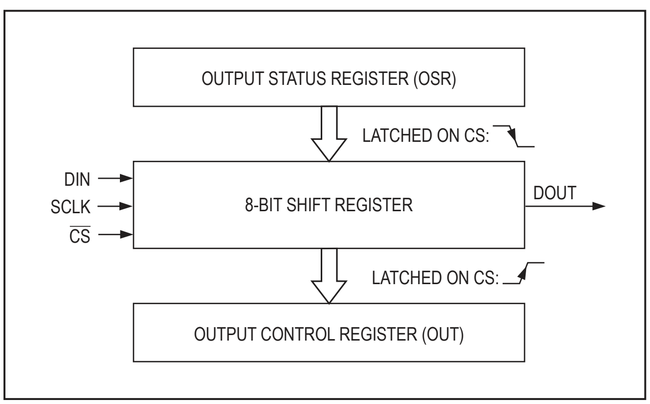


Figure 1. Serial Interface

DOUT is the output of the internal output status register for diagnostics purposes (see Figure 2 and Tables 2 and 3). Status data for each channel is transferred to the shift register at the falling edge of $\overline{CS}$. The data bits contained in the shift register are then transferred to the DOUT output synchronously with SCLK's falling edge.

While $\overline{CS}$ is low, the switches always remain in their previous states. Drive $\overline{CS}$ high after 8 bits of data have been shifted in to update the output state, and to further inhibit data from entering the shift register. When $\overline{CS}$ is high, transitions at DIN and SCLK have no effect on the output, and the first input bit (D7) is present at DOUT.

If the number of data bits entered while $\overline{CS}$ is low is greater or less than 8, the shift register contains only the last 8 data bits, regardless of when they were entered.

The 3-wire serial interface is compatible with SPI, QSPI, and MICROWIRE standards. The latch that drives the analog output stages is updated on the rising edge of $\overline{CS}$, regardless of SCLK's state.

Diagnostic Information

The MAX4896 contains an internal output status register used for diagnostics information for each output (see Tables 1, 2, and 3). When a fault condition is detected at any channel for longer than the minimum fault-filtering time ($t_{D(FAULT)\_min}$), the fault information is latched into the corresponding position in the output status register (see Table 2), and the $\overline{FLAG}$ asserts. Status/diagnostics data for each channel in the output status register is transferred to the output shift register at the falling edge of $\overline{CS}$. While $\overline{CS}$ is low, the diagnostics bits are then transferred to DOUT synchronously with SCLK's falling edge. A rising edge at $\overline{CS}$ resets the output status register data. During normal operation,the output status bit is the same as the DIN bit (DO1 = D1, DO2 = D2). When the MAX4896 is operating with a fault condition, the output status bit is the inverse of the DIN bit (DO1 = 0, D1 = 1).

Table 1. Serial-Input Address

DIN	D0	D1	D2	D3	D4	D5	D6	D7
OUT_	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	OUT7	OUT8

Table 2. Serial-Output Address

DIN	DO0	DO1	DO2	DO3	DO4	DO5	DO6	DO7
OUT_	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	OUT7	OUT8

Table 3. Status-Register Output Diagnostic

OUTPUT STATUS	DO_STATUS BIT	DIAGNOSTIC
Off	Low	Normal operation.
Off	High	Fault condition. Output open or short circuit.
On	Low	Fault condition. Short circuit to positive load voltage.
On	High	Normal operation.

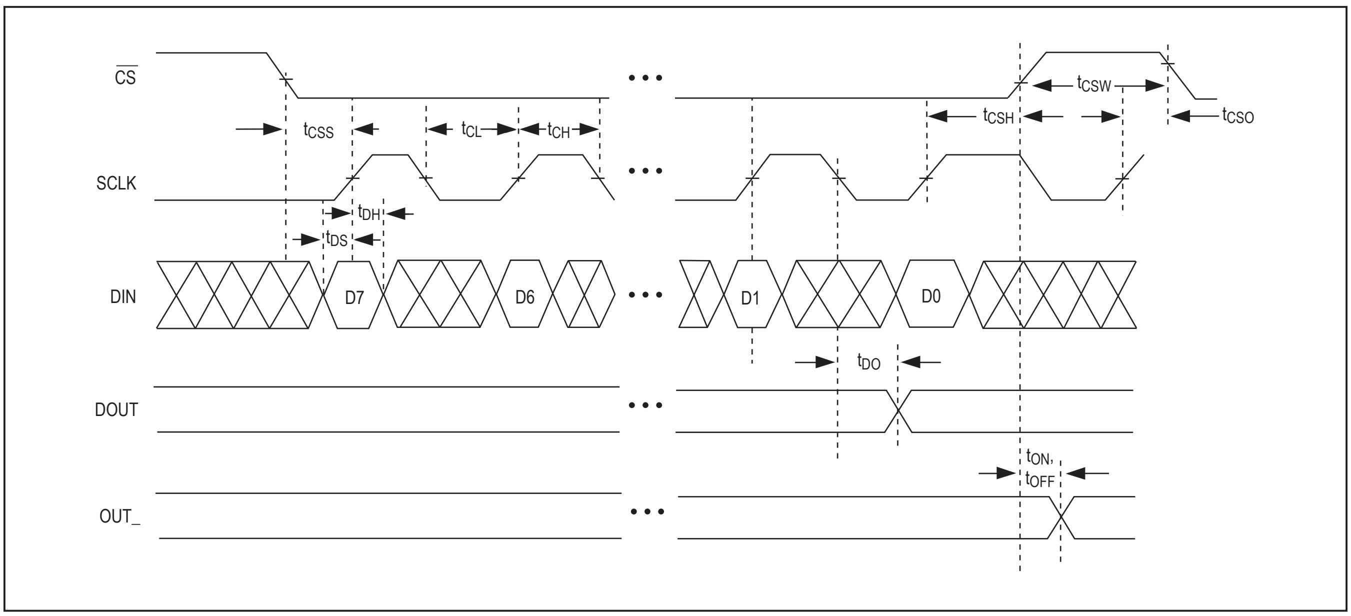


Figure 2. 3-Wire Serial-Interface Timing

The minimum fault-filtering time helps mask short-duration fault conditions, such as driving highly capacitive loads.

The typical diagnostics software routine works as follows:

- Write data to the MAX4896
- Wait for t_D(FAULT) maximum to ensure diagnostics data is ready and valid
- Write same data to the MAX4896 and read out the diagnostics data from the shift register

Use Table 3 to diagnose the output state.

To reduce processor overhead, an interrupt-based diagnostics routine is possible. The diagnostics routine will analyze diagnostics data only when the $\overline{FLAG}$ output triggers an interrupt.

Output Short-Circuit/ Current-Limiting Protection

The MAX4896 channels (OUT_) are protected against short-circuits conditions. When the channel's output current exceeds the current-limit threshold (I_{LIM}) for longer than the minimum fault-filtering time ($t_{D(FAULT)}$ min), the short-circuit protection is activated. The short-circuit protection behavior is determined by the logic level at SPLD. When SPLD = high, an overloaded channel remains in a current-limited state until the short-circuit condition is removed or thermal shutdown is reached. This allows the operation of loads where the inrush currents may exceed the MAX4896 internal current limit.

When SPLD = low, an overloaded channel immediately turns off (latched-off). When a shorted output is latched off, the channel can be turned back on after the next serial input data is latched into the MAX4896. If the short-circuit condition is still applied to the output channel after the new bitstream is clocked into the MAX4986, the $\overline{FLAG}$ pin returns high and remains high for the fault filtering time before asserting low again.

Open-Load Detection

The MAX4896 features an output pulldown current source, along with a voltage comparator, to detect an open-load fault condition. To enable the open-load detection function, PDCD must be low. The voltage at OUT_ is compared with the diagnostics threshold voltage ($V_{DS(OL)}$) to determine whether a open-load fault condition exists. Open-load detection only works when the output channel is turned off.

Thermal Shutdown

If the junction temperature exceeds +160°C, all outputs are switched off immediately (no filtering time) and $\overline{FLAG}$ asserts. The hysteresis is approximately +20°C, disabling thermal shutdown once the temperature drops below +140°C.

$\overline{RESET}$

The MAX4896 features an asynchronous reset input that allows the user to simultaneously turn all outputs off using a single control line. Drive $\overline{RESET}$ low to clear all latches and registers, and to turn off all outputs. While $\overline{RESET}$ is low, the OUT pulldown currents are disabled, regardless of the state of PDCD.

$\overline{FLAG}$ Output

$\overline{FLAG}$ is an open-drain latched output that can be connected to a µP interrupt and pulls low whenever a fault condition (short-circuit and/or open-load) is detected in any of the eight outputs for longer than the minimum fault-filtering time ($t_{D(FAULT)}$ min). When not using all channels, connect each unused output to V_S through a 10kΩ pullup resistor to avoid inadvertently triggering the $\overline{FLAG}$. $\overline{FLAG}$ asserts immediately, (no filtering time), when a thermal-shutdown fault condition is detected. The latch $\overline{FLAG}$ deasserts on $\overline{CS}$ rising edge.

Applications Information

Daisy Chaining

The MAX4896 features a digital output (DOUT) that provides a simple way to daisy chain multiple devices. This feature allows the user to drive large banks of relays using only a single serial interface. To daisy chain multiple devices, connect all $\overline{CS}$ inputs together and connect the DOUT of one device to the DIN of another device (see Figure 3). During operation, a stream of serial data is shifted through all the MAX4896s in series.

Inductive Kickback Protection

Each output features an output protection clamp, limiting the OUT voltage to 65V (typ). The clamp protects against voltage transient when driving inductive loads.

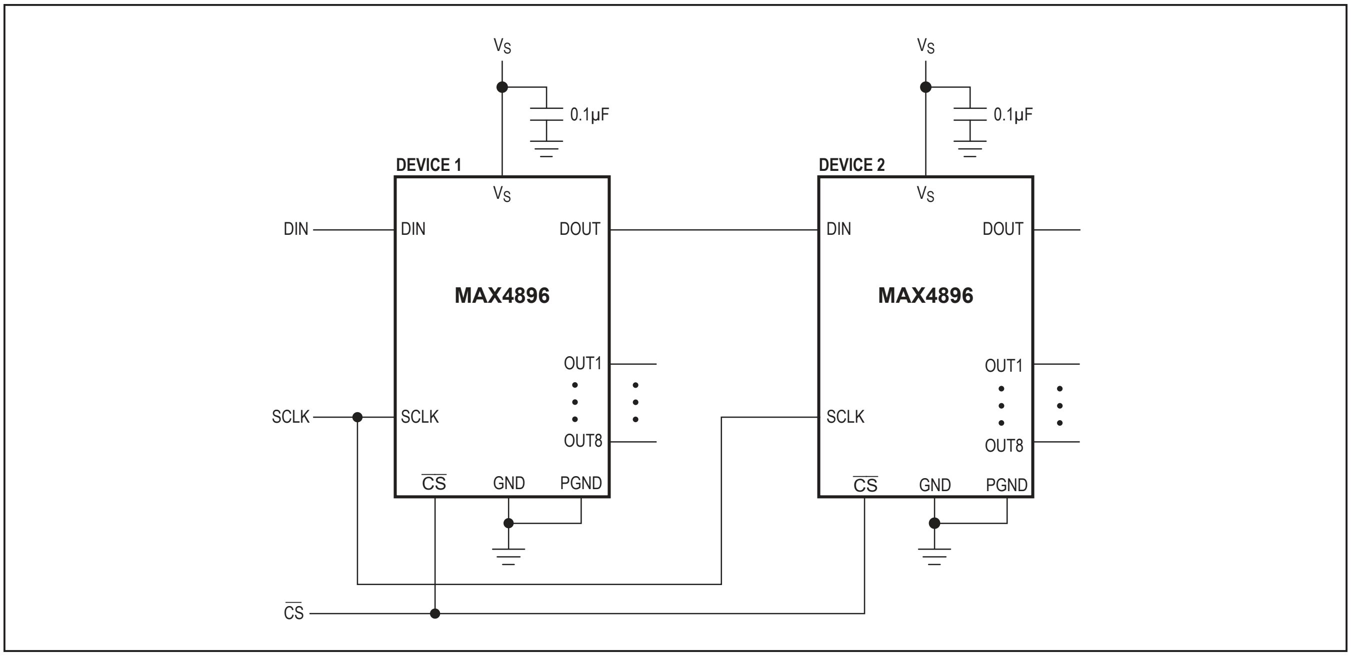


Figure 3. Daisy-Chain Configuration

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX4896ATP+	-40°C to +125°C	20 TQFN-EP* (5mm x 5mm)
MAX4896ETP+	-40°C to +85°C	20 TQFN-EP* (5mm x 5mm)

**EP = Exposed pad.*
+Denotes lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/05	Initial release	—
1	6/07	Removal of future product notice	-
2	12/07	EP clarification	7
3	7/12	Updated $\overline{FLAG}$ *Output* section	10
4	5/14	Removed automotive reference under *Applications* section	1
5	1/20	Updated the *General Description, Benefits and Features, Typical Operating Circuit, Pin Description, Detailed Description, Output Short-Circuit/Current-Limiting Protection, Open-Load Detection,* and $\overline{FLAG}$ *Output* sections, and Figure 3	1, 7–8, 10–11

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at https://www.maximintegrated.com/en/storefront/storefront.html.