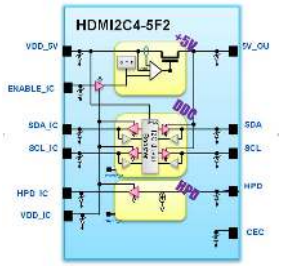
HDMI2C4-5F2

Datasheet

ESD protection and signal booster for HDMI™ source control stage interface

WLCSP (12 bumps) package



Product status link
HDMI2C4-5F2

Features

- For HDMI™ 1.4, 2.0 & 2.1 application, operating temperature from -40 to 85 °C
- 8 kV contact ESD protection on connector side (IEC 61000-4-2 level 4)
- DDC (I2C) buffers with level shifter and backdrive protection
- High integration level in 1 package
- DDC (I2C) link protection, bi-directional signal conditioning circuit and dynamic pull-up
- HPD pull down, signal conditioning with level shifter and backdrive protection
- Enable function available for power consumption control and optimization (=ENABLE_IC)
- 325 mA Short-circuit protection on 5V output with backdrive protection
- Proposed in 500 µm pitch WLCSP package 12 bumps

Benefits

- Minimal PCB footprint in tablet, set top box, game console and other consumer application
- Protection of ultra-sensitive HDMI™ ASICs
- Ultra low power consumption in stand-by mode thanks to Enable function
- Improved HDMI™ interface ruggedness and user experience
- Long and/or poor quality cable support with dynamic pull-up on DDC bus

Complies with the following standards

- Dedicated for HDMI™ 1.4, 2.0 and 2.1 version
- IEC 61000-4-2 level 4
- JESD22-A114D level 2

Applications

Consumer and computer electronics HDMI™ Source device such as:

- Tablet and smartphone
- HD set-top boxes
- Game console
- DVD and Blu-Ray Disk systems
- Notebook
- PC graphic cards

Description

The HDMI2C4-5F2 is an integrated ESD protection and signal conditioning device for control links of HDMI™ transmitters (Source).

This device is a simple solution that provides HDMI™ designers with an easy and fast way to reach full compliance with the stringent HDMI™ CTS on a wide temperature range.

1 Functional description

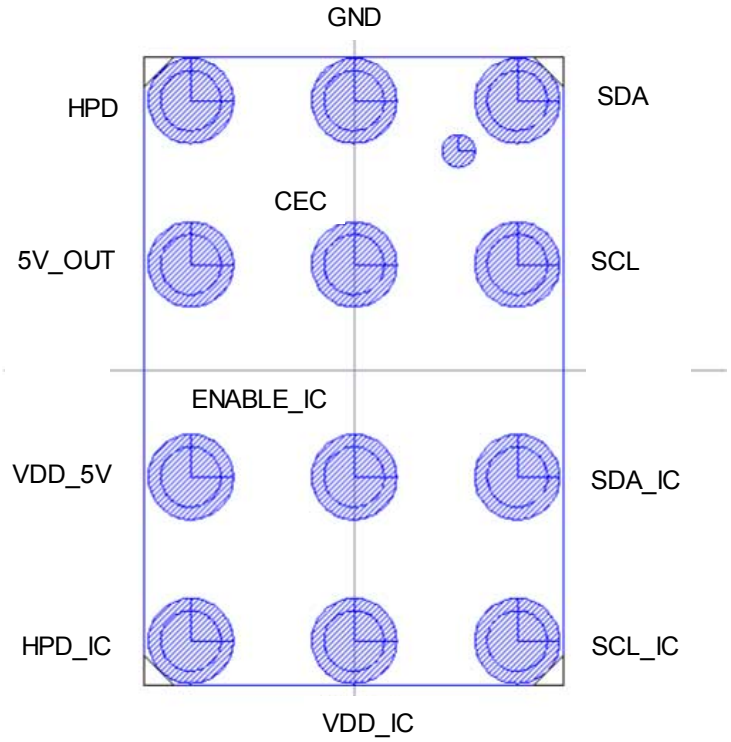
The HDMI2C4-5F2 is a fully integrated ESD protection and signal conditioning device for control stage of HDMI™ transmitters (Source).

The component offers two buffers, integrating signal conditioning dynamic pull-up on DDC bus for maximum system robustness and signal integrity. These buffers embed also a protection to prevent from connector backdrive current when the ENABLE_IC input is low. This component is compliant with clock stretching mode.

The +5 V supplied to the cable is protect against accidental surge current and short circuit. Enable function is available to allow power consumption control and to prevent from connector backdrive current. All these features are provided in a single 12 bumps WLCSP package featuring natural PCB routing, cost optimization and saving space on the board.

The HDMI2C4-5F2 is a simple solution that provides HDMI™ designers with an easy and fast way to reach full compliance with the stringent HDMI™ CTS on a wide temperature range. STMicroelectronics proposes also a large range of high speed ESD protections and common mode filter (ECMF™ series) dedicated to the TMDS lanes giving the flexibility to the designer to filter and protect these (high speed video link against ESD strikes and EMC issues).

Figure 1. Pin configuration (bump side)



2 Application information

2.1 DDC bus description

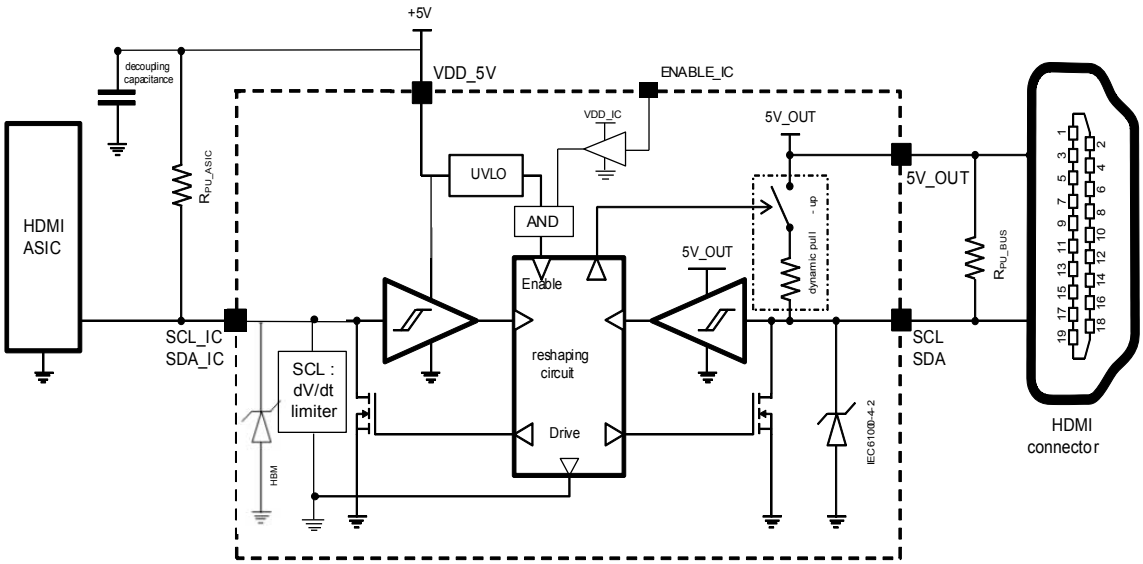
The DDC bus is described in the HDMI™ standards as the display data channel. The topology corresponds to an I2C bus that must be compliant with the I2C bus specification UM10204 revision 5 (October 2012). The DDC bus is made of 2 lines; data line (SDA) and clock line (SCL). It is used to create a point to point communication link from the source to the sink. EEDID and HDCP protocols are especially flowing through this link, making this I2C communication channel a key element in the HDMI™ application.

The DDC block integrated in the HDMI2C4-5F2 allows a bidirectional communication between the cable and the ASIC. It is fully compliant with the HDMI™ 2.0 standard (I2C bus specification) and its CTS. It is shifting the 5 V voltage from the cable (V_{5V_OUT}) down to the ASIC voltage level (V_{DD_IC}) that can be as low as 1.8 V.

During clock stretching operation, when the sink pulls-down the bus, thanks to the comparator and level shifter, the ASIC input is pulled-down to avoid any glitch.

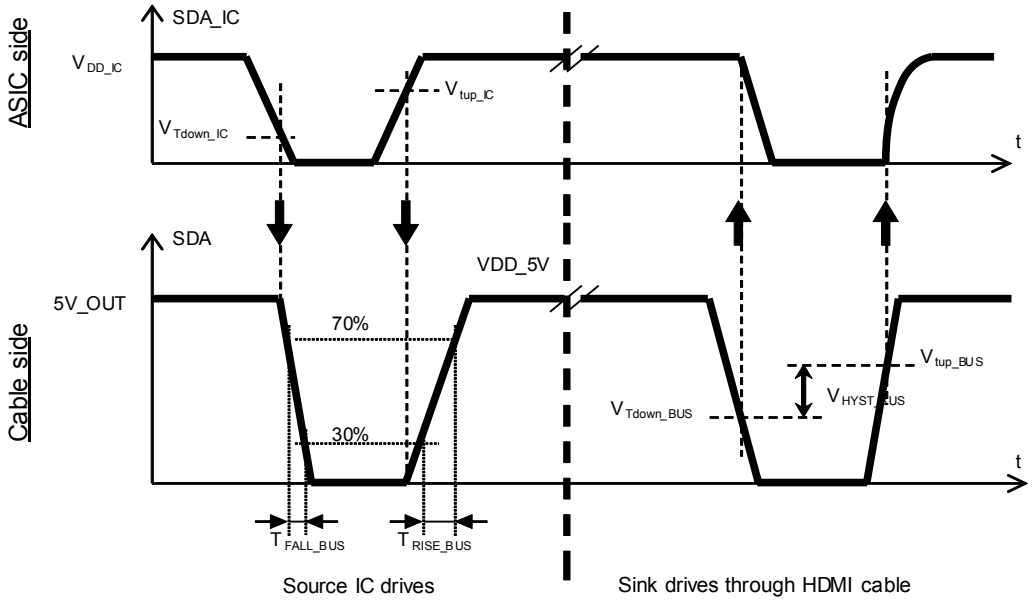
The Figure 2. shows the functional diagram of the DDC block integrated in the HDMI2C4-5F2 device.

Figure 2. DDC buffer functional diagram (SCL and SDA lines)



The Figure 3. illustrates the electrical parameter of the DDC block specified by the Table 8..

Figure 3. Simplified view of the electrical parameters of the SDA level shifter

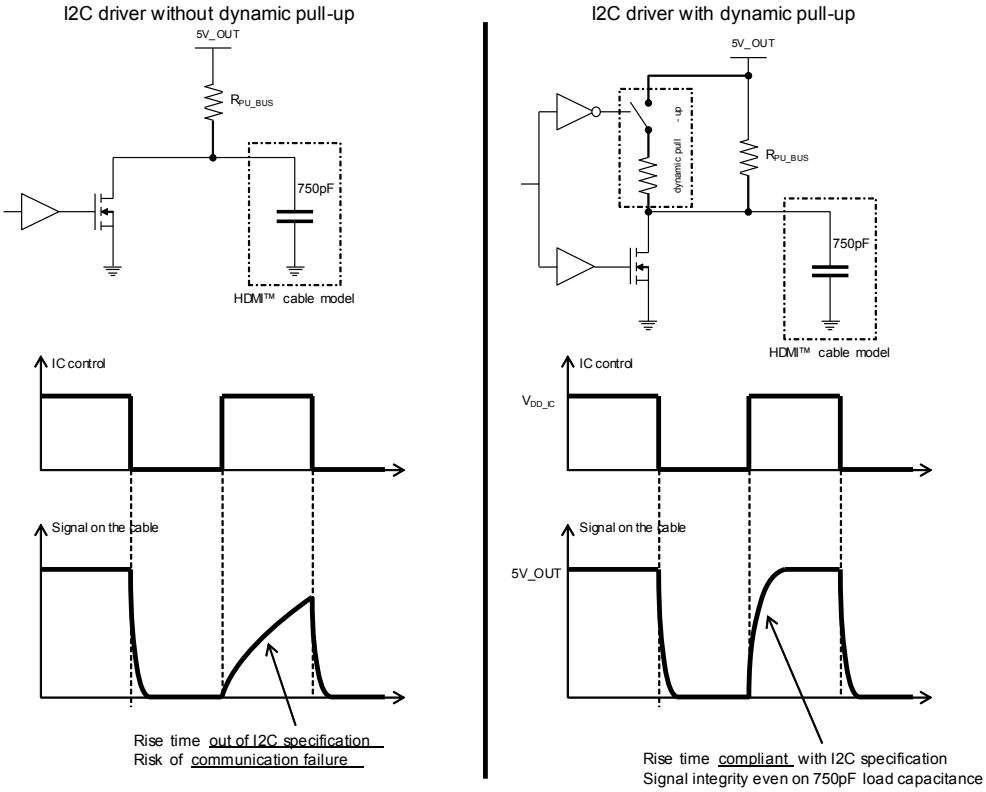


Capacitance measured at the HDMI connector output is equal to the sum of HDMI2C4-5F2 capacitance plus bus capacitance between HDMI2C4-5F2 and HDMI connector output. Thanks to the internal structure of the integrated DDC block, measured capacitance is equal to the input capacitance and then independent from the IC actual capacitance. For compliance test, capacitance on DDC bus must be measured with HDMI2C4-5F2 powered on.

The HDMI™ standard specifies that the max capacitance of the cable can reach up to 700 pF. Knowing that the max capacitance of the sink input can reach up to 50 pF, this means that the I2C buffer must be able to drive a load capacitance up to 750 pF. On the other hand, the I2C standard specifies a maximum rise time (30%-70%) of the signal must be lower than 1 µs in order to keep the signal integrity. Taking into account the max cable capacitance of 750 pF, it is not possible to guarantee a rise time lower than 1µs in worst case.

Therefore, a dynamic pull-up has been integrated at the output of SDA and SCL lines and synchronized with the I2C driver. This signal booster accelerates for a short period the charging time of the equivalent cable capacitance, allowing driving any HDMI™ cable. The Figure 4. illustrates the benefit of the dynamic pull-up integrated in the HDMI2C4-5F2 device.

Figure 4. Benefit of the dynamic pull-up on the DDC bus



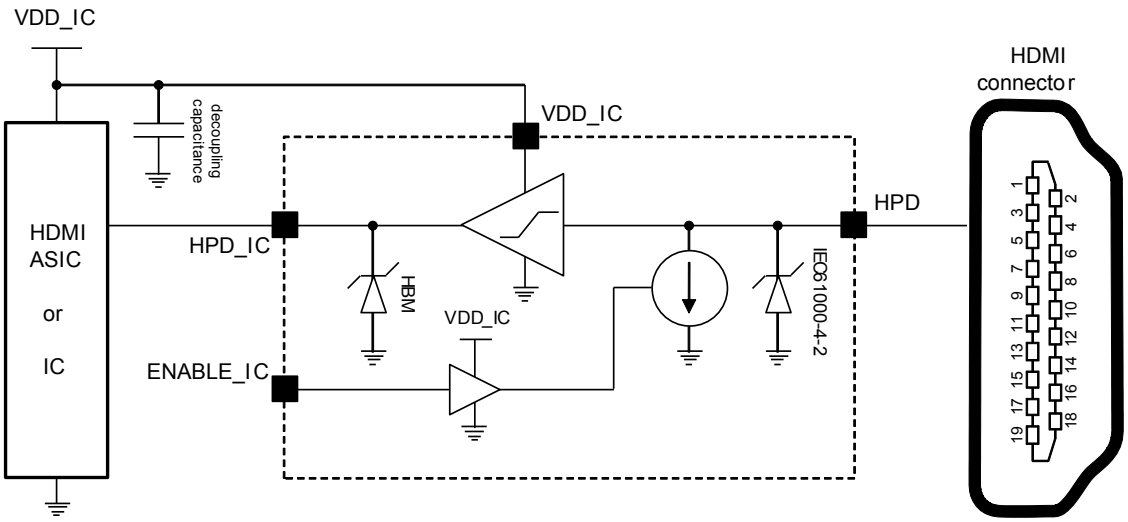
Before activating the DDC buffers, three following conditions must be respected:

- V_{DD_5V} must be higher than the V_{DD_ON} threshold (Table 4.)
- ENABLE_IC input must be set to a high level
- All inputs and outputs (SDA, SCL, SDA_IC, SCL_IC) must be set to a high level at the same time as well as HPD input
- The DDC outputs (SCL and SDA on cable side) integrate a protection against ESD which is compliant with -IEC61000-4-2 standard, level 4 (8 kV contact).

2.2 HDP line description

The HDMI2C4-5F2 proposes a unique solution to manage and to protect HPD link. The Figure 5. shows an overview of the function diagram of the integrated block.

Figure 5. HPD line functional diagram



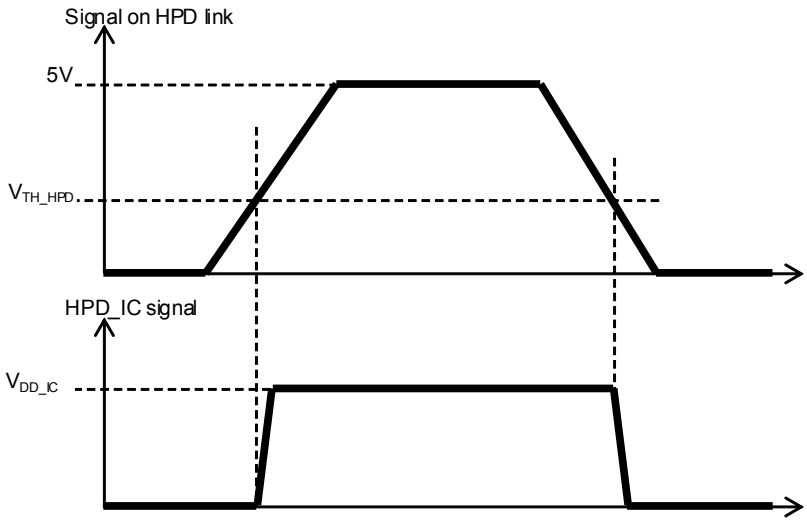
Simply connect the PIN3 of the HDMI™ connector to one side of the device, and then use the HPD_IC and VDD_IC outputs on the other side of the device to manage HPD link.

HPD input (cable side) integrates a protection against ESD which is compliant with IEC61000-4-2 standard, level 4 (8 kV contact).

When the ENABLE_IC input is set at a low level, the HPD is not pulled down and the HPD_IC output is forced at a low level.

The integrated HPD block is pulling down the line via a current source. When the input voltage is detected to be higher than a threshold level, the signal is converted into a high state level on the ASIC side, at the voltage level of the ASIC power supply-VDD_IC. The electrical parameters relevant to the HPD block and specified by the Table 7. are shown by the Figure 6..

Figure 6. **Simplified view of the electrical parameters of the HPD block**



2.3 +5 V protection

The +5 V power supply that the source device has to provide to the HDMI™ cable is described by the HDMI™ standard. It must be protected against accidental short circuit that could occur on the cable side.

The HDMI2C4-5F2 device embeds a low drop current limiter. If an overcurrent is detected, the HDMI2C4-5F2 limits the current through the +5 V power supply. If the current is too high (short circuit), the device opens the +5V.

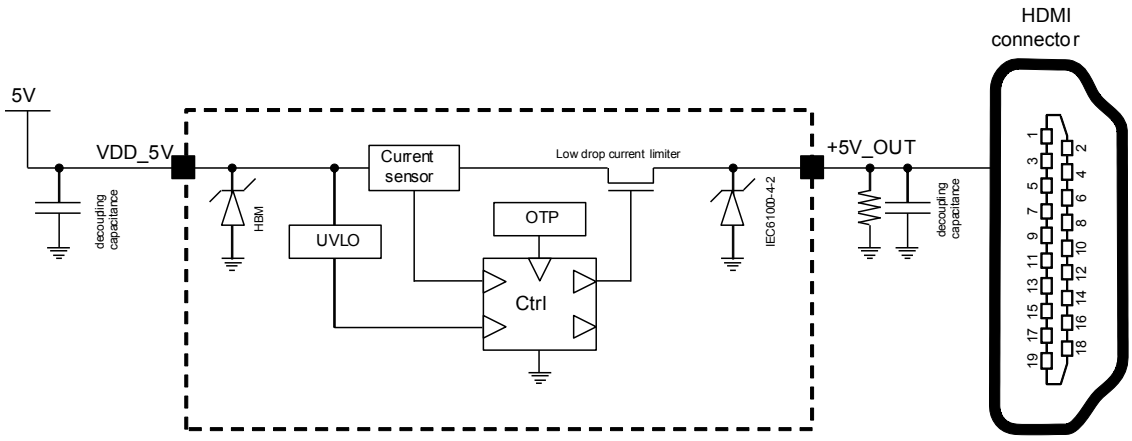
Furthermore, the HDMI2C4-5F2 device embeds also an over temperature protection (OTP). If the internal temperature of the device is reaching a too high value, the +5 V supply is opened in order to protect the application.

An under voltage lockout (UVLO) is also integrated in the block. It checks the main +5 V power supply state, and enable the +5V_OUT only if the main power supply has reach a minimal value $V_{DD\_5V\_ON}$.

When the ENABLE_IC input is set at a low level, the 5 V supply is opened to prevent from connector backdrive current.

The Figure 7. shows the functional diagram of the current limiter block.

Figure 7. **5 V link functional diagram**



To summarize, the short circuit protection and the over temperature protection features are providing a high robustness level of the application.

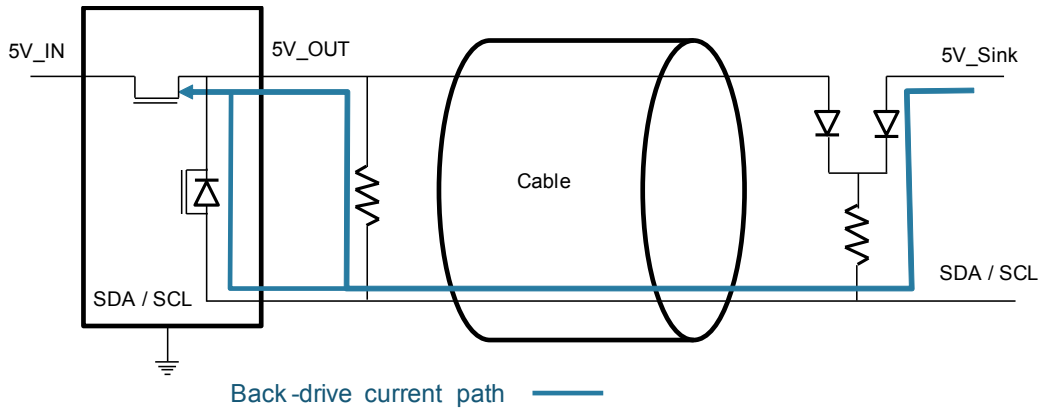
The 5V_OUT pin integrates also a protection against ESD which is compliant with IEC61000-4-2 standard, level 4 (8 kV contact). The decoupling capacitance is mandatory accordingly to the power management state of the art.

The OUT_5V pin is pulled down when EN = 0 or V_{DD_5V} < UVLO threshold level.

2.4 Backdrive protection

Thanks to the innovative switch architecture, when the ENABLE_IC input is set at a low level, backdrive current is blocked whatever backdrive current is coming from +5V_OUT and/or DDC lines (see Figure 8.). Back-drive function is activated as soon as UVLO function is turned ON.

Figure 8. Backdrive current diagram



2.5 Enable function

Enable function is available to allow user control to switch on or switch off the device even if V_{DD_5V} and V_{DD_IC} are supplied. When the device is disabled, 5V_OUT output is pulled-down by an internal 1.4 kΩ resistor.

2.6 Application block diagrams

The Figure 9. shows an application block diagram proposal, with all possible options implemented. Thanks to ENABLE_IC signal control, the designer has then the tools to optimize the power consumption of the global application with a stand-by mode.

Figure 9. Application block diagram

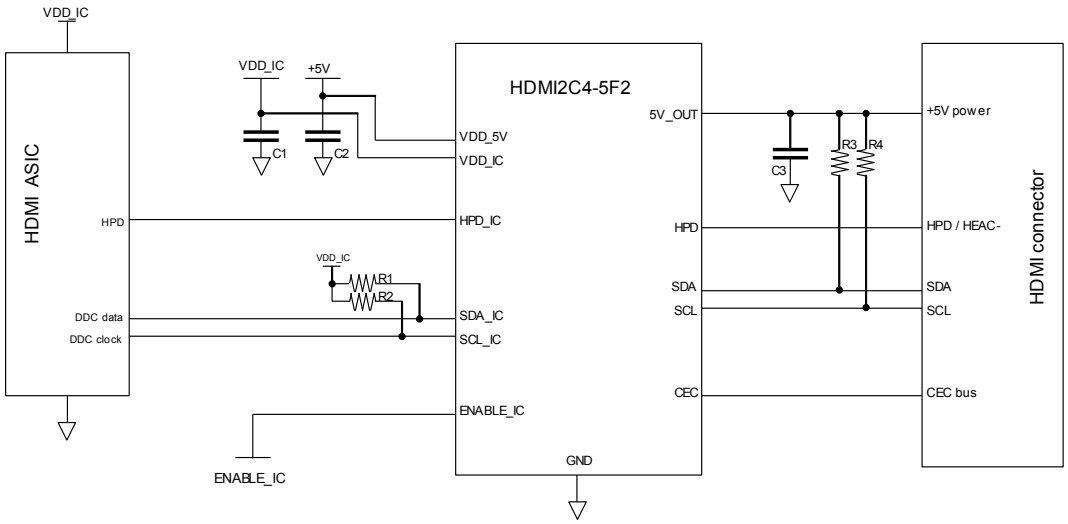


Table 1. External component recommendations

Ref.	Typical value	Comment
R1 and R2	10 kΩ	Pull-up resistance on DDC bus, ASIC side, value selected to be compliant with I2C levels.
C1 and C2	100 nF	Decoupling capacitance on power supplies.
R3 and R4	1.8 kΩ	Pull-up resistances on DDC bus, specified by the HDMI™ standard.
C3	1 µF, 10 V minimum, -10 % tolerance	ESD (low ESR) decoupling capacitance.

Note: SCL_IC, SDA_IC have to be driven with an ASIC working with open drain outputs.

Figure 10. **Pin numbering (bump side)**

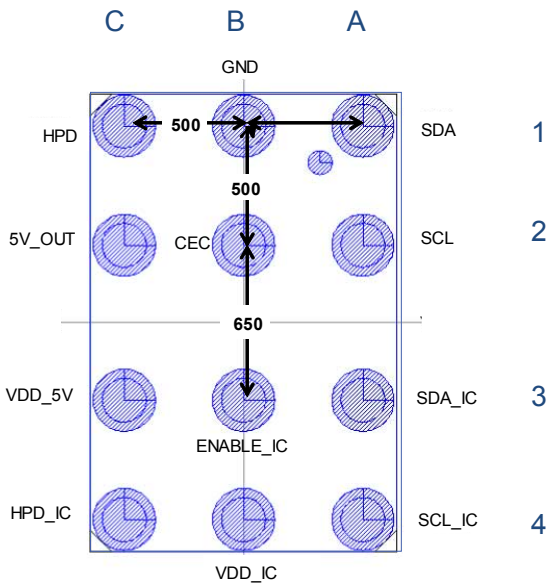


Table 2. **Pin numbering and description**

Pin	Name	Description	Pin	Name	Description
A1	SDA	DDC output HDMI cable side	A3	SDA_IC	DDC input ASIC side
B1	GND	Ground	B3	ENABLE_IC	Enable all functions
C1	HPD	HPD - input HDMI cable side	C3	VDD_5V	+5 V main power supply
A2	SCL	DDC output HDMI cable side	A4	SCL_IC	DDC input ASIC side
B2	CEC	CEC output HDMI cable side	B4	VDD_IC	HDMI ASIC power supply
C2	5V_OUT	+5 V power supply HDMI cable side	C4	HPD_IC	HPD output ASIC side

3 Electrical characteristics

Table 3. Absolute maximum ratings (limiting values)

Symbol	Parameter	Test conditions	Value	Unit
V_{PP_BUS}	ESD discharge on HDMI cable side (pins A1, C1, A2, B2 and C2) IEC 61000-4-2 level 4	Contact discharge	±8(1)	kV
		Air discharge	±15	
V_{PP_IC}	ESD discharge (all pins) HBM -JESD22-A114D, level 2	Contact discharge	±2	kV
		Air discharge	±2	
T_{STG}	Storage temperature range		-55 to +150	°C
T_{OP}	Operating temperature range		-40 to +85	°C
T_L	Maximum lead temperature		260	°C
V_{DD_5V}, V_{DD_IC}	Supply voltages		6	V
Inputs	Logical input min / max voltage range		-0.3 to 6	V

1. *With a 1 µF low ESR capacitor connected to the 5V_OUT pin*

Table 4. Power supply characteristics (T_{amb} = 25 °C)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
V_{DD_IC}	Low-voltage ASIC/HPD supply voltage		1.62		5.3	V
V_{DD_5V}	5 V input supply voltage range		4.9	5.0	5.3	V
$V_{DD\_5V\_ON}$(1)	+5 V power on reset		3.5	3.8	4.1	V
I_{QS_5V}	Quiescent currents on V_{DD_5V}, V_{DD_IC}	V_{DD_IC} = 5 V, V_{DD_IC} = 1.8 V, idle-state on DDC links, HPD and 5V_OUT links open, -ENABLE_IC = 1.8 V			700	µA
I_{QS_IC}					60	µA
T_{SD}	Thermal Shutdown threshold		120		150	°C

1. *In order to activate the DDC lines, the V_{DD_5V} has to reach the V_{DD_ON} threshold. The inputs and outputs of the bidirectional level shifters must be set to a high level after the power-on, and the HPD line has to be activated one time.*

Table 5. HDMI 5V_OUT current limiter electrical characteristics (T_{amb} = 25 °C, V_{DD_5V} = 5 V, unless otherwise specified)

Pin number	Description	Test conditions	Value			Unit
			Min.	Typ.	Max.	
R_{Pull_down}(1)	Output pull down resistor on 5V_OUT when the circuit is disabled	V_{DD_5V} = 5 V, V_{DD_IC} = 1.8 V Idle-state on DDC links, HPD and 5V_OUT links open, ENABLE_IC = 0 V	1.1	1.4	1.7	kΩ
V_{DROP}	Drop-out voltage	I_{5V_OUT} = 250 mA	42	79	125	mV

Pin number	Description	Test conditions	Value			Unit
			Min.	Typ.	Max.	
I_{DC_MAX}[1]	Max DC current on 5V_OUT pin without OCP or OTP activation		250			mA
I_{5V_OCP}[1]	Over current protection on 5V_OUT pin	V_{5V_OUT} = 0 V	250	325	400	mA

1. *for T_{amb} from -40 °C to +85 °C*

Table 6. Enable electrical characteristics (T_{amb} = 25 °C, V_{DD_5V} = 5 V, unless otherwise specified)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
I_{LEAK}	Backdrive current for 5_{V_OUT}, SDA, SCL, HPD	ENABLE_IC=0 V_{DD_5V} = 0 V, V_{DD_IC} = 0 V, Tested pin = 5 V			1	µA
$I_{QS\_5V\_OFF}$	Quiescent currents on V_{DD_5V}, V_{DD_IC}	V_{DD_5V} = 5 V, V_{DD_IC} = 1.8 V, SCL, SCL_IC, SDA, SDA_IC, HPD = V_{DD_IC} and ENABLE_IC = 0 V			95	µA
$I_{QS\_IC\_OFF}$					1	µA
V_{TH_EN} / V_{DD_IC}	Enable input threshold level	V_{DD_IC} = 1.8 V	30	50	70	%
t_{ON}	Turn on time	V_{DD_5V} = 5 V, C_L = 1 µF and R_L = 100 Ω, see Figure 11 and Figure 12	10	50	100	µs
t_{OFF}	Turn off time	V_{DD_5V} = 5 V, C_L = 1 µF and R_L = 100 Ω, see Figure 11. and Figure 12.	50	250	500	µs

Figure 11. Output rise and fall test load

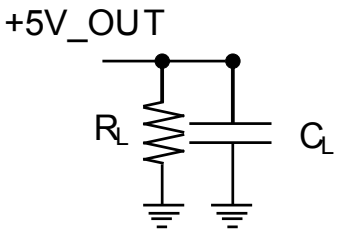


Figure 12. **Enable time**

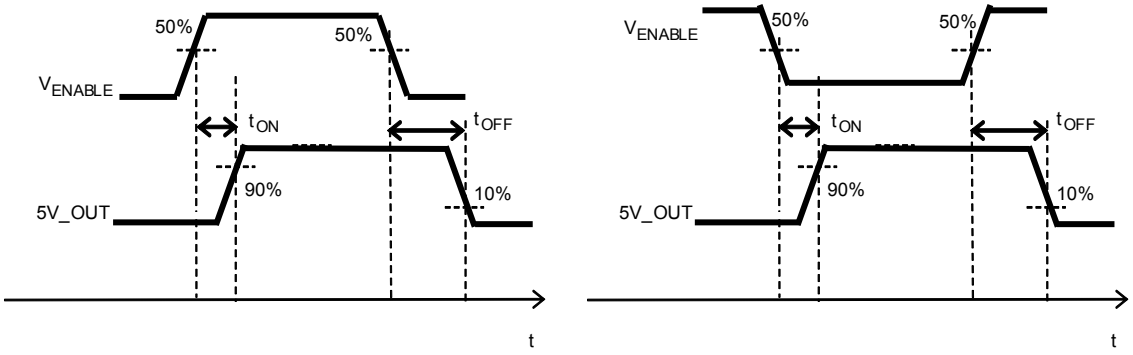


Table 7. **HPD line electrical characteristics (T_{amb} = 25 °C, V_{DD_5V} = 5 V, unless otherwise specified)**

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
I_{PULL_DOWN}	Pull-down current in HPD block			15	25	µA
V_{TH_HPD}	HPD input low-level		1.0		1.7	V
C_{IN_HPD}	Input capacitance	V_{DD_5V} = 0 V, V_{BIAS} = 0 V, f = 1 MHz, V_{OSC} = 30 mV		21	25	pF
$V_{OL\_HPD\_IC}$	HPD_IC output low-level	Current sunk by H_{PD_IC} pin is 500 µA			15	%V_{DD_IC}
$V_{OH\_HPD\_IC}$	HPD_IC output high-level	Current sourced by H_{PD_IC} pin is 500 µA	80			%V_{DD_IC}

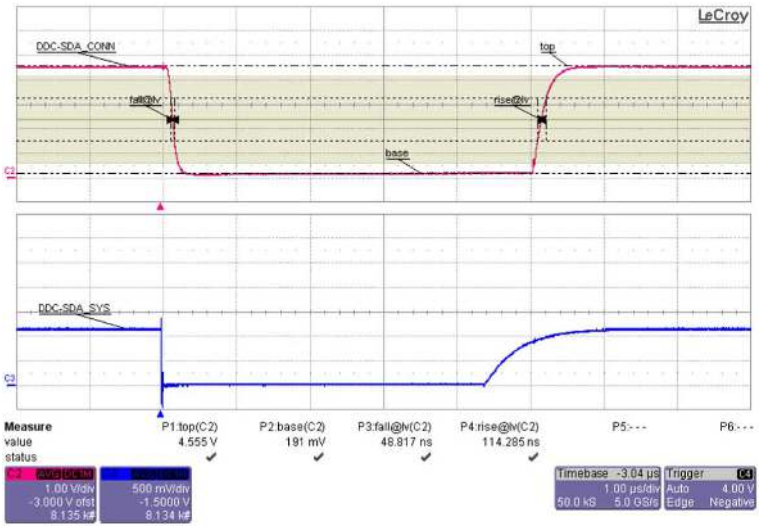
Table 8. **SDA line electrical characteristics (T_{amb} = 25 °C, V_{DD_5V} = 5 V, V_{DD_IC} = 1.8 V, unless otherwise specified)**

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
V_{Tup_BUS}	Upward input voltage threshold on bus side	V_{DD_5V} = 5 V			3.5	V
V_{Tdown_BUS}	Downward input voltage threshold on bus side	V_{DD_5V} = 5 V	1.5			V
V_{HYST_BUS}	Input hysteresis on bus side	V_{DD_5V} = 5 V	1.0		1.3	V
V_{OL_BUS}	Output low level	Current sunk by SDA pin is 3 mA			0.35	V
T_{RISE_BUS}	Output rise-time (30%-70%)	C_{BUS} = 750 pF(1), R_{UP} = 2 kΩ // 47 kΩ + 10 % (2)			500	ns
T_{FALL_BUS}	Output fall-time (70%-30%)				200	ns
V_{Tup_IC}	Upward input voltage threshold on IC side		55	60	65	%V_{DD_IC}

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
V_{Tdown_IC}	Downward input voltage threshold on IC side		35	40	45	$\%V_{DD\_IC}$
V_{OL_IC}	Output low-level on IC side	Current sunk by S_{DA_IC} pin is 3 mA			20	$\%V_{DD\_IC}$
C_{IN_DDC}	Input capacitance on DDC link	V_{DD_5V} = 0 V, V_{DD_IC} = 0 V, V_{BIAS} = 0 V, f = 1 MHz, V_{OSC} = 30 mV		25	30(3)	pF

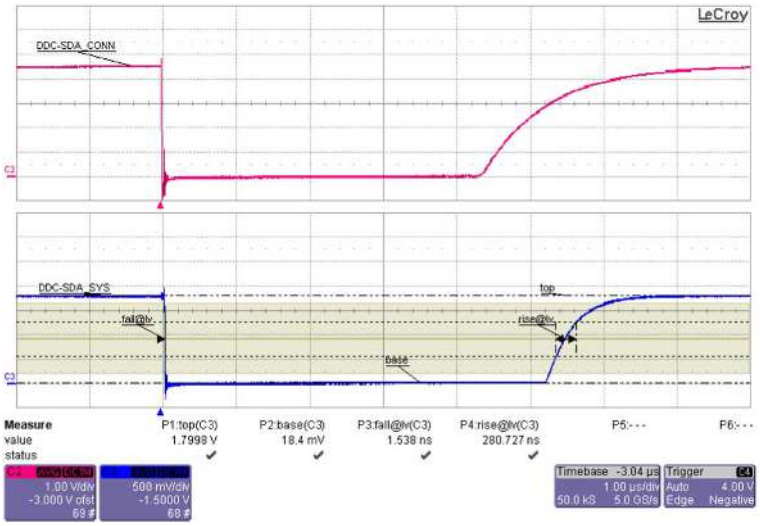
1. *Maximum load capacitance allowed on I2C entire link (cable plus connector) is 750 pF in HDMI™ 1.4 specification.*
2. *Two pull-up resistors in parallel (sink+source). Typical value is 47kΩ and maximum value is 47kΩ +10% in HDMI 1.4 specification.*
3. *Maximum capacitance allowed at connector output is 50 pF in HDMI™ 1.4 specification.*

Figure 13. SDA typical waveforms (IC to cable communication)



Note: Measurements performed with 750 pF load, C_{SYSTEM} = 15 pF and V_{DD_IC} = 1.8 V

Figure 14. SDA typical waveforms (Cable to IC communication)



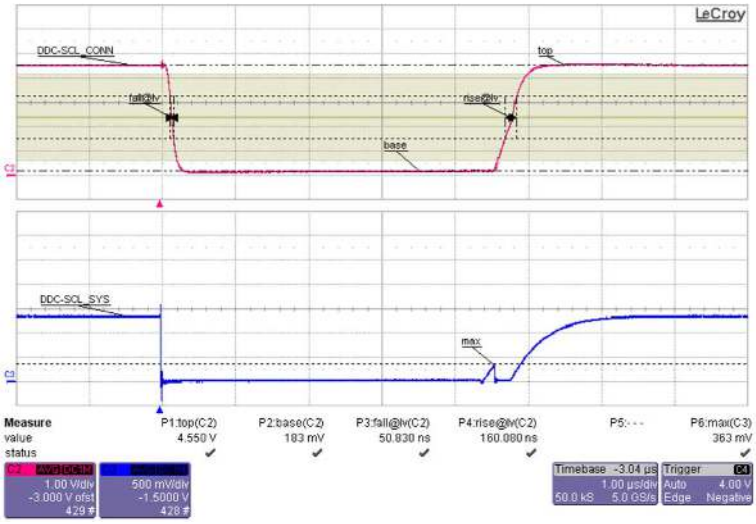
Note: Measurements performed with 750 pF load, C_{SYSTEM} = 15 pF and V_{DD_IC} = 1.8 V

Table 9. SCL line electrical characteristics (T_{amb} = 25 °C, V_{DD_5V} = 5 V, V_{DD_IC} = 1.8 V, unless otherwise specified)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
V_{TH_BUS}	Input voltage threshold on bus side	V_{DD_5V} = 5 V	1.5	2.0	2.5	V
V_{OL_BUS}	Output low level	Current sunk by SCL pin is 3 mA			0.35	V
T_{RISE_BUS}	Output rise-time (30%-70%)	C_{BUS} = 750 pF(1) R_{UP} = 2 kΩ // 47 kΩ + 10% (2)			500	ns
T_{FALL_BUS}	Output fall-time (70%-30%)				200	ns
V_{TH_IC}	Input voltage threshold on IC side		24		30	%V_{DD_IC}
V_{OL_IC}	Output low-level on IC side	Current sunk by SCL_IC pin is 3 mA			20	%V_{DD_IC}
C_{IN_DDC}	Input capacitance on DDC link	V_{DD_5V} = 0 V, V_{DD_IC} = 0 V, V_{BIAS} = 0 V,f = 1 MHz, V_{OSC}=30 mV		25	30(3)	pF

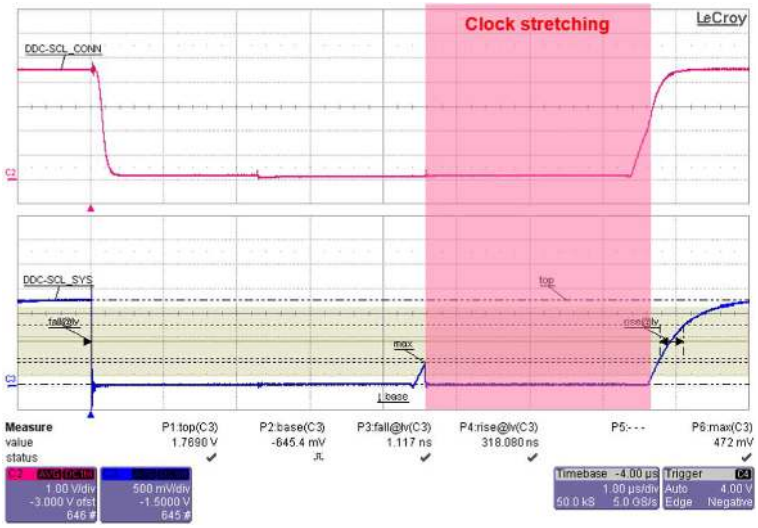
1. *Maximum load capacitance allowed on I2C entire link (cable plus connector) is 750 pF in HDMI™ 1.4 specification.*
2. *Two pull-up resistors in parallel (sink+source). Typical value is 47 kΩ and maximum value is -47 kΩ +10% in HDMI 1.4 specification.*
3. *Maximum capacitance allowed at connector output is 50 pF in HDMI™ 1.4 specification.*

Figure 15. SCL typical waveforms (IC to cable communication in normal mode - without clock stretching operation)



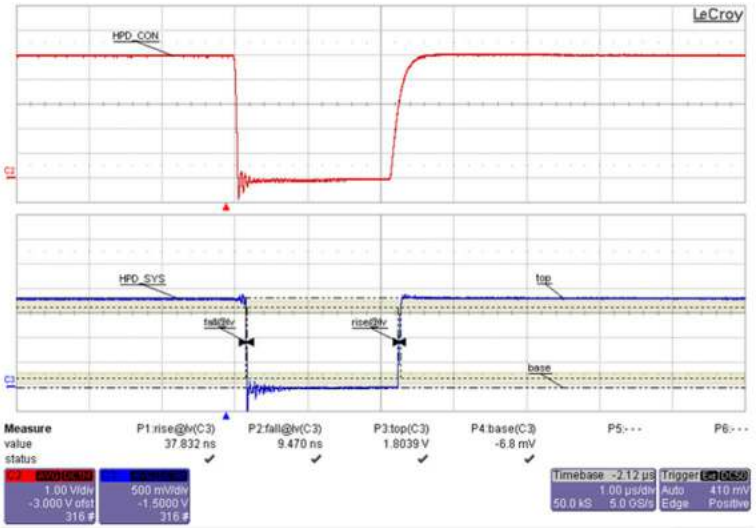
When the source IC releases the clock line and SCL_IC rises up to V_{TH_IC} level, the HDMI2C4-5F2 forces SCL_IC signal at low level and releases SCL on cable side.
When the cable side reaches V_{TH_BUS} level, the HDMI2C4-5F2 activates the dynamic pull-up on cable side and releases SCL_IC. A small parasitic spike occurs on SCL_IC with voltage below $0.3*V_{DD\_IC}$.

Figure 16. SCL typical waveforms (IC to cable communication in clock stretching operation)



Note: Measurements performed with 750 pF load, C_{SYSTEM} = 15 pF and V_{DD_IC} = 1.8 V

Figure 17. **HPD typical waveform (Timing)**

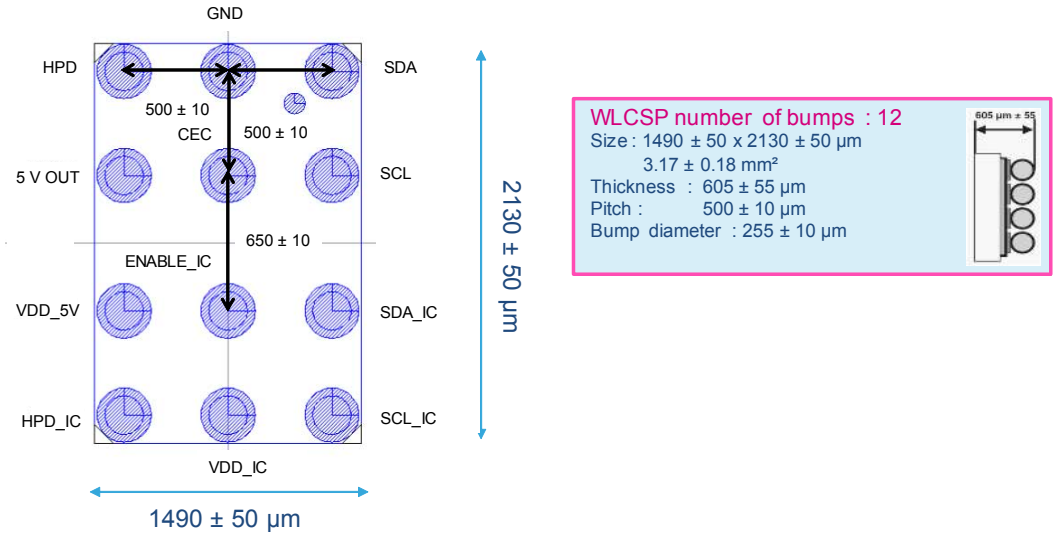


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

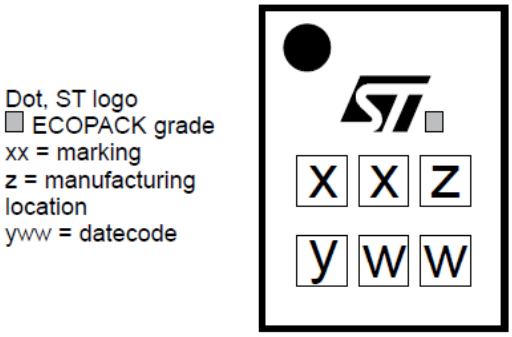
4.1 WLCSP 12 bumps package information

Figure 18. WLCSP 12 bumps package outline



4.2 WLCSP 12 bumps packing information

Figure 19. **Marking**



Note: More packing information is available in the application note:

- *AN2348 Flip-Chip: "Package description and recommendations for use"*

Figure 20. **Footprint**

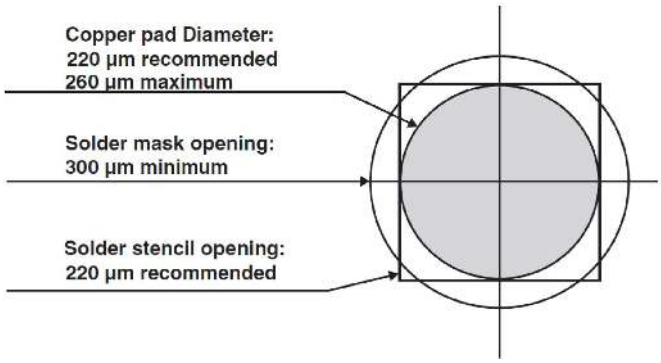
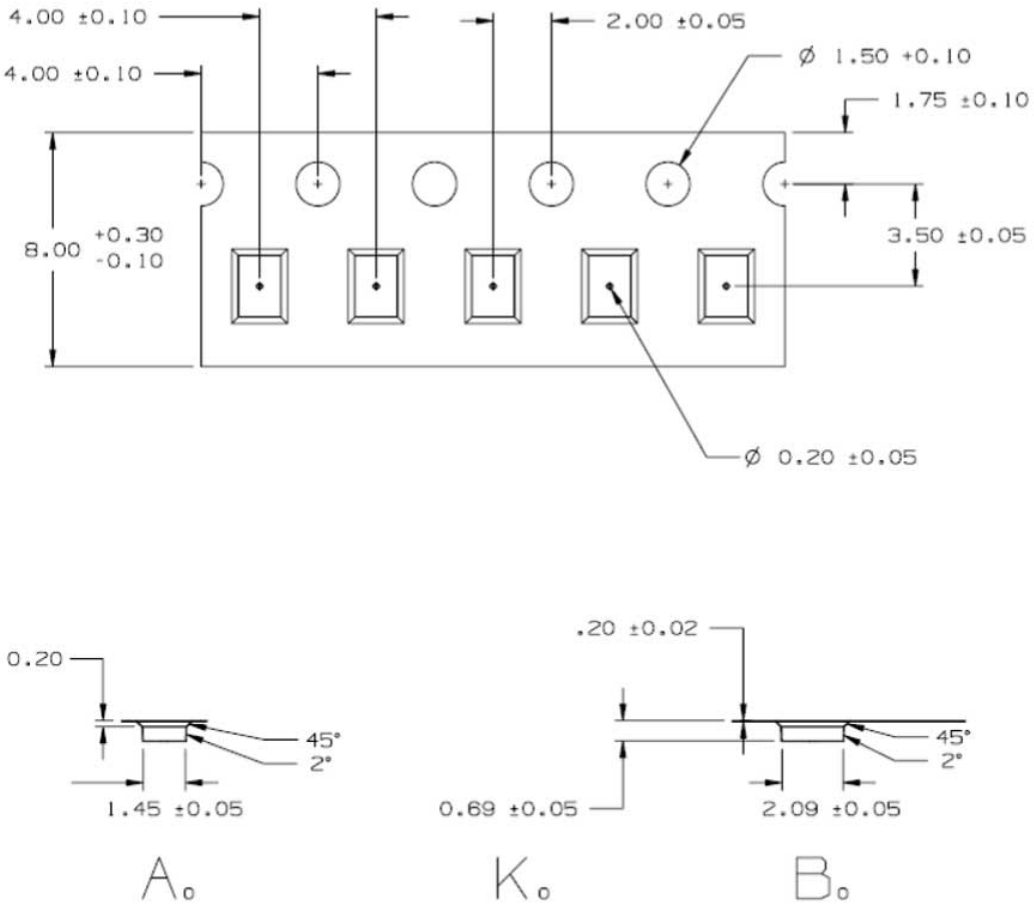


Figure 21. **WLCSP 12 bumps tape and reel specification (all dimensions in mm)**



5 Ordering information

Figure 22. **Ordering information scheme**

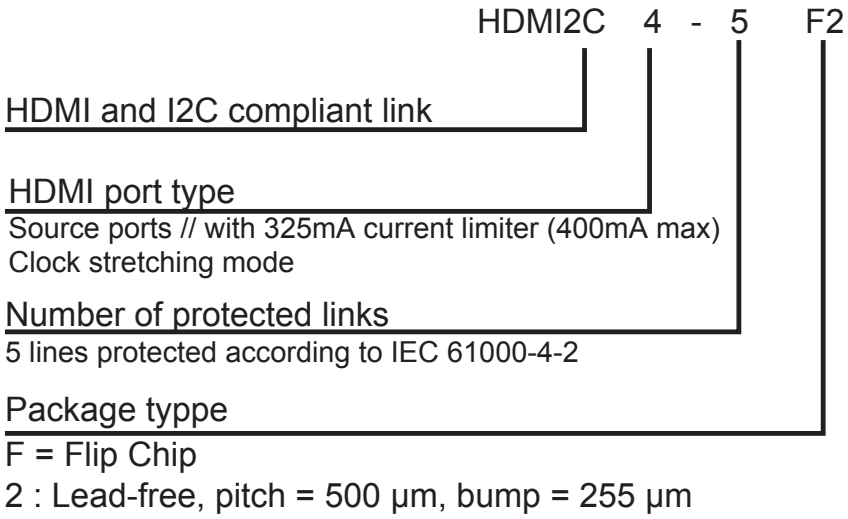


Table 10. **Ordering information**

Order code	Marking	Package	Weight	Base qty.	Delivery mode
HDMI2C4-5F2	PX	WLCSP	4 mg	5000	Tape and reel

Note: More information is available in AN2348 application note :

- *STMicroelectronics 400 micro-meter Flip Chip: package description and recommendation for use*

Revision history

Table 11. **Document revision history**

Date	Revision	Changes
10-Aug-2018	1	Initial release.

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