

## Features

- High Performance, Low Power AVR<sup>®</sup> 8-bit Microcontroller
- Advanced RISC Architecture
  - 131 Powerful Instructions - Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 1 MIPS throughput per MHz
  - On-chip 2-cycle Multiplier
- Data and Non-Volatile Program Memory
  - 8K Bytes Flash of In-System Programmable Program Memory
    - Endurance: 10,000 Write/Erase Cycles
  - Optional Boot Code Section with Independent Lock Bits
- In-System Programming by On-chip Boot Program
- True Read-While-Write Operation
  - 512 Bytes of In-System Programmable EEPROM
- Endurance: 100,000 Write/Erase Cycles
  - 512 Bytes Internal SRAM
  - Programming Lock for Flash Program and EEPROM Data Security
- On Chip Debug Interface (debugWIRE)
- Peripheral Features
  - Two 12-bit High Speed PSC (Power Stage Controllers) with 4-bit Resolution Enhancement
    - Non Overlapping Inverted PWM Output Pins With Flexible Dead-Time
    - Variable PWM duty Cycle and Frequency
    - Synchronous Update of all PWM Registers
    - Auto Stop Function for Event Driven PFC Implementation
    - Less than 25 Hz Step Width at 150 kHz Output Frequency
    - PSC2 with four Output Pins and Output Matrix
  - One 8-bit General purpose Timer/Counter with Separate Prescaler and Capture Mode
  - One 16-bit General purpose Timer/Counter with Separate Prescaler, Compare Mode and Capture Mode
  - Master/Slave SPI Serial Interface
  - 10-bit ADC
    - 8 Single Ended Channels and 1 Fully Differential ADC Channel Pair
    - Programmable Gain (5x, 10x, 20x, 40x on Differential Channel)
    - Internal Reference Voltage
  - Two Analog Comparator with Resistor-Array to Adjust Comparison Voltage
  - 4 External Interrupts
  - Programmable Watchdog Timer with Separate On-Chip Oscillator
- Special Microcontroller Features
  - Low Power Idle, Noise Reduction, and Power Down Modes
  - Power On Reset and Programmable Brown Out Detection
  - Flag Array in Bit-programmable I/O Space (4 bytes)
  - In-System Programmable via SPI Port
  - Internal Calibrated RC Oscillator ( 8 MHz)
  - On-chip PLL for fast PWM ( 32 MHz, 64 MHz) and CPU (16 MHz)



## 8-bit AVR<sup>®</sup> Microcontroller with 8K Bytes In-System Programmable Flash

### AT90PWM1

## Summary



- Operating Voltage: 2.7V - 5.5V
- Extended Operating Temperature:  
– -40°C to +105°

## 1. History

Product	Revision
AT90PWM1	First revision of parts

## 2. Disclaimer

Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characterized.

## 3. Pin Configurations

Figure 3-1. SOIC 24-pin Package

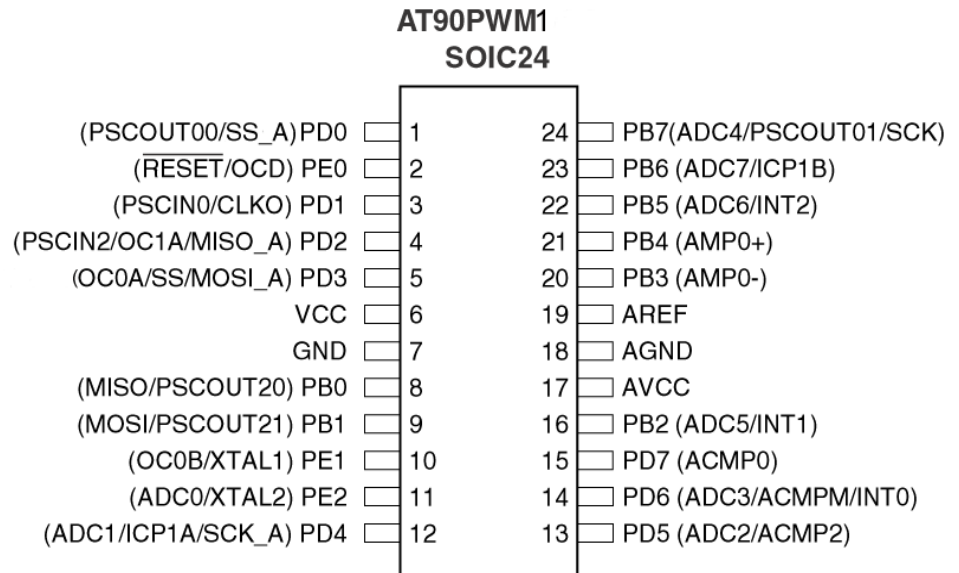
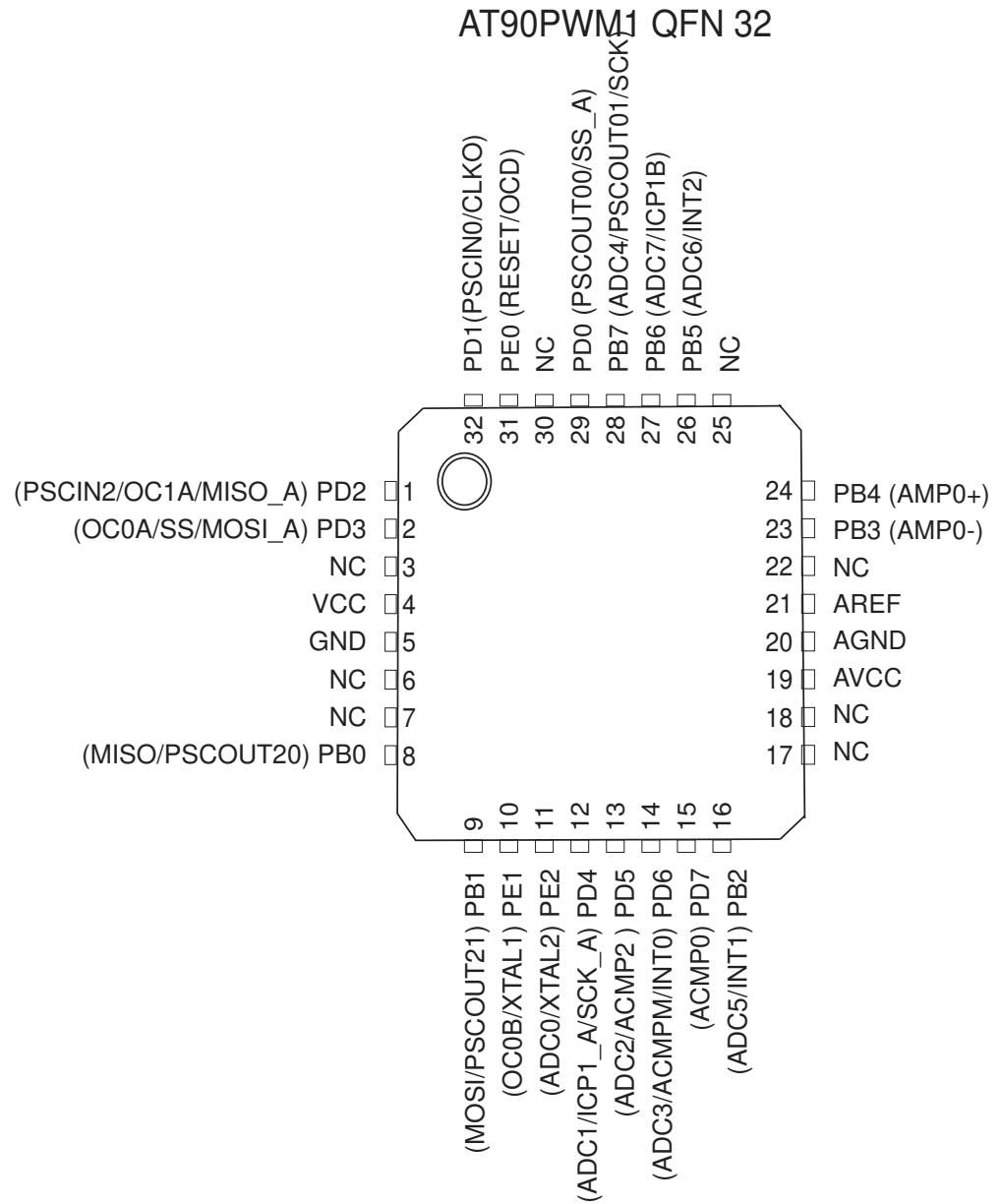


Figure 3-2. QFN 32 -pin Package



### 3.1 Pin Descriptions

**Table 3-1.** Pin out description

QFN32	S024 Pin Number	Mnemonic	Type	Name, Function & Alternate Function
5	7	GND	Power	<b>Ground:</b> 0V reference
20	18	AGND	Power	<b>Analog Ground:</b> 0V reference for analog part
4	6	VCC	power	<b>Power Supply:</b>
19	17	AVCC	Power	<b>Analog Power Supply:</b> This is the power supply voltage for analog part For a normal use this pin must be connected.
21	19	AREF	Power	<b>Analog Reference :</b> reference for analog converter . This is the reference voltage of the A/D converter. As output, can be used by external analog
8	8	PBO	I/O	MISO (SPI Master In Slave Out) PSCOUT20 output
9	9	PB1	I/O	MOSI (SPI Master Out Slave In) PSCOUT21 output
16	16	PB2	I/O	ADC5 (Analog Input Channel5 ) INT1
23	20	PB3	I/O	AMP0- (Analog Differential Amplifier 0 Input Channel )
24	21	PB4	I/O	AMP0+ (Analog Differential Amplifier 0 Input Channel )
26	22	PB5	I/O	ADC6 (Analog Input Channel 6) INT 2
27	23	PB6	I/O	ADC7 (Analog Input Channel 7) ICP1B (Timer 1 input capture alternate input) PSCOUT11 output
28	24	PB7	I/O	PSCOUT01 output ADC4 (Analog Input Channel 4) SCK (SPI Clock)
29	1	PD0	I/O	PSCOUT00 output XCK (UART Transfer Clock) SS_A (Alternate SPI Slave Select)
32	3	PD1	I/O	PSCIN0 (PSC 0 Digital Input ) CLKO (System Clock Output)
1	4	PD2	I/O	PSCIN2 (PSC 2 Digital Input) OC1A (Timer 1 Output Compare A) MISO_A (Programming & alternate SPI Master In Slave Out)
2	5	PD3	I/O	TXD (Dali/UART Tx data) OC0A (Timer 0 Output Compare A) SS (SPI Slave Select) MOSI_A (Programming & alternate Master Out SPI Slave In)

**Table 3-1.** Pin out description (Continued)

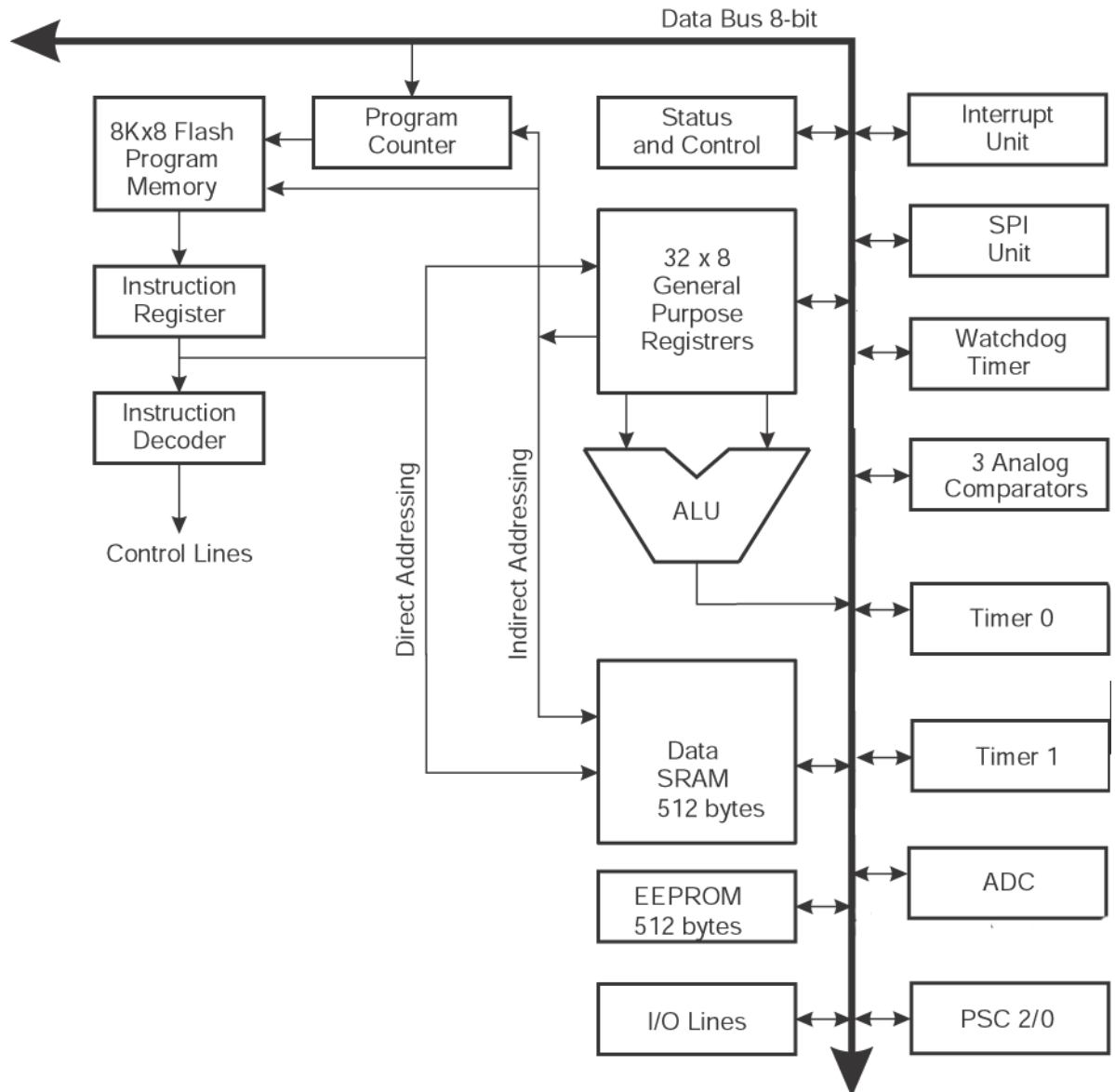
QFN32	S024 Pin Number	Mnemonic	Type	Name, Function & Alternate Function
12	12	PD4	I/O	ADC1 (Analog Input Channel 1) RXD (Dali/UART Rx data) ICP1A (Timer 1 input capture) SCK_A (Programming & alternate SPI Clock)
13	13	PD5	I/O	ADC2 (Analog Input Channel 2) ACMP2 (Analog Comparator 2 Positive Input )
14	14	PD6	I/O	ADC3 (Analog Input Channel 3 ) ACMPM reference for analog comparators INT0
15	15	PD7	I/O	ACMP0 (Analog Comparator 0 Positive Input )
31	2	PE0	I/O or I	RESET (Reset Input) OCD (On Chip Debug I/O)
10	10	PE1	I/O	XTAL1: XTAL Input OC0B (Timer 0 Output Compare B)
11	11	PE2	I/O	XTAL2: XTAL OuTput ADC0 (Analog Input Channel 0)

## 4. Overview

The AT90PWM1 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the AT90PWM1 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

## 4.1 Block Diagram

Figure 4-1. Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The AT90PWM1 provides the following features: 8K bytes of In-System Programmable Flash with Read-While-Write capabilities, 512 bytes EEPROM, 512 bytes SRAM, 53 general purpose I/O lines, 32 general purpose working registers, 2 Power Stage Controllers, two flexible Timer/Counters with compare modes and PWM, an 8-channel 10-bit ADC with two differential

input stage with programmable gain, a programmable Watchdog Timer with Internal Oscillator, an SPI serial port, an On-chip Debug system and four software selectable power saving modes.

The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI ports and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or Hardware Reset. The ADC Noise Reduction mode stops the CPU and all I/O modules except ADC, to minimize switching noise during ADC conversions. In Standby mode, the Crystal/Resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption.

The device is manufactured using Atmel's high-density nonvolatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed in-system through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel AT90PWM1 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The AT90PWM1 AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

## 4.2 Pin Descriptions

### 4.2.1 VCC

Digital supply voltage.

### 4.2.2 GND

Ground.

### 4.2.3 Port B (PB7..PB0)

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the AT90PWM1 as listed on [page 65](#).

### 4.2.4 Port D (PD7..PD0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the AT90PWM1 as listed on [page 68](#).

#### 4.2.5 Port E (PE2..0) RESET/ XTAL1/ XTAL2

Port E is an 3-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port E output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port E pins that are externally pulled low will source current if the pull-up resistors are activated. The Port E pins are tri-stated when a reset condition becomes active, even if the clock is not running.

If the RSTDISBL Fuse is programmed, PE0 is used as an I/O pin. Note that the electrical characteristics of PE0 differ from those of the other pins of Port C.

If the RSTDISBL Fuse is unprogrammed, PE0 is used as a Reset input. A low level on this pin for longer than the minimum pulse length will generate a Reset, even if the clock is not running. The minimum pulse length is given in [Table 9-1 on page 43](#). Shorter pulses are not guaranteed to generate a Reset.

Depending on the clock selection fuse settings, PE1 can be used as input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

Depending on the clock selection fuse settings, PE2 can be used as output from the inverting Oscillator amplifier.

The various special features of Port E are elaborated in [“Alternate Functions of Port E” on page 71](#) and [“Clock Systems and their Distribution” on page 27](#).

#### 4.2.6 AVCC

AVCC is the supply voltage pin for the A/D Converter on Port F. It should be externally connected to  $V_{CC}$ , even if the ADC is not used. If the ADC is used, it should be connected to  $V_{CC}$  through a low-pass filter.

#### 4.2.7 AREF

This is the analog reference pin for the A/D Converter.

### 4.3 About Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.



## 5. Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0xFF)	PICR2H									page 162
(0xFE)	PICR2L									page 162
(0xFD)	PFRC2B	PCAE2B	PISEL2B	PELEV2B	PFLTE2B	PRFM2B3	PRFM2B2	PRFM2B1	PRFM2B0	page 161
(0xFC)	PFRC2A	PCAE2A	PISEL2A	PELEV2A	PFLTE2A	PRFM2A3	PRFM2A2	PRFM2A1	PRFM2A0	page 161
(0xFB)	PCTL2	PPRE21	PPRE20	PBFM2	PAOC2B	PAOC2A	PARUN2	PCCYC2	PRUN2	page 160
(0xFA)	PCNF2	PFIFTY2	PALOCK2	PLOCK2	PMODE21	PMODE20	POP2	PCLKSEL2	POME2	page 157
(0xF9)	OCR2RBH									page 157
(0xF8)	OCR2RBL									page 157
(0xF7)	OCR2SBH									page 157
(0xF6)	OCR2SBL									page 157
(0xF5)	OCR2RAH									page 156
(0xF4)	OCR2RAL									page 156
(0xF3)	OCR2SAH									page 156
(0xF2)	OCR2SAL									page 156
(0xF1)	POM2	POMV2B3	POMV2B2	POMV2B1	POMV2B0	POMV2A3	POMV2A2	POMV2A1	POMV2A0	page 163
(0xF0)	PSOC2	POS23	POS22	PSYNC21	PSYNC20	POEN2D	POEN2B	POEN2C	POEN2A	page 155
(0xEF)	PICR1H									
(0xEE)	PICR1L									
(0xED)	PFRC1B	PCAE1B	PISEL1B	PELEV1B	PFLTE1B	PRFM1B3	PRFM1B2	PRFM1B1	PRFM1B0	page 161
(0xEC)	PFRC1A	PCAE1A	PISEL1A	PELEV1A	PFLTE1A	PRFM1A3	PRFM1A2	PRFM1A1	PRFM1A0	page 161
(0xEB)	PCTL1								PRUN1	page 160
(0xEA)	Reserved	-	-	-	-	-	-	-	-	
(0xE9)	Reserved	-	-	-	-	-	-	-	-	
(0xE8)	Reserved	-	-	-	-	-	-	-	-	
(0xE7)	Reserved	-	-	-	-	-	-	-	-	
(0xE6)	Reserved	-	-	-	-	-	-	-	-	
(0xE5)	Reserved	-	-	-	-	-	-	-	-	
(0xE4)	Reserved	-	-	-	-	-	-	-	-	
(0xE3)	Reserved	-	-	-	-	-	-	-	-	
(0xE2)	Reserved	-	-	-	-	-	-	-	-	
(0xE1)	Reserved	-	-	-	-	-	-	-	-	
(0xE0)	PSOC1	-	-	PSYNC11	PSYNC10	-	POEN1B	-	POEN1A	
(0xDF)	PICR0H									page 162
(0xDE)	PICR0L									page 162
(0xDD)	PFRC0B	PCAE0B	PISEL0B	PELEV0B	PFLTE0B	PRFM0B3	PRFM0B2	PRFM0B1	PRFM0B0	page 161
(0xDC)	PFRC0A	PCAE0A	PISEL0A	PELEV0A	PFLTE0A	PRFM0A3	PRFM0A2	PRFM0A1	PRFM0A0	page 161
(0xDB)	PCTL0	PPRE01	PPRE00	PBFM0	PAOC0B	PAOC0A	PARUN0	PCCYC0	PRUN0	page 158
(0xDA)	PCNF0	PFIFTY0	PALOCK0	PLOCK0	PMODE01	PMODE00	POP0	PCLKSEL0	-	page 157
(0xD9)	OCR0RBH									page 157
(0xD8)	OCR0RBL									page 157
(0xD7)	OCR0SBH									page 157
(0xD6)	OCR0SBL									page 157
(0xD5)	OCR0RAH									page 156
(0xD4)	OCR0RAL									page 156
(0xD3)	OCR0SAH									page 156
(0xD2)	OCR0SAL									page 156
(0xD1)	Reserved	-	-	-	-	-	-	-	-	
(0xD0)	PSOC0	-	-	PSYNC01	PSYNC00	-	POEN0B	-	POEN0A	page 155
(0xCF)	Reserved	-	-	-	-	-	-	-	-	
(0xCE)	Reserved	-	-	-	-	-	-	-	-	
(0xCD)	Reserved	-	-	-	-	-	-	-	-	
(0xCC)	Reserved	-	-	-	-	-	-	-	-	
(0xCB)	Reserved	-	-	-	-	-	-	-	-	
(0xCA)	Reserved	-	-	-	-	-	-	-	-	
(0xC9)	Reserved	-	-	-	-	-	-	-	-	
(0xC8)	Reserved	-	-	-	-	-	-	-	-	
(0xC7)	Reserved	-	-	-	-	-	-	-	-	
(0xC6)	Reserved	-	-	-	-	-	-	-	-	
(0xC5)	Reserved	-	-	-	-	-	-	-	-	
(0xC4)	Reserved	-	-	-	-	-	-	-	-	
(0xC3)	Reserved	-	-	-	-	-	-	-	-	
(0xC2)	Reserved	-	-	-	-	-	-	-	-	
(0xC1)	Reserved	-	-	-	-	-	-	-	-	
(0xC0)	Reserved	-	-	-	-	-	-	-	-	
(0xBF)	Reserved	-	-	-	-	-	-	-	-	



Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0xBE)	Reserved	–	–	–	–	–	–	–	–	
(0xBD)	Reserved	–	–	–	–	–	–	–	–	
(0xBC)	Reserved	–	–	–	–	–	–	–	–	
(0xBB)	Reserved	–	–	–	–	–	–	–	–	
(0xBA)	Reserved	–	–	–	–	–	–	–	–	
(0xB9)	Reserved	–	–	–	–	–	–	–	–	
(0xB8)	Reserved	–	–	–	–	–	–	–	–	
(0xB7)	Reserved	–	–	–	–	–	–	–	–	
(0xB6)	Reserved	–	–	–	–	–	–	–	–	
(0xB5)	Reserved	–	–	–	–	–	–	–	–	
(0xB4)	Reserved	–	–	–	–	–	–	–	–	
(0xB3)	Reserved	–	–	–	–	–	–	–	–	
(0xB2)	Reserved	–	–	–	–	–	–	–	–	
(0xB1)	Reserved	–	–	–	–	–	–	–	–	
(0xB0)	Reserved	–	–	–	–	–	–	–	–	
(0xAF)	AC2CON	AC2EN	AC2IE	AC2IS1	AC2IS0	AC2SADE-	AC2M2	AC2M1	AC2M0	<a href="#">page 178</a>
(0xAD)	AC0CON	AC0EN	AC0IE	AC0IS1	AC0IS0	-	AC0M2	AC0M1	AC0M0	<a href="#">page 177</a>
(0xAC)	Reserved	–	–	–	–	–	–	–	–	<a href="#">page 258</a>
(0xAB)	Reserved	–	–	–	–	–	–	–	–	<a href="#">page 258</a>
(0xAA)	Reserved	–	–	–	–	–	–	–	–	<a href="#">page 257</a>
(0xA9)	Reserved	–	–	–	–	–	–	–	–	
(0xA8)	Reserved	–	–	–	–	–	–	–	–	
(0xA7)	Reserved	–	–	–	–	–	–	–	–	
(0xA6)	Reserved	–	–	–	–	–	–	–	–	
(0xA5)	PIM2	-	-	PSEIE2	PEVE2B	PEVE2A	-	-	PEOPE2	<a href="#">page 164</a>
(0xA4)	PIFR2	-	-	PSEI2	PEV2B	PEV2A	PRN21	PRN20	PEOP2	<a href="#">page 164</a>
(0xA3)	Reserved	–	–	–	–	–	–	–	–	
(0xA2)	Reserved	–	–	–	–	–	–	–	–	
(0xA1)	PIM0	-	-	PSEIE0	PEVE0B	PEVE0A	-	-	PEOPE0	<a href="#">page 164</a>
(0xA0)	PIFR0	-	-	PSEI0	PEV0B	PEV0A	PRN01	PRN00	PEOP0	<a href="#">page 164</a>
(0x9F)	Reserved	–	–	–	–	–	–	–	–	
(0x9E)	Reserved	–	–	–	–	–	–	–	–	
(0x9D)	Reserved	–	–	–	–	–	–	–	–	
(0x9C)	Reserved	–	–	–	–	–	–	–	–	
(0x9B)	Reserved	–	–	–	–	–	–	–	–	
(0x9A)	Reserved	–	–	–	–	–	–	–	–	
(0x99)	Reserved	–	–	–	–	–	–	–	–	
(0x98)	Reserved	–	–	–	–	–	–	–	–	
(0x97)	Reserved	–	–	–	–	–	–	–	–	
(0x96)	Reserved	–	–	–	–	–	–	–	–	
(0x95)	Reserved	–	–	–	–	–	–	–	–	
(0x94)	Reserved	–	–	–	–	–	–	–	–	
(0x93)	Reserved	–	–	–	–	–	–	–	–	
(0x92)	Reserved	–	–	–	–	–	–	–	–	
(0x91)	Reserved	–	–	–	–	–	–	–	–	
(0x90)	Reserved	–	–	–	–	–	–	–	–	
(0x8F)	Reserved	–	–	–	–	–	–	–	–	
(0x8E)	Reserved	–	–	–	–	–	–	–	–	
(0x8D)	Reserved	–	–	–	–	–	–	–	–	
(0x8C)	Reserved	–	–	–	–	–	–	–	–	
(0x8B)	OCR1BH	OCR1B15	OCR1B14	OCR1B13	OCR1B12	OCR1B11	OCR1B10	OCR1B9	OCR1B8	<a href="#">page 120</a>
(0x8A)	OCR1BL	OCR1B7	OCR1B6	OCR1B5	OCR1B4	OCR1B3	OCR1B2	OCR1B1	OCR1B0	<a href="#">page 120</a>
(0x89)	OCR1AH	OCR1A15	OCR1A14	OCR1A13	OCR1A12	OCR1A11	OCR1A10	OCR1A9	OCR1A8	<a href="#">page 120</a>
(0x88)	OCR1AL	OCR1A7	OCR1A6	OCR1A5	OCR1A4	OCR1A3	OCR1A2	OCR1A1	OCR1A0	<a href="#">page 120</a>
(0x87)	ICR1H	ICR115	ICR114	ICR113	ICR112	ICR111	ICR110	ICR19	ICR18	<a href="#">page 121</a>
(0x86)	ICR1L	ICR17	ICR16	ICR15	ICR14	ICR13	ICR12	ICR11	ICR10	<a href="#">page 121</a>
(0x85)	TCNT1H	TCNT115	TCNT114	TCNT113	TCNT112	TCNT111	TCNT110	TCNT19	TCNT18	<a href="#">page 120</a>
(0x84)	TCNT1L	TCNT17	TCNT16	TCNT15	TCNT14	TCNT13	TCNT12	TCNT11	TCNT10	<a href="#">page 120</a>
(0x83)	Reserved	–	–	–	–	–	–	–	–	
(0x82)	TCCR1C	FOC1A	FOC1B	–	–	–	–	–	–	<a href="#">page 119</a>
(0x81)	TCCR1B	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10	<a href="#">page 118</a>
(0x80)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	–	–	WGM11	WGM10	<a href="#">page 116</a>
(0x7F)	DIDR1	–	–	ACMP0D	AMP0PD	AMP0ND	ADC10D/ACMP1D	ADC9D/AMP1PD	ADC8D/AMP1ND	<a href="#">page 199</a>
(0x7E)	DIDR0	ADC7D	ADC6D	ADC5D	ADC4D	ADC3D/ACMPMD	ADC2D/ACMP2D	ADC1D	ADC0D	<a href="#">page 199</a>
(0x7D)	Reserved	–	–	–	–	–	–	–	–	



Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x1A (0x3A)	<b>GPIOR2</b>	GPIOR27	GPIOR26	GPIOR25	GPIOR24	GPIOR23	GPIOR22	GPIOR21	GPIOR20	<a href="#">page 25</a>
0x19 (0x39)	<b>GPIOR1</b>	GPIOR17	GPIOR16	GPIOR15	GPIOR14	GPIOR13	GPIOR12	GPIOR11	GPIOR10	<a href="#">page 25</a>
0x18 (0x38)	<b>Reserved</b>	–	–	–	–	–	–	–	–	
0x17 (0x37)	<b>Reserved</b>	–	–	–	–	–	–	–	–	
0x16 (0x36)	<b>TIFR1</b>	–	–	ICF1	–	–	OCF1B	OCF1A	TOV1	<a href="#">page 122</a>
0x15 (0x35)	<b>TIFR0</b>	–	–	–	–	–	OCF0B	OCF0A	TOV0	<a href="#">page 94</a>
0x14 (0x34)	<b>Reserved</b>	–	–	–	–	–	–	–	–	
0x13 (0x33)	<b>Reserved</b>	–	–	–	–	–	–	–	–	
0x12 (0x32)	<b>Reserved</b>	–	–	–	–	–	–	–	–	
0x11 (0x31)	<b>Reserved</b>	–	–	–	–	–	–	–	–	
0x10 (0x30)	<b>Reserved</b>	–	–	–	–	–	–	–	–	
0x0F (0x2F)	<b>Reserved</b>	–	–	–	–	–	–	–	–	
0x0E (0x2E)	<b>PORTE</b>	–	–	–	–	–	PORTE2	PORTE1	PORTE0	<a href="#">page 73</a>
0x0D (0x2D)	<b>DDRE</b>	–	–	–	–	–	DDE2	DDE1	DDE0	<a href="#">page 73</a>
0x0C (0x2C)	<b>PINE</b>	–	–	–	–	–	PINE2	PINE1	PINE0	<a href="#">page 73</a>
0x0B (0x2B)	<b>PORTD</b>	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	<a href="#">page 73</a>
0x0A (0x2A)	<b>DDR0</b>	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	<a href="#">page 73</a>
0x09 (0x29)	<b>PIND</b>	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	<a href="#">page 73</a>
0x08 (0x28)	<b>Reserved</b>	–	–	–	–	–	–	–	–	
0x07 (0x27)	<b>Reserved</b>	–	–	–	–	–	–	–	–	
0x06 (0x26)	<b>Reserved</b>	–	–	–	–	–	–	–	–	
0x05 (0x25)	<b>PORTB</b>	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	<a href="#">page 72</a>
0x04 (0x24)	<b>DDRB</b>	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	<a href="#">page 72</a>
0x03 (0x23)	<b>PINB</b>	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	<a href="#">page 73</a>
0x02 (0x22)	<b>Reserved</b>	–	–	–	–	–	–	–	–	
0x01 (0x21)	<b>Reserved</b>	–	–	–	–	–	–	–	–	
0x00 (0x20)	<b>Reserved</b>	–	–	–	–	–	–	–	–	

- Note:
1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
  2. I/O Registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
  3. Some of the status flags are cleared by writing a logical one to them. Note that, unlike most other AVRs, the CBI and SBI instructions will only operate on the specified bit, and can therefore be used on registers containing such status flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.
  4. When using the I/O specific commands IN and OUT, the I/O addresses 0x00 - 0x3F must be used. When addressing I/O Registers as data space using LD and ST instructions, 0x20 must be added to these addresses. The AT90PWM1 is a complex microcontroller with more peripheral units than can be supported within the 64 location reserved in Opcode for the IN and OUT instructions. For the Extended I/O space from 0x60 - 0xFF in SRAM, only the ST/STS/STD and LD/LDS/LDD instructions can be used.

## 6. Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
<b>ARITHMETIC AND LOGIC INSTRUCTIONS</b>					
ADD	Rd, Rr	Add two Registers	$Rd \leftarrow Rd + Rr$	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,H	1
ADIW	Rdl,K	Add Immediate to Word	$Rdh:Rdl \leftarrow Rdh:Rdl + K$	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	$Rd \leftarrow Rd - Rr$	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	$Rd \leftarrow Rd - K$	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry two Registers	$Rd \leftarrow Rd - Rr - C$	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	$Rd \leftarrow Rd - K - C$	Z,C,N,V,H	1
SBIW	Rdl,K	Subtract Immediate from Word	$Rdh:Rdl \leftarrow Rdh:Rdl - K$	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND Registers	$Rd \leftarrow Rd \cdot Rr$	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	$Rd \leftarrow Rd \cdot K$	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	$Rd \leftarrow Rd \vee Rr$	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	$Rd \leftarrow Rd \vee K$	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	$Rd \leftarrow Rd \oplus Rr$	Z,N,V	1
COM	Rd	One's Complement	$Rd \leftarrow 0xFF - Rd$	Z,C,N,V	1
NEG	Rd	Two's Complement	$Rd \leftarrow 0x00 - Rd$	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	$Rd \leftarrow Rd \vee K$	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	$Rd \leftarrow Rd \cdot (0xFF - K)$	Z,N,V	1
INC	Rd	Increment	$Rd \leftarrow Rd + 1$	Z,N,V	1
DEC	Rd	Decrement	$Rd \leftarrow Rd - 1$	Z,N,V	1
TST	Rd	Test for Zero or Minus	$Rd \leftarrow Rd \oplus Rd$	Z,N,V	1
CLR	Rd	Clear Register	$Rd \leftarrow Rd \oplus Rd$	Z,N,V	1
SER	Rd	Set Register	$Rd \leftarrow 0xFF$	None	1
MUL	Rd, Rr	Multiply Unsigned	$R1:R0 \leftarrow Rd \times Rr$	Z,C	2
MULS	Rd, Rr	Multiply Signed	$R1:R0 \leftarrow Rd \times Rr$	Z,C	2
MULSU	Rd, Rr	Multiply Signed with Unsigned	$R1:R0 \leftarrow Rd \times Rr$	Z,C	2
FMUL	Rd, Rr	Fractional Multiply Unsigned	$R1:R0 \leftarrow (Rd \times Rr) \ll 1$	Z,C	2
FMULS	Rd, Rr	Fractional Multiply Signed	$R1:R0 \leftarrow (Rd \times Rr) \ll 1$	Z,C	2
FMULSU	Rd, Rr	Fractional Multiply Signed with Unsigned	$R1:R0 \leftarrow (Rd \times Rr) \ll 1$	Z,C	2
<b>BRANCH INSTRUCTIONS</b>					
RJMP	k	Relative Jump	$PC \leftarrow PC + k + 1$	None	2
IJMP		Indirect Jump to (Z)	$PC \leftarrow Z$	None	2
RCALL	k	Relative Subroutine Call	$PC \leftarrow PC + k + 1$	None	3
ICALL		Indirect Call to (Z)	$PC \leftarrow Z$	None	3
RET		Subroutine Return	$PC \leftarrow STACK$	None	4
RETI		Interrupt Return	$PC \leftarrow STACK$	I	4
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) $PC \leftarrow PC + 2$ or 3	None	1/2/3
CP	Rd,Rr	Compare	$Rd - Rr$	Z, N,V,C,H	1
CPC	Rd,Rr	Compare with Carry	$Rd - Rr - C$	Z, N,V,C,H	1
CPI	Rd,K	Compare Register with Immediate	$Rd - K$	Z, N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBRS	Rr, b	Skip if Bit in Register is Set	if (Rr(b)=1) $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBIC	P, b	Skip if Bit in I/O Register Cleared	if (P(b)=0) $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBIS	P, b	Skip if Bit in I/O Register is Set	if (P(b)=1) $PC \leftarrow PC + 2$ or 3	None	1/2/3
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BREQ	k	Branch if Equal	if (Z = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRNE	k	Branch if Not Equal	if (Z = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRCS	k	Branch if Carry Set	if (C = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRCC	k	Branch if Carry Cleared	if (C = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRSH	k	Branch if Same or Higher	if (C = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRLO	k	Branch if Lower	if (C = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRMI	k	Branch if Minus	if (N = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRPL	k	Branch if Plus	if (N = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if (N $\oplus$ V = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRLT	k	Branch if Less Than Zero, Signed	if (N $\oplus$ V = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRTS	k	Branch if T Flag Set	if (T = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRTS	k	Branch if T Flag Cleared	if (T = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then $PC \leftarrow PC + k + 1$	None	1/2

Mnemonics	Operands	Description	Operation	Flags	#Clocks
<b>BIT AND BIT-TEST INSTRUCTIONS</b>					
SBI	P,b	Set Bit in I/O Register	$I/O(P,b) \leftarrow 1$	None	2
CBI	P,b	Clear Bit in I/O Register	$I/O(P,b) \leftarrow 0$	None	2
LSL	Rd	Logical Shift Left	$Rd(n+1) \leftarrow Rd(n), Rd(0) \leftarrow 0$	Z,C,N,V	1
LSR	Rd	Logical Shift Right	$Rd(n) \leftarrow Rd(n+1), Rd(7) \leftarrow 0$	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	$Rd(0) \leftarrow C, Rd(n+1) \leftarrow Rd(n), C \leftarrow Rd(7)$	Z,C,N,V	1
ROR	Rd	Rotate Right Through Carry	$Rd(7) \leftarrow C, Rd(n) \leftarrow Rd(n+1), C \leftarrow Rd(0)$	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	$Rd(n) \leftarrow Rd(n+1), n=0..6$	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	$Rd(3..0) \leftarrow Rd(7..4), Rd(7..4) \leftarrow Rd(3..0)$	None	1
BSET	s	Flag Set	$SREG(s) \leftarrow 1$	SREG(s)	1
BCLR	s	Flag Clear	$SREG(s) \leftarrow 0$	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	$T \leftarrow Rr(b)$	T	1
BLD	Rd, b	Bit load from T to Register	$Rd(b) \leftarrow T$	None	1
SEC		Set Carry	$C \leftarrow 1$	C	1
CLC		Clear Carry	$C \leftarrow 0$	C	1
SEN		Set Negative Flag	$N \leftarrow 1$	N	1
CLN		Clear Negative Flag	$N \leftarrow 0$	N	1
SEZ		Set Zero Flag	$Z \leftarrow 1$	Z	1
CLZ		Clear Zero Flag	$Z \leftarrow 0$	Z	1
SEI		Global Interrupt Enable	$I \leftarrow 1$	I	1
CLI		Global Interrupt Disable	$I \leftarrow 0$	I	1
SES		Set Signed Test Flag	$S \leftarrow 1$	S	1
CLS		Clear Signed Test Flag	$S \leftarrow 0$	S	1
SEV		Set Twos Complement Overflow	$V \leftarrow 1$	V	1
CLV		Clear Twos Complement Overflow	$V \leftarrow 0$	V	1
SET		Set T in SREG	$T \leftarrow 1$	T	1
CLT		Clear T in SREG	$T \leftarrow 0$	T	1
SEH		Set Half Carry Flag in SREG	$H \leftarrow 1$	H	1
CLH		Clear Half Carry Flag in SREG	$H \leftarrow 0$	H	1
<b>DATA TRANSFER INSTRUCTIONS</b>					
MOV	Rd, Rr	Move Between Registers	$Rd \leftarrow Rr$	None	1
MOVW	Rd, Rr	Copy Register Word	$Rd+1:Rd \leftarrow Rr+1:Rr$	None	1
LDI	Rd, K	Load Immediate	$Rd \leftarrow K$	None	1
LD	Rd, X	Load Indirect	$Rd \leftarrow (X)$	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	$Rd \leftarrow (X), X \leftarrow X + 1$	None	2
LD	Rd, -X	Load Indirect and Pre-Dec.	$X \leftarrow X - 1, Rd \leftarrow (X)$	None	2
LD	Rd, Y	Load Indirect	$Rd \leftarrow (Y)$	None	2
LD	Rd, Y+	Load Indirect and Post-Inc.	$Rd \leftarrow (Y), Y \leftarrow Y + 1$	None	2
LD	Rd, -Y	Load Indirect and Pre-Dec.	$Y \leftarrow Y - 1, Rd \leftarrow (Y)$	None	2
LDD	Rd, Y+q	Load Indirect with Displacement	$Rd \leftarrow (Y + q)$	None	2
LD	Rd, Z	Load Indirect	$Rd \leftarrow (Z)$	None	2
LD	Rd, Z+	Load Indirect and Post-Inc.	$Rd \leftarrow (Z), Z \leftarrow Z + 1$	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	$Z \leftarrow Z - 1, Rd \leftarrow (Z)$	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	$Rd \leftarrow (Z + q)$	None	2
LDS	Rd, k	Load Direct from SRAM	$Rd \leftarrow (k)$	None	2
ST	X, Rr	Store Indirect	$(X) \leftarrow Rr$	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	$(X) \leftarrow Rr, X \leftarrow X + 1$	None	2
ST	-X, Rr	Store Indirect and Pre-Dec.	$X \leftarrow X - 1, (X) \leftarrow Rr$	None	2
ST	Y, Rr	Store Indirect	$(Y) \leftarrow Rr$	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	$(Y) \leftarrow Rr, Y \leftarrow Y + 1$	None	2
ST	-Y, Rr	Store Indirect and Pre-Dec.	$Y \leftarrow Y - 1, (Y) \leftarrow Rr$	None	2
STD	Y+q, Rr	Store Indirect with Displacement	$(Y + q) \leftarrow Rr$	None	2
ST	Z, Rr	Store Indirect	$(Z) \leftarrow Rr$	None	2
ST	Z+, Rr	Store Indirect and Post-Inc.	$(Z) \leftarrow Rr, Z \leftarrow Z + 1$	None	2
ST	-Z, Rr	Store Indirect and Pre-Dec.	$Z \leftarrow Z - 1, (Z) \leftarrow Rr$	None	2
STD	Z+q, Rr	Store Indirect with Displacement	$(Z + q) \leftarrow Rr$	None	2
STS	k, Rr	Store Direct to SRAM	$(k) \leftarrow Rr$	None	2
LPM		Load Program Memory	$R0 \leftarrow (Z)$	None	3
LPM	Rd, Z	Load Program Memory	$Rd \leftarrow (Z)$	None	3
LPM	Rd, Z+	Load Program Memory and Post-Inc	$Rd \leftarrow (Z), Z \leftarrow Z + 1$	None	3
SPM		Store Program Memory	$(Z) \leftarrow R1:R0$	None	-
IN	Rd, P	In Port	$Rd \leftarrow P$	None	1
OUT	P, Rr	Out Port	$P \leftarrow Rr$	None	1
PUSH	Rr	Push Register on Stack	$STACK \leftarrow Rr$	None	2
POP	Rd	Pop Register from Stack	$Rd \leftarrow STACK$	None	2
<b>MCU CONTROL INSTRUCTIONS</b>					

Mnemonics	Operands	Description	Operation	Flags	#Clocks
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR/timer)	None	1
BREAK		Break	For On-chip Debug Only	None	N/A

## 7. Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
16	2.7 - 5.5V	AT90PWM1-16SU	SO24	Extended (-40°C to 105°C)
16	2.7 - 5.5V	AT90PWM1-16MU	QFN32	Extended (-40°C to 105°C)

Note: All packages are Pb free, fully LHF

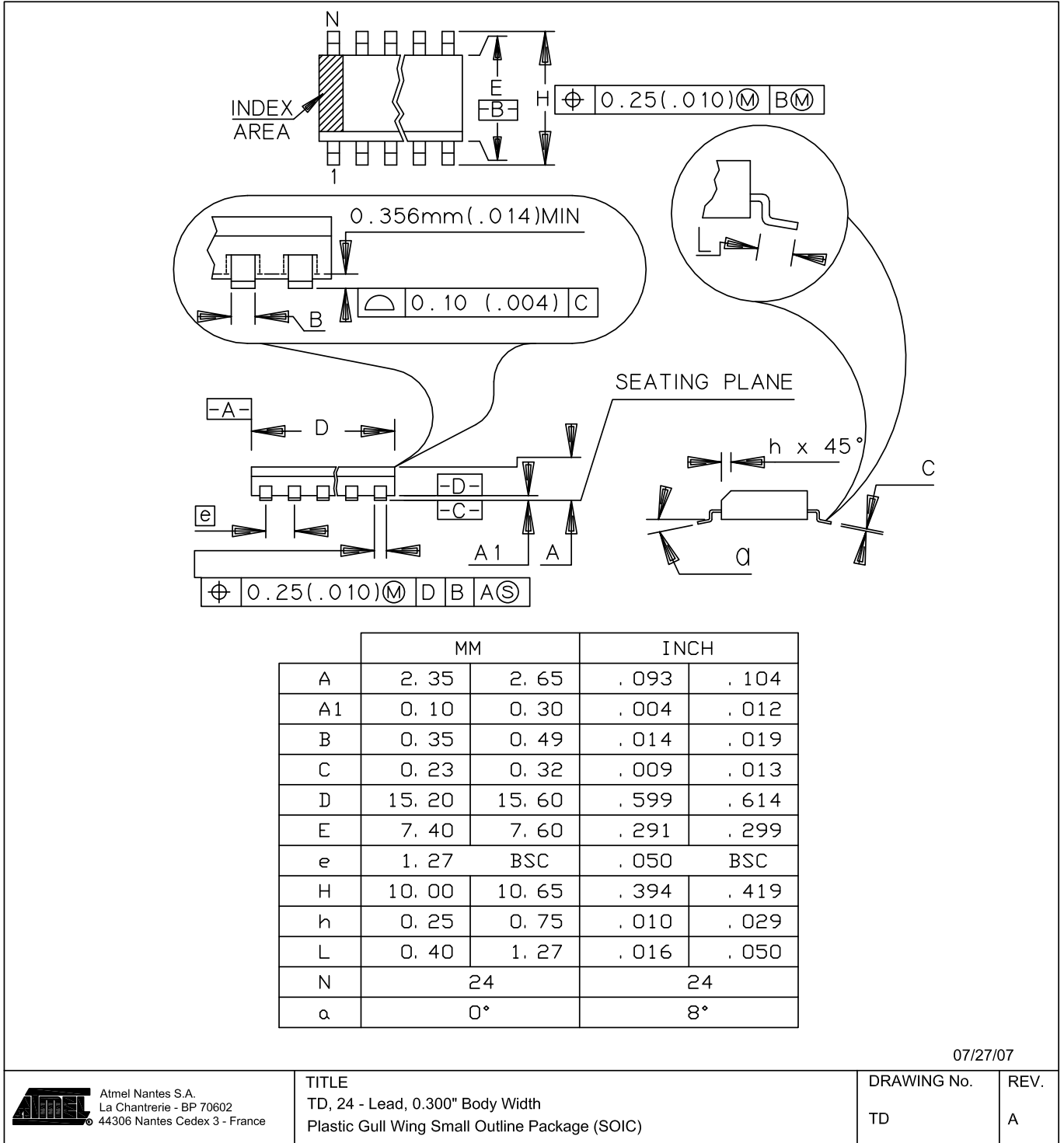
Note: This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.



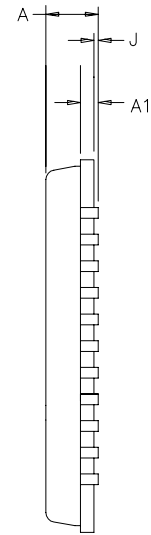
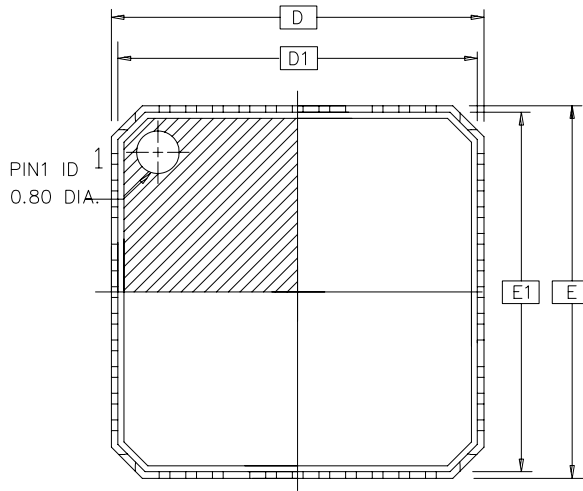
## 8. Package Information

Package Type	
<b>SO24</b>	24-Lead, 0.300" Body width, Plastic GullWing Small Outline Package (SOIC)
<b>QFN32</b>	32-Lead, Quad Flat No lead

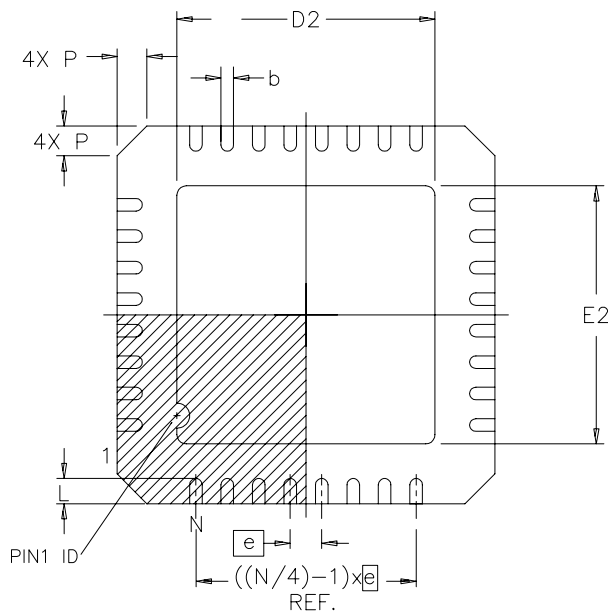
# 8.1 SO24



## 8.2 QFN32



DRAWINGS NOT SCALED



	MM			INCH		
	MIN	NDM	MAX	MIN	NDM	MAX
A	0.80	-	1.00	.032	-	.040
J	0.00	0.01	0.05	.000	.000	.002
A1	0.20 ref			.008 ref		
D/E	7.00 BSC			.276 BSC		
D1/E1	6.75 BSC			.266 BSC		
D2/E2	2.25	-	5.25	.090	-	.207
N	32					
P	0.24	0.42	0.60	.009	.016	.024
e	0.65 BSC			.026 BSC		
L	0.35	-	0.75	.014	-	.030
b	0.23	-	0.35	.009	-	.014

Compliant JEDEC Standard MO-220 variation VKKC



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