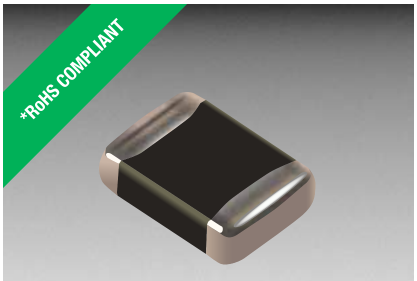


Features

- Formerly a KEKOVARICON product
- Four model sizes available - 0603, 0805, 1206 and 1210
- Characterized for inductance and capacitance
- Short response time
- Non-sensitive to mildly activated fluxes
- Operating voltage range up to 18 V
- Non-plastic coating for better flammability rating
- RoHS compliant*

BOURNS®

ZVE Series - Suppression Varistors

General Information

ZVE varistors are designed to suppress ESD events, including those specified in IEC 1000-4-2 or other standards used for Electromagnetic Compliance testing. The ZVE series is typically applied to protect integrated circuits and other components at the circuit board level operating at 18 VDC or less.

The fabrication method, design and materials of these devices result in capacitance characteristics typically suitable for high frequency attenuation/low-pass filter circuit functions, providing suppression and filtering in a single device.

Absolute Maximum Ratings

Parameter	Value	Units
Continuous:		
Steady State Applied Voltage		
DC Voltage Range (V_{dc})	≤ 18	V
AC Voltage Range (V_{rms})	2 to 30	V
Transient:		
Peak Single Pulse Surge Current, 8/20 μs Waveform (I_{max})	20, 30	A
Single Pulse Surge Energy, 10/1000 μs Waveform (W_{max})	0.05 to 0.1	J
Operating Ambient Temperature	-55 to +125	°C
Storage Temperature Range	-55 to +150	°C
Threshold Voltage Temperature Coefficient	< +0.05	%/°C
Response Time	< 1	ns
Climatic Category	55 / 125 / 56	

Additional Information

Click these links for more information:

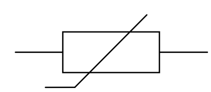
PRODUCT SELECTOR | TECHNICAL LIBRARY | INVENTORY | SAMPLES | CONTACT

Agency Recognition

Standard	UL 1449
File Number	E326499**

**Not all rated voltages are UL recognized; check the file for details.

Multilayered Varistor Symbol



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EMEA: Tel: +36 88 885 877 • Email: eurocus@bourns.com
The Americas: Tel: +1-951 781-5500 • Email: americus@bourns.com
www.bourns.com

WARNING Cancer and Reproductive Harm - www.P65Warnings.ca.gov

Applications

- Protection of components and circuits sensitive to ESD transients occurring on power supply, control and signal lines
- Suppression of ESD events as specified in IEEEC 1000-4-2, MIL-STD 883C, method 3015.7 or AEC-Q200-002 for Electromagnetic Compliance (EMC)
- Used in mobile communication, computer/EDP products, medical products* handheld/portable devices, industrial equipment, including diagnostic port protection and I/O interfaces

ZVE Series – Suppression Varistors

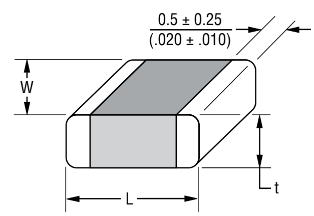
BOURNS®

Device Ratings

Model	V_{rms}	V_{dc}	V_n @ 1 mA	V_c 8/20 μs	I_c 8/20 μs	W_{max} 10/1000 μs	P max.	C_{max} @ 1 MHz	I_{typ} 100 mA/ns
	V	V	V	V	A	J	W	pF	nH
ZVE 14 S 0603	14	18	22 - 28	50	2	0.05	0.003	75	< 1.0
ZVE 14 S 0805	14	18	22 - 28	50	2	0.10	0.004	100	< 1.5
ZVE 14 S 1206	14	18	22 - 28	50	2	0.10	0.004	200	< 1.8
ZVE 14 S 1210	14	18	22 - 28	50	2	0.10	0.004	400	< 3.5

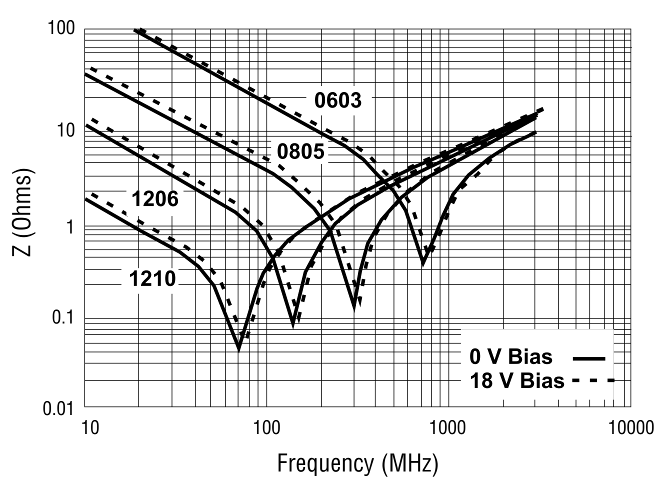
Product Dimensions

Model	Dimension		
	L	W	t (Max.)
ZVE 14 S 0603	1.6 ± 0.20 (.063 ± .008)	0.80 ± 0.10 (.031 ± .004)	0.95 (.037)
ZVE 14 S 0805	2.0 ± 0.25 (.079 ± .010)	1.25 ± 0.20 (.049 ± .008)	0.95 (.037)
ZVE 14 S 1206	3.2 ± 0.30 (.126 ± .012)	1.60 ± 0.20 (.063 ± .008)	1.20 (.047)
ZVE 14 S 1210	3.2 ± 0.30 (.126 ± .012)	2.50 ± 0.25 (.098 ± .010)	1.30 (.051)



DIMENSIONS: $\frac{\text{MM}}{\text{(INCHES)}}$

Capacitance - Frequency Characteristics



Specifications are subject to change without notice.
Users should verify actual device performance in their specific applications.
The products described herein and this document are subject to specific legal disclaimers as set forth on the last page of this document, and at www.bourns.com/docs/legal/disclaimer.pdf.

How to Order

ZVE14S1206NIR1yy

- Series Designator
  - ZVE = ZVE Series
- Maximum Continuous Working Voltage (V_{rms})
- V_n Tolerance
  - S = Special (See Device Ratings Table for Details)
- Model Size
  - 0603
  - 0805
  - 1206
  - 1210
- End Terminations
  - (Blank) = AgPd end terminations suitable for Pb reflow soldering (Available upon Request)
  - N = Barrier type end terminations suitable for Pb-free reflow soldering
  - NI = NiSn barrier type end terminations suitable for Pb and Pb-free reflow soldering (Standard)
- Packaging
  - R1 = 4000 pcs. per 180 mm (7-inch) reel
- Special Requirements
  - yy

Instructions for Creating Orderable Part Number:

1) Start with base part number in characteristics table (example: ZVE14S1206).

2) Add End Terminations: NI (example part number becomes ZVE14S1206NI).

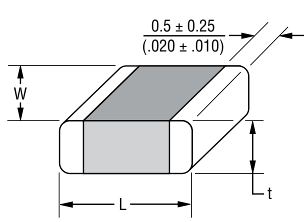
3) Add Packaging: R1 (example part number becomes ZVE14S1206NIR1).

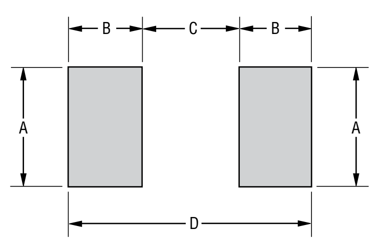
4) Part number can have no spaces or lower case letters.

Typical Part Marking

No marking.

Soldering Pad Configuration





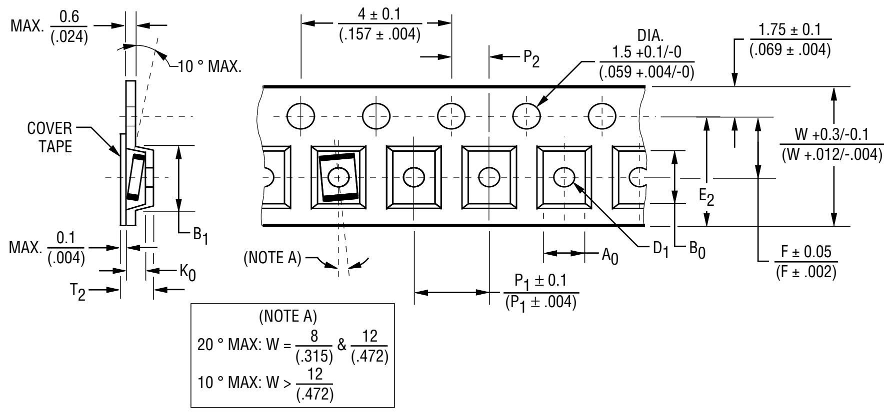
DIMENSIONS: MM / (INCHES)

Size	Dimension						
	L	W	t (Max.)	A	B	C	D
0603	1.6 ± 0.20 (.063 ± .008)	0.80 ± 0.10 (.315 ± .004)	1.0 (.039)	1.0 (.039)	1.0 (.039)	0.6 (.024)	2.6 (.102)
0805	2.0 ± 0.25 (.079 ± .010)	1.25 ± 0.20 (.049 ± .008)	1.1 (.043)	1.4 (.055)	1.2 (.047)	1.0 (.039)	3.4 (.134)
1206	3.2 ± 0.30 (.126 ± .012)	1.60 ± 0.20 (.063 ± .008)	1.6 (.063)	1.8 (.071)	1.2 (.047)	2.1 (.083)	4.5 (.177)
1210	3.2 ± 0.30 (.126 ± .012)	2.50 ± 0.20 (.098 ± .008)	1.8 (.071)	2.8 (.110)	1.2 (.047)	2.1 (.083)	4.5 (.177)

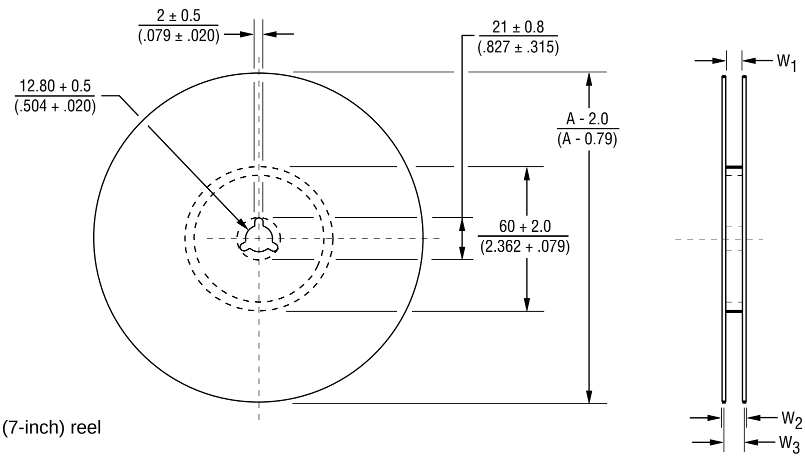
Packaging Specifications

Conforms to IEC Publication 286-3 Ed. 4: 2007-06

Tape



Reel



4000 pcs. per 180 mm (7-inch) reel

Dimension	Model Size			
	0603	0805	1206	1210
A_0	1.2 (.047)	1.6 (.063)	1.9 (.075)	2.9 (.114)
B_0	1.9 (.075)	2.4 (.094)	3.75 (.148)	3.7 (.146)
K_0 MAX.	1.1 (.043)		1.8 (.071)	2.0 (.079)
B_1 MAX.	4.35 (.171)			
D_1 DIA. MIN.	0.3 (.012)			
E_2 MIN.	6.25 (.246)			
P_1	4 (.157)			

Dimension	Model Size			
	0603	0805	1206	1210
F	3.5 (.138)			
W	8.0 (.315)			
T_2 MAX.	3.5 (.138)			
W_1	8.4 + 1.5 (.331 + .059)			
W_2 MAX.	14.4 (.567)			
W_3	7.9 (.311) to 10.9 (.429)			
A DIA.	180 (7.087)			

DIMENSIONS: MM / (INCHES)

Soldering Recommendations for SMD Components

Popular soldering techniques used for surface mounted components are Wave and Infrared Reflow processes. Both processes can be performed with Pb-containing or Pb-free solders.

End Termination	Designation	Recommended and Suitable for	RoHS Compliant
NiSn End Termination	ZVE Series ...Ni R1	Pb-containing and Pb-free soldering	Yes

Wave Soldering

This process is generally associated with discrete components mounted on the underside of printed circuit boards, or for large top-side components with bottom-side mounting tabs to be attached, such as the frames of transformers, relays, connectors, etc. SMD varistors to be wave soldered are first glued to the circuit board, usually with an epoxy adhesive. When all components on the PCB have been positioned and an appropriate amount of time is allowed for adhesive curing, the completed assembly is then placed on a conveyor and run through a single, double wave process.

Infrared Reflow Soldering

These reflow processes are typically associated with top-side component placement. This technique utilizes a mixture of adhesive and solder compounds (and sometimes fluxes) that are blended into a paste. The paste is then screened onto PCB soldering pads specifically designed to accept a particular sized SMD component. The recommended solder paste wet layer thickness is 100 to 300 μm. Once the circuit board is fully populated with SMD components, it is placed in a reflow environment, where the paste is heated to slightly above its eutectic temperature. When the solder paste reflows, the SMD components are attached to the solder pads.

Solder Fluxes

Solder fluxes are generally applied to populated circuit boards to keep oxides from forming during the heating process and to facilitate the flowing of the solder. Solder fluxes can be either a part of the solder paste compound or separate materials, usually fluids. Recommended fluxes are:

- non-activated (R) fluxes, whenever possible
- mildly activated (RMA) fluxes of class L3CN
- class ORLO

Activated (RA), water soluble or strong acidic fluxes with a chlorine content > 0.2 wt. % are NOT RECOMMENDED. The use of such fluxes could create high leakage current paths along the body of the varistor components.

When a flux is applied prior to wave soldering, it is important to completely dry any residual flux solvents prior to the soldering process.

Thermal Shock

To avoid the possibility of generating stresses in the varistor chip due to thermal shock, a preheat stage to within 100 °C of the peak soldering process temperature is recommended. Additionally, SMD varistors should not be subjected to a temperature gradient greater than 4 °C/sec., with an ideal gradient being 2 °C/sec. Peak temperatures should be controlled. Wave and Reflow soldering conditions for SMD varistors with Pb-containing solders are shown on the next page in Fig. 1 and 2 respectively, while Wave and Reflow soldering conditions for SMD varistors with Pb-free solders are shown in Fig. 1 and 3.

Whenever several different types of SMD components are being soldered, each having a specific soldering profile, the soldering profile with the least heat and the minimum amount of heating time is recommended. Once soldering has been completed, it is necessary to minimize the possibility of thermal shock by allowing the hot PCB to cool to less than 50 °C before cleaning.

Soldering Recommendations for SMD Components (Continued)

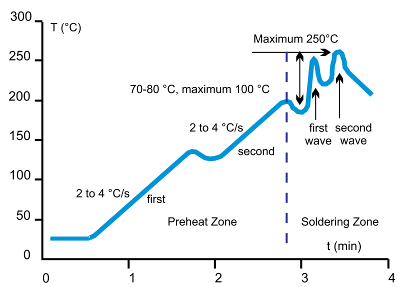


Fig. 1. Wave Soldering Temperature Profile for Pb-free and Pb-containing Soldering

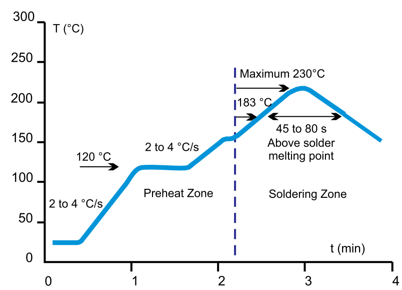


Fig. 2. Infrared Reflow Temperature Profile for Pb-containing Soldering

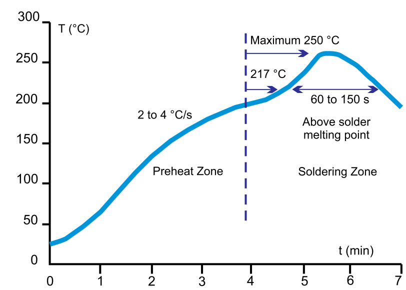


Fig. 3. Reflow Temperature Profile for Pb-free Soldering

Inspection Criteria

When Wave or Infrared Reflow processes are used, the inspection criteria to determine acceptable solder joints will depend on several key variables, principally termination material process profiles.

Pb-containing Wave and IR Reflow Soldering

Solder forms a metallurgical junction with the thin tin-alloy (over the barrier layer), and due to its small volume “climbs” the outer surface of the terminations, so the meniscus will be slightly lower. This optical appearance difference should be taken into consideration when programming visual inspection of the PCB after soldering.

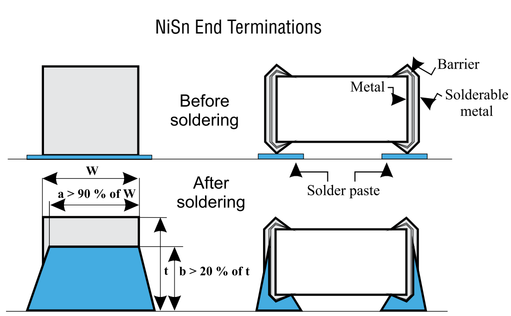


Fig. 4 Soldering Criteria for Wave and IR Reflow Pb-containing Soldering

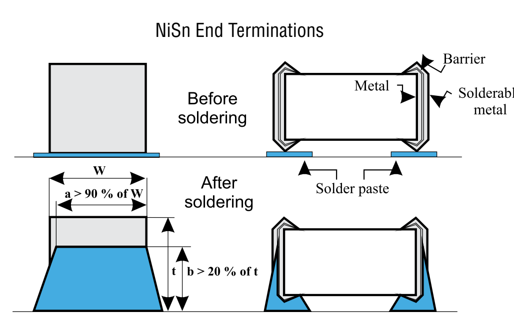


Fig. 5 Soldering Criteria for Wave and IR Reflow Pb-free Soldering

Pb-free Wave and IR Reflow Soldering

Solder forms a metallurgical junction with the entire volume of the end termination, i.e., it diffuses from pad to end termination across the inner side, forming a “mirror” or “negative meniscus. The height of the solder penetration can be clearly seen on the end termination and is always 30 % higher than the chip height.

Since barrier type terminations on Bourns® chips do not require the use of sometimes problematic nickel and tin-alloy electroplating processes, these varistors are truly considered environmentally friendly.

Solder Test and Retained Samples

Reflow soldering test based on J-STD-020D.1 and soldering test by dipping based on IEC 60068- 2 for Pb-free solders are performed on each production lot as shown in the following chart. Test results and accompanying samples are retained for a minimum of two (2) years. The solderability of a specific lot can be checked at any time within this period, should a customer require this information.

Soldering Recommendations for SMD Components (Continued)

Test	Resistance to Flux	Solderability	Static Leaching (Simulation of Reflow Soldering)	Dynamic Leaching (Simulation of Wave Soldering)
Soldering method	Dipping	Dipping	Dipping	Dipping with Agitation
Flux	L3CN, ORL0	L3CN, ORL0, R	L3CN, ORL0, R	L3CN, ORL0, R
Pb Solder	62Sn / 36Pb / 2Ag			
Pb Soldering Temperature (°C)	235 ± 5	235 ± 5	260 ± 5	235 ± 5
Pb-Free Solder	Sn96 / Cu0,4-0,8 / 3-4Ag			
Pb-Free Soldering Temperature (°C)	250 ± 5	250 ± 5	280 ± 5	250 ± 5
Soldering Time (sec.)	2	210	10	> 15
Burn-in Conditions	V_{dcmax}, 48 hours	-	-	-
Acceptance Criterion	dVn < 5 %, i_{dc} must stay unchanged	> 95 % of end termination must be covered by solder	> 95 % of end termination must be intact and covered by solder	> 95 % of end termination must be intact and covered by solder

Rework Criteria - Soldering Iron

Unless absolutely necessary, the use of soldering irons is NOT recommended for reworking varistor chips. If no other means of rework is available, the following criteria must be strictly followed:

- Do not allow the tip of the iron to directly contact the top of the chip
- Do not exceed the following soldering iron specifications:
  Output Power......................................30 Watts Maximum
  Temperature of Soldering Iron Tip.......280 °C Maximum
  Soldering Time....................................10 Seconds Maximum

Storage Conditions

SMD varistors should be used within 1 year of purchase to avoid possible soldering problems caused by oxidized terminals. The storage environment should be controlled, with humidity less than 40 % and temperature between -25 and +45 °C. Varistor chips should always be stored in their original packaged unit.

When varistor chips have been in storage for more than 1 year, and when there is evidence of solderability difficulties, Bourns can "refresh" the terminations to eliminate these problems.

Reliability - Lifetime

Pb-free Wave and IR Reflow Soldering

In general, **reliability** is the ability of a component to perform and maintain its functions in routine circumstances, as well as in hostile or unexpected circumstances.

The Mean life of the ZVX series is a function of:

- Factor of Applied Voltage
- Ambient Temperature

Mean life is closely related to Failure rate (formula).

Mean life (ML) is the arithmetic mean (average) time to failure of a component.

Failure rate is the frequency with which an engineered system or component fails, expressed, for example, in failures per hour. Failure rate is usually time dependent, and an intuitive corollary is that the rate changes over time versus the expected life cycle of a system.

Failure rate formula - calculation

$$\Lambda = \frac{10^9}{ML\ [h]}\ [fit]$$

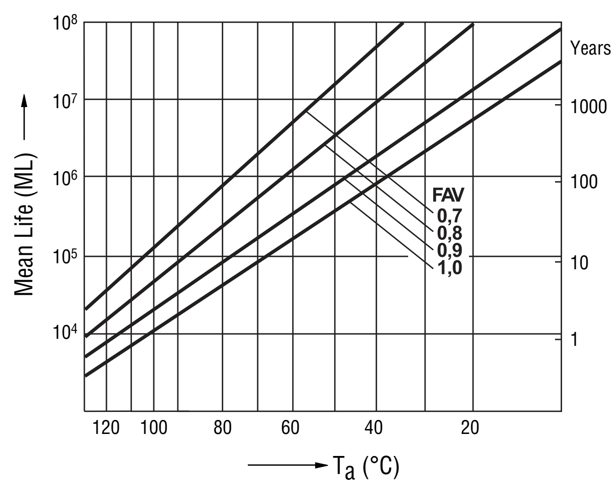
FAV - Factor of Applied Voltage

$$FAV = \frac{V_{apl}}{V_{max}}$$

V_{apl} ....applied voltage

V_{max} ....maxiimum operating voltage

ZVE Series
Mean Life on Arrhenius Model



Reliability Testing Procedures

Varistor test procedures comply with CECC 42200, IEC 1051-1/2 (and AEC-Q200, if applicable). Test results are available upon customer request. Special tests can be performed upon customer request.

Reliability Parameter	Test	Tested According to	Condition to be Satisfied after Testing
AC/DC Bias Reliability	AC/DC Life Test	CECC 42200, Test 4.20 or IEC 1051-1, Test 4.20, AEC-Q200 Test 8 - 1000 h at UCT	$\lvert \delta V_n$ (1 mA)$\rvert < 10$ %
Pulse Current Capability	I_{max} 8/20 μs	CECC 42200, Test C 2.1 or IEC 1051-1, Test 4.5 10 pulses in the same direction at 2 pulses per minute at maximum peak current for 10 pulses	$\lvert \delta V_n$ (1 mA)$\rvert < 10$ % no visible damage
Pulse Energy Capability	W_{max} 10/1000 μs	CECC 42200, Test C 2.1 or IEC 1051-1, Test 4.5 10 pulses in the same direction at 1 pulse every 2 minutes at maximum peak current for 10 pulses	$\lvert \delta V_n$ (1 mA)$\rvert < 10$ % no visible damage
WLD Capability	WLD x 10	ISO 7637, Test pulse 5, 10 pulses at rate of 1 per minute	$\lvert \delta V_n$ (1 mA)$\rvert < 15$ % no visible damage
V_{jump} Capability	V_{jump} 5 min.	Increase of supply voltage to $V \geq V_{jump}$ for 1 minute	$\lvert \delta V_n$ (1 mA)$\rvert < 15$ % no visible damage
Environmental and Storage Reliability	Climatic Sequence	CECC 42200, Test 4.16 or IEC 1051-1, Test 4.17 a) Dry heat, 16h, UCT, Test Ba, IEC 68-2-2 b) Damp heat, cyclic, the first cycle: 55 °C, 93 % RH, 24 h, Test Db 68-2-4 c) Cold, LCT, 2 h, Test Aa, IEC 68-2-1 d) Damp heat cyclic, remaining 5 cycles: 55 °C, 93 % RH, 24 h/cycle, Test Bd, IEC 68-2-30	$\lvert \delta V_n$ (1 mA)$\rvert < 10$ %
	Thermal Shock	CECC 42200, Test 4.12, Test Na, IEC 68-2-14, AEC-Q200 Test 16, 5	$\lvert \delta V_n$ (1 mA)$\rvert < 10$ % no visible damage
	Steady State Damp Heat	CECC 42200, Test 4.17, Test Ca, IEC 68-2-3, AEC-Q200 Test 6, 56 days, 40 °C, 93 % RH, AEC-Q200 Test 7: Bias, Rh, T all at 85.	$\lvert \delta V_n$ (1 mA)$\rvert < 10$ %
	Storage Test	IEC 68-2-2, Test Ba, AEC-Q200 Test 3, 1000 h at maximum storage temperature	$\lvert \delta V_n$ (1 mA)$\rvert < 5$ %

Continued on Next Page

Reliability Testing Procedures (Continued)

Reliability Parameter	Test	Tested According to	Condition to be Satisfied after Testing
Mechanical Reliability	Solderability	CECC 42200, Test 4.10.1, Test Ta, IEC 68-2-20 solder bath and reflow method	Solderable at shipment and after 2 years of storage, criteria: >95% must be covered by solder for reflow meniscus
	Resistance to Soldering Heat	CECC 42200, Test 4.10.2, Test Tb, IEC 68-2-20 solder bath nad reflow method	$\|\delta V_n$ (1 mA)$\| < 5$ %
	Terminal Strength	JIS-C-6429, App. 1, 18N for 60 sec. - same for AEC-Q200 Test 22	No visual damage
	Board Flex	JIS-C-6429, App. 2, 2 mm min. AEC-Q200 test 21 - Board flex: 2 mm flex min.	$\|\delta V_n$ (1 mA)$\| < 2$ % No visible damage
	Vibration	CECC 42200, Test 4.15, Test Fc, IEC 68-2-6, AEC-Q200 Test 14 Frequency range 10 to 55 Hz (AEC: 10-2000 Hz) Amplitude 0.75 m/s^2 or 98 m/s^2 (AEC: 5 g for 20 minutes) Total duration 6 h (3x2 h) (AEC: 12 cycles each of 3 directions) Waveshape - half sine	$\|\delta V_n$ (1 mA)$\| < 2$ % No visible damage
	Mechanical Shock	CECC 42200, Test 4.14, Test Ea, IEC 68-2-27, AEC-Q200 Test 13. Acceleration = 490 m/s^2 (AEC: MIL-STD-202-Method 213), Pulse duration = 11 ms, Waveshape - half sine; Number of shocks = 3x6	$\|\delta V_n$ (1 mA)$\| < 10$ % No visible damage
Electrical Transient Conduction	ISO-7637-1 Pulses	AEC-Q200 Test 30: Test pulses 1 to 3. Also other pulses - freestyle.	$\|\delta V_n$ (1 mA)$\| < 10$ % No visible damage

Terminology

Term	Symbol	Definition
Rated AC Voltage	V_{rms}	Maximum continuous sinusoidal AC voltage (<5 % total harmonic distortion) which may be applied to the component under continuous operation conditions at +25 °C
Rated DC Voltage	V_{dc}	Maximum continuous DC voltage (<5 % ripple) which may be applied to the component under continuous operating conditions at +25 °C
Supply Voltage	V	The voltage by which the system is designated and to which certain operating characteristics of the system are referred; V_{rms} = 1.1 x V
Leakage Current	I_{dc}	The current passing through the varistor at V_{dc} and at +25 °C or at any other specified temperature
Varistor Voltage	V_n	Voltage across the varistor measured at a given reference current (I_n)
Reference Current	I_n	Reference current = 1 mA DC
Clamping Voltage Protection Level	V_c	The peak voltage developed across the varistor under standard atmospheric conditions, when passing an 8/20 μs class current pulse
Class Current	I_c	A peak value of current which is 1/10 of the maximum peak current for 100 pulses at two per minute for the 8/20 μs pulse
Voltage Clamping Ratio	V_c/V_{app}	A figure of merit measure of the varistor clamping effectiveness as defined by the symbols V_c/V_{app}, where (V_{app} = V_{rms} or V_{dc})
Jump Start Transient	V_{jump}	The jump start transient results from the temporary application of an overvoltage in excess of the rated battery voltage. The circuit power supply may be subjected to a temporary overvoltage condition due to the voltage regulation failing or it may be deliberately generated when it becomes necessary to boost start the car.
Rated Single Pulse Transient Energy	W_{max}	Energy which may be dissipated for a single 10/1000 μs pulse of a maximum rated current, with rated AC voltage or rated DC voltage also applied, without causing device failure
Load Dump Transient	WLD	Load Dump is a transient which occurs in automotive environments. It is an exponentially decaying positive voltage which occurs in the event of a battery disconnect while the alternator is still generating charging current with other loads remaining on the alternator circuit at the time of battery disconnect.
Rated Peak Single Pulse Transient Current	I_{max}	Maximum peak current which may be applied for a single 8/20 μs pulse, with rated line voltage also applied, without causing device failure
Rated Transient Average Power Dissipation	P	Maximum average power which may be dissipated due to a group of pulses occurring within a specified isolated time period, without causing device failure at 25 °C
Capacitance	C	Capacitance between two terminals of the varistor measured @ 1 kHz
Non-linearity Exponent	α	A measure of varistor nonlinearity between two given operating currents, I_n and I_1 as described by I = k V exp(a), where: - k is a device constant, - $I_1 < I < I_n$ and - a log (I_1/I_n)/log(V_1/V_n) = 1/log (V_1/V_n), where: - I_r is reference current (1 mA) and V_n is varistor voltage - I_1 = 10 I_n, V_1 is the voltage measured at I_1
Response Time	tr	The time lag between application of a surge and varistor's "turn-on" conduction action
Varistor Voltage Temperature Coefficient	TC	(V_n @ 85 °C - V_n @ 25 °C) / (V_n @ 25 °C) x 60 °C) x 100
Insulation Resistance	IR	Minimum resistance between shorted terminals and varistor surface
Isolation Voltage		The maximum peak voltage which may be applied under continuous operating conditions between the varistor terminations and any conducting mounting surface
Operating Temperature		The range of ambient temperature for which the varistor is designed to operate continuously as defined by the temperature limits of its climatic category
Climatic Category	LCT/UCT/DHD	LCT & UCT = Lower and Upper Category Temperature - the minimum and maximum ambient temperatures for which a varistor has been designed to operate continuously. DHD = Dump Heat Test Duration
Storage Temperature		Storage temperature range without voltage applied
Current/Energy Derating		Derating of maximum values when operated above UCT

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