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FAIRCHILD™

March 2015

FDD8424H

Dual N & P-Channel PowerTrench® MOSFET
N-Channel: 40V, 20A, 24mΩ P-Channel: -40V, -20A, 54mΩ

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 24mΩ at V_{GS} = 10V, I_D = 9.0A

- Max $r_{DS(on)}$ = 30mΩ at V_{GS} = 4.5V, I_D = 7.0A

Q2: P-Channel

- Max $r_{DS(on)}$ = 54mΩ at V_{GS} = -10V, I_D = -6.5A

- Max $r_{DS(on)}$ = 70mΩ at V_{GS} = -4.5V, I_D = -5.6A

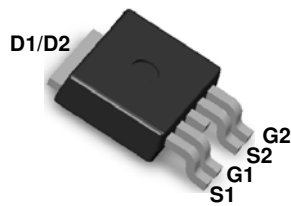- Fast switching speed

- RoHS Compliant

General Description

These dual N and P-Channel enhancement mode Power MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench- process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

Application

- Inverter

- H-Bridge

Dual DPAK 4L

N-Channel   **P-Channel**
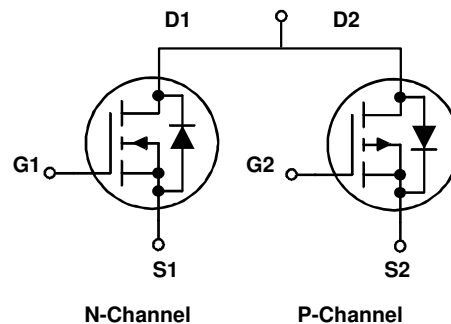
MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter		Q1	Q2	Units
V_{DS}	Drain to Source Voltage		40	-40	V
V_{GS}	Gate to Source Voltage		±20	±20	V
I_D	Drain Current - Continuous (Package Limited)		20	-20	A
	- Continuous (Silicon Limited)	T_C = 25°C	26	-20	
	- Continuous	T_A = 25°C	9.0	-6.5	
	- Pulsed		55	-40	
P_D	Power Dissipation for Single Operation	T_C = 25°C (Note 1)	30	35	W
		T_A = 25°C (Note 1a)	3.1		
		T_A = 25°C (Note 1b)	1.3		
E_{AS}	Single Pulse Avalanche Energy	(Note 3)	29	33	mJ
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150		°C

Thermal Characteristics

$R_{θJC}$	Thermal Resistance, Junction to Case, Single Operation for Q1	(Note 1)	4.1	°C/W
$R_{θJC}$	Thermal Resistance, Junction to Case, Single Operation for Q2	(Note 1)	3.5	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD8424H	FDD8424H	TO-252-4L	13"	16mm	2500 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250µA, V_{GS} = 0V I_D = -250µA, V_{GS} = 0V	Q1 Q2	40 -40			V
$\dfrac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250µA, referenced to 25°C I_D = -250µA, referenced to 25°C	Q1 Q2		34 -32		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 32V, V_{GS} = 0V V_{DS} = -32V, V_{GS} = 0V	Q1 Q2			1 -1	µA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V	Q1 Q2			±100 ±100	nA nA
On Characteristics							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250µA V_{GS} = V_{DS}, I_D = -250µA	Q1 Q2	1 -1	1.7 -1.6	3 -3	V
$\dfrac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250µA, referenced to 25°C I_D = -250µA, referenced to 25°C	Q1 Q2		-5.3 4.8		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10V, I_D = 9.0A V_{GS} = 4.5V, I_D = 7.0A V_{GS} = 10V, I_D = 9.0A, T_J = 125°C	Q1		19 23 29	24 30 37	mΩ
		V_{GS} = -10V, I_D = -6.5A V_{GS} = -4.5V, I_D = -5.6A V_{GS} = -10V, I_D = -6.5A, T_J = 125°C	Q2		42 58 62	54 70 80	
g_{FS}	Forward Transconductance	V_{DS} = 5V, I_D = 9.0A V_{DS} = -5V, I_D = -6.5A	Q1 Q2		29 13		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	Q1 V_{DS} = 20V, V_{GS} = 0V, f = 1MHZ	Q1 Q2		750 1000	1000 1330	pF
C_{oss}	Output Capacitance	Q2	Q1 Q2		115 140	155 185	pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = -20V, V_{GS} = 0V, f = 1MHZ	Q1 Q2		75 75	115 115	pF
R_g	Gate Resistance	f = 1MHz	Q1 Q2	0.1 0.1	1.1 3.3	3.3 9.9	Ω
Switching Characteristics							
$t_{d(on)}$	Turn-On Delay Time	Q1 V_{DD} = 20V, I_D = 9.0A, V_{GS} = 10V, R_{GEN} = 6Ω	Q1 Q2		7 7	14 14	ns
t_r	Rise Time		Q1 Q2		13 3	24 10	ns
$t_{d(off)}$	Turn-Off Delay Time	Q2 V_{DD} = -20V, I_D = -6.5A, V_{GS} = -10V, R_{GEN} = 6Ω	Q1 Q2		17 20	31 36	ns
t_f	Fall Time		Q1 Q2		6 3	12 10	ns
$Q_{g(TOT)}$	Total Gate Charge	Q1 V_{GS} = 10V, V_{DD} = 20V, I_D = 9.0A	Q1 Q2		14 17	20 24	nC
Q_{gs}	Gate to Source Charge	Q2	Q1 Q2		2.3 3.0		nC
Q_{gd}	Gate to Drain "Miller" Charge	V_{GS} = -10V, V_{DD} = -20V, I_D = -6.5A	Q1 Q2		3.2 3.6		nC

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions		Type	Min	Typ	Max	Units
Drain-Source Diode Characteristics								
I_S	Maximum Continuous Drain to Source Diode Forward Current			Q1 Q2			20 -20	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		(Note 2)	Q1 Q2			55 -40	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = 9.0A V_{GS} = 0V, I_S = -6.5A	(Note 2) (Note 2)	Q1 Q2		0.87 0.88	1.2 -1.2	V
t_{rr}	Reverse Recovery Time	Q1 I_F = 9.0A, di/dt = 100A/s		Q1 Q2		25 29	38 44	ns
Q_{rr}	Reverse Recovery Charge	Q2 I_F = -6.5A, di/dt = 100A/s		Q1 Q2		19 29	29 44	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

Q1

a. 40°C/W when mounted on
   a 1 in^2 pad of 2 oz copper

Scale 1 : 1 on letter size paper

b. 96°C/W when mounted on a
   minimum pad of 2 oz copper

Q2

a. 40°C/W when mounted on
   a 1 in^2 pad of 2 oz copper

Scale 1 : 1 on letter size paper

b. 96°C/W when mounted on a
   minimum pad of 2 oz copper
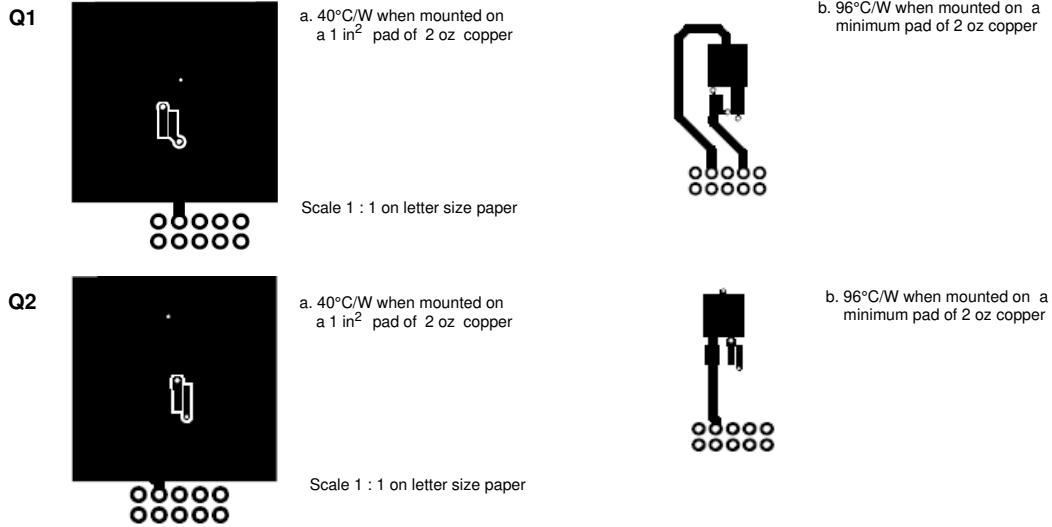
2. Pulse Test: Pulse Width < 300µs, Duty cycle < 2.0%.
3. Starting T_J = 25°C, N-ch: L = 0.3mH, I_{AS} = 14A, V_{DD} = 40V, V_{GS} = 10V; P-ch: L = 0.3mH, I_{AS} = -15A, V_{DD} = -40V, V_{GS} = -10V.

Typical Characteristics (Q1 N-Channel) $T_J = 25°C$ unless otherwise noted
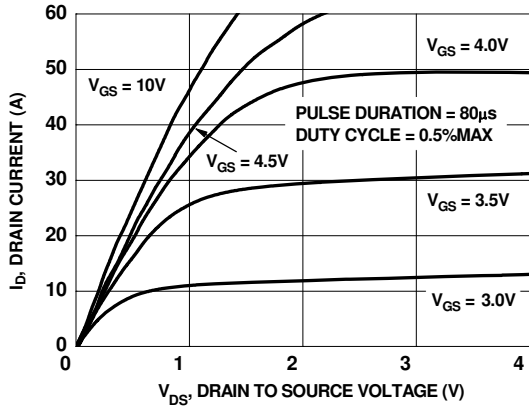
Figure 1. On- Region Characteristics
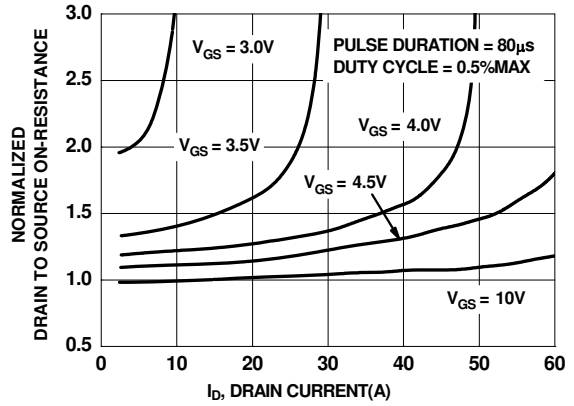
Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage
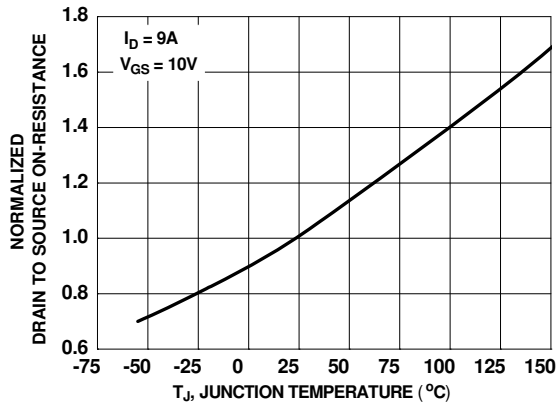
Figure 3. Normalized On-Resistance vs Junction Temperature
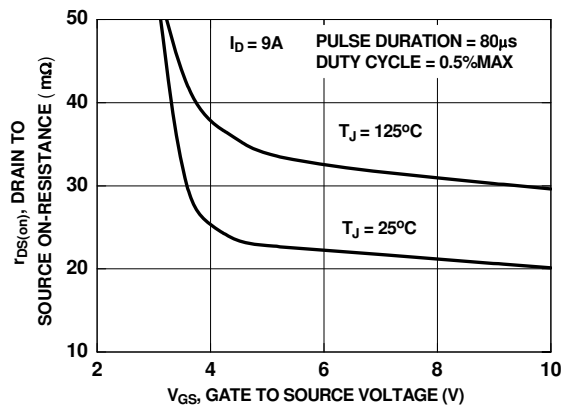
Figure 4. On-Resistance vs Gate to Source Voltage
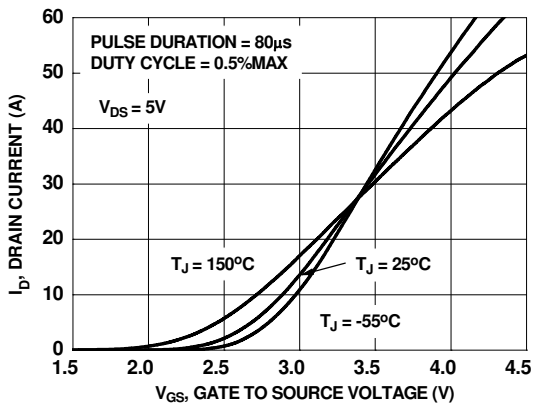
Figure 5. Transfer Characteristics
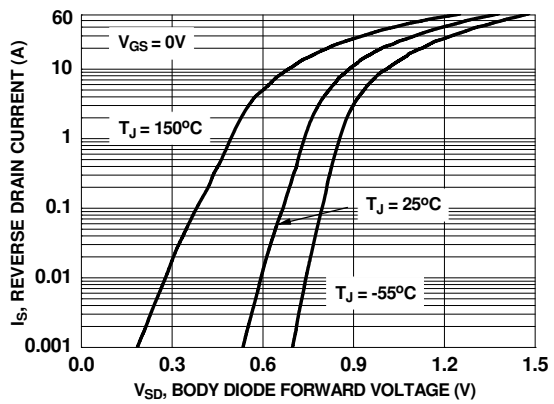
Figure 6. Source to Drain Diode Forward Voltage vs Source Current

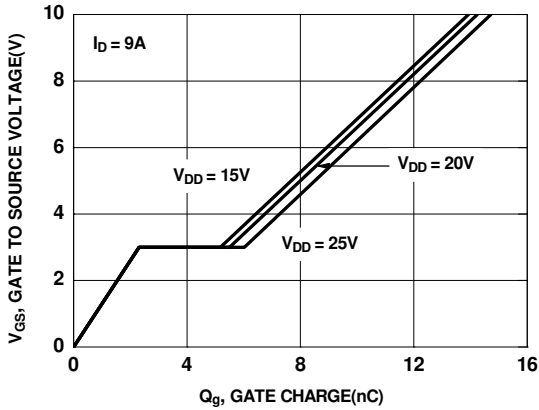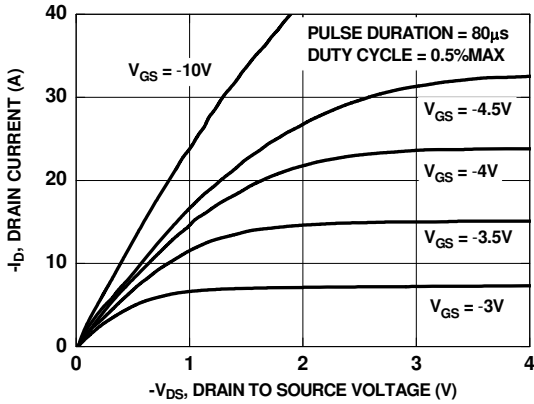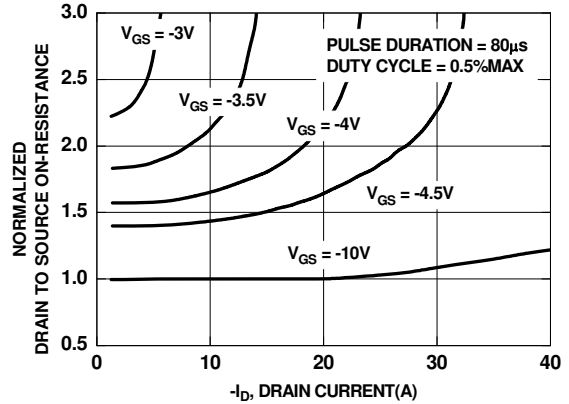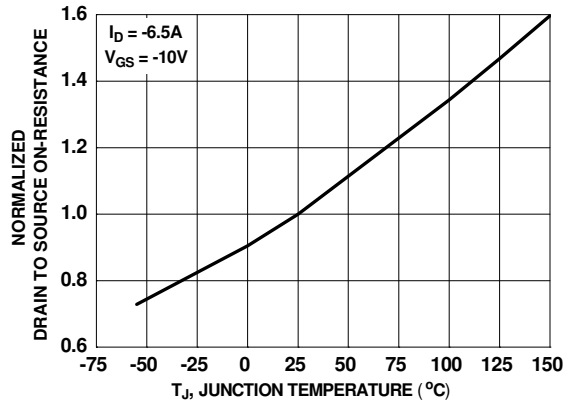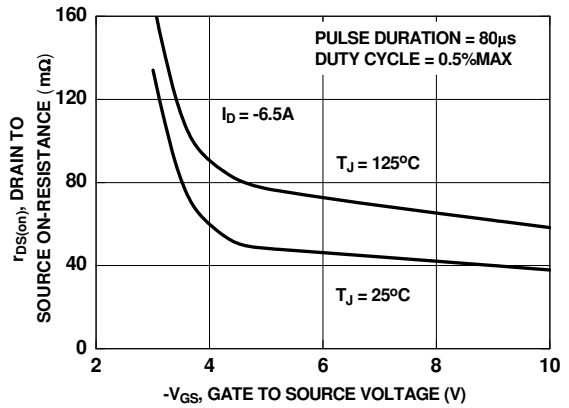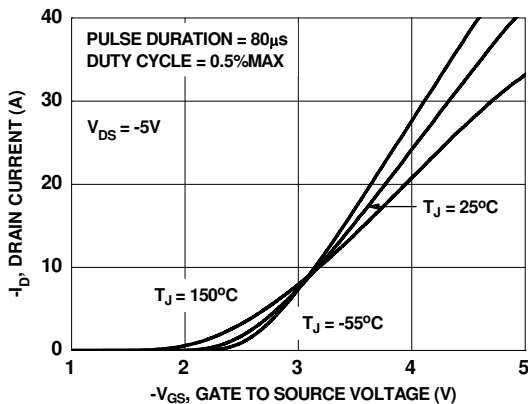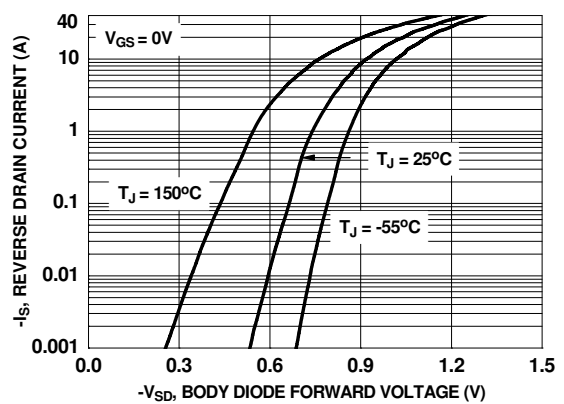## Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted
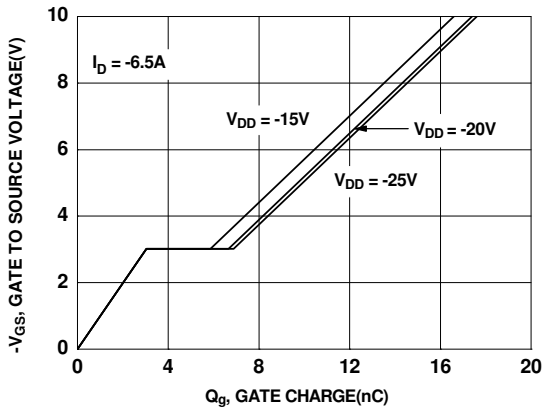

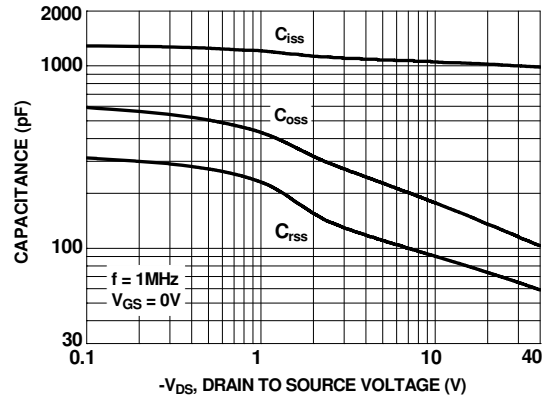**Figure 7. Gate Charge Characteristics**
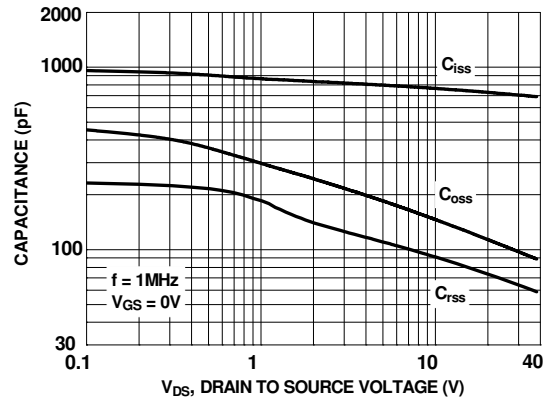
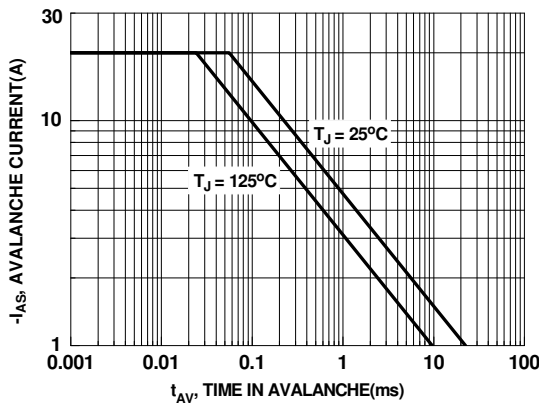**Figure 8. Capacitance vs Drain to Source Voltage**
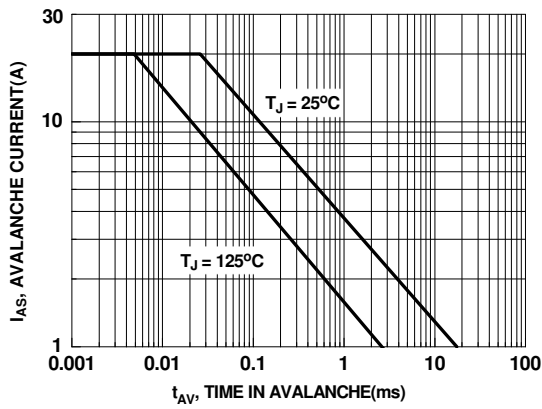
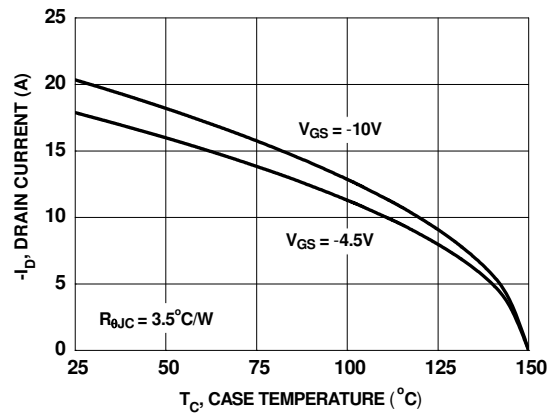**Figure 9. Unclamped Inductive Switching Capability**
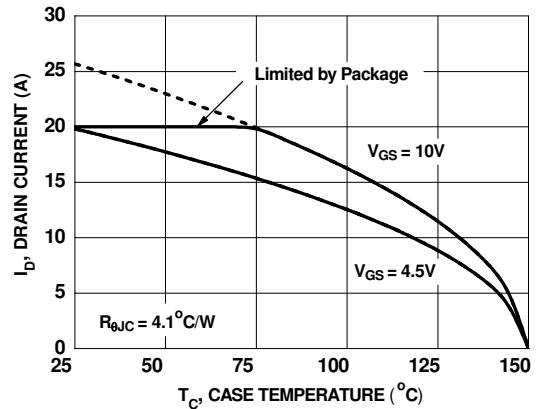

Figure 10. Maximum Continuous Drain Current vs Case Temperature
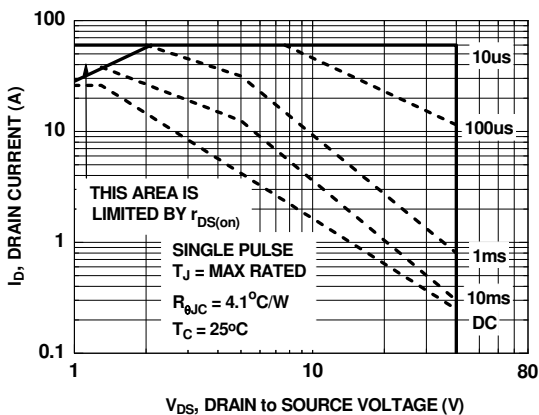

Figure 11. Forward Bias Safe Operating Area
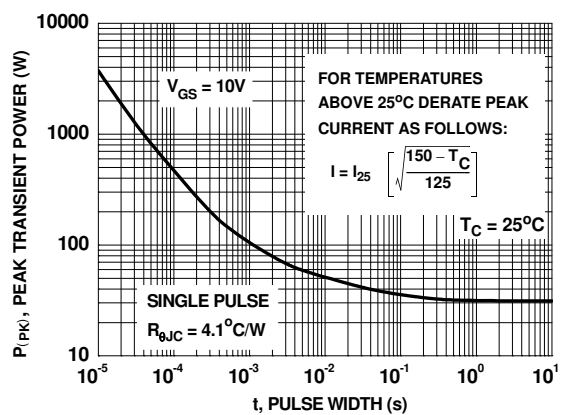
Figure 12. Single Pulse Maximum Power Dissipation
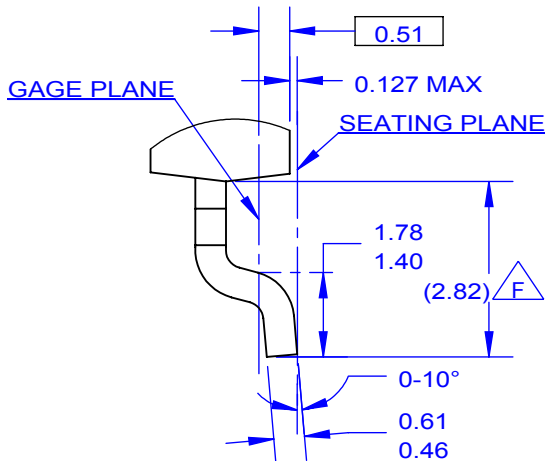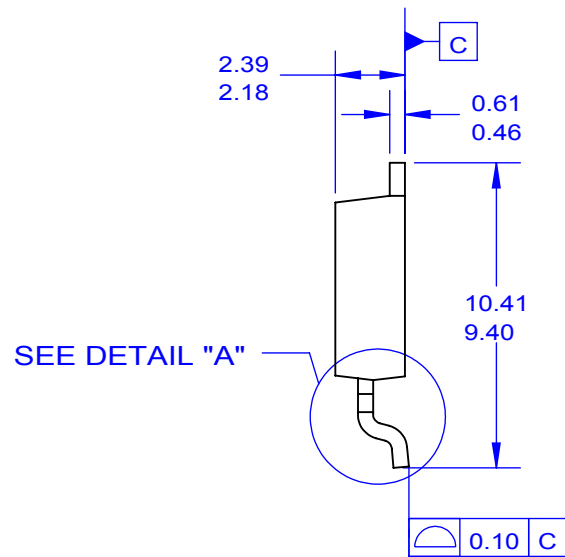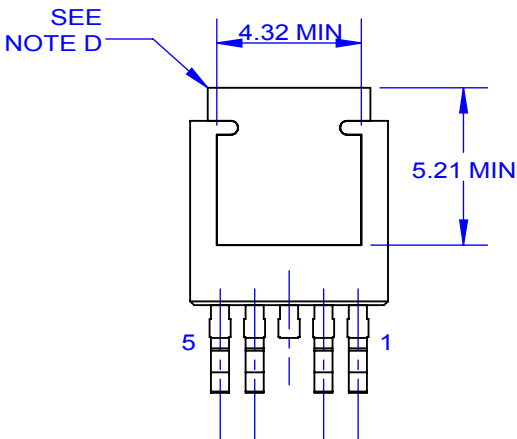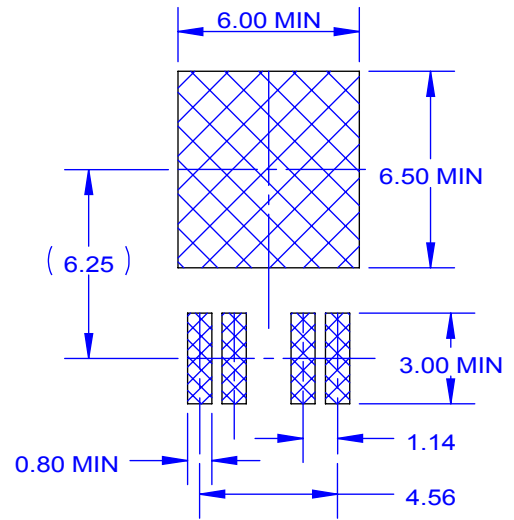
Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted
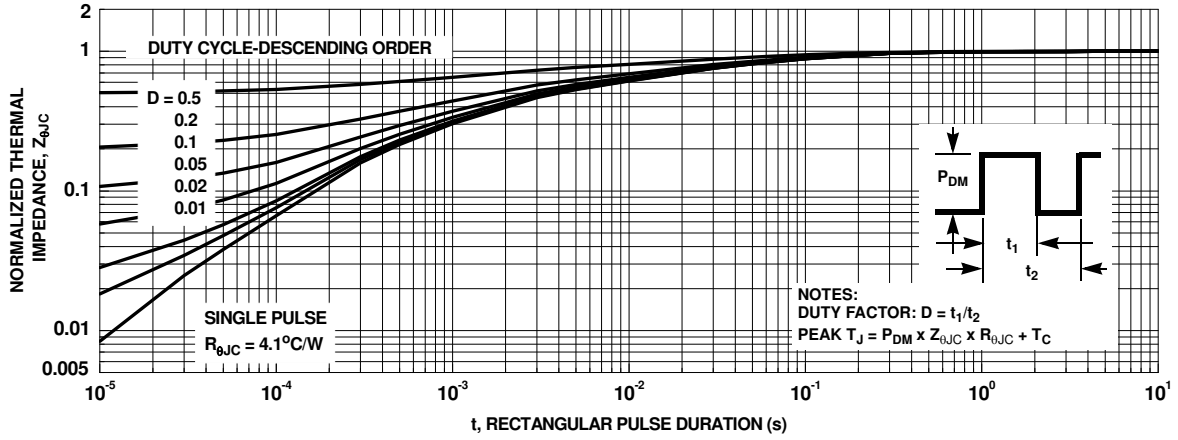
Figure 13. Transient Thermal Response Curve

The chart shows:
- NORMALIZED THERMAL IMPEDANCE, $Z_{\theta JC}$ (vertical axis)
- t, RECTANGULAR PULSE DURATION (s) (horizontal axis)
- DUTY CYCLE-DESCENDING ORDER
- D = 0.5, 0.2, 0.1, 0.05, 0.02, 0.01
- SINGLE PULSE
- $R_{\theta JC}$ = 4.1°C/W
- NOTES:
- DUTY FACTOR: D = t_1/t_2
- PEAK T_J = P_{DM} x $Z_{\theta JC}$ x $R_{\theta JC}$ + T_C

Typical Characteristics (Q2 P-Channel) $T_J = 25°C$ unless otherwise noted

Figure 14. On- Region Characteristics

Figure 15. Normalized on-Resistance vs Drain Current and Gate Voltage

Figure 16. Normalized On-Resistance vs Junction Temperature

Figure 17. On-Resistance vs Gate to Source Voltage

Figure 18. Transfer Characteristics

Figure 19. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q2 P-Channel) T_J = 25°C unless otherwise noted

Figure 20. Gate Charge Characteristics

Figure 21. Capacitance vs Drain to Source Voltage

Figure 22. Unclamped Inductive Switching Capability

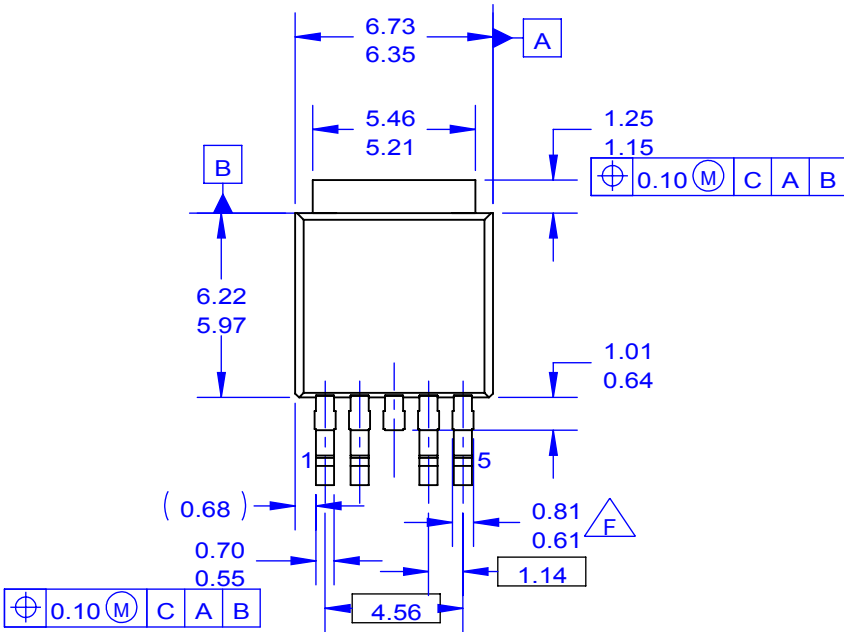Figure 23. Maximum Continuous Drain Current vs Case Temperature
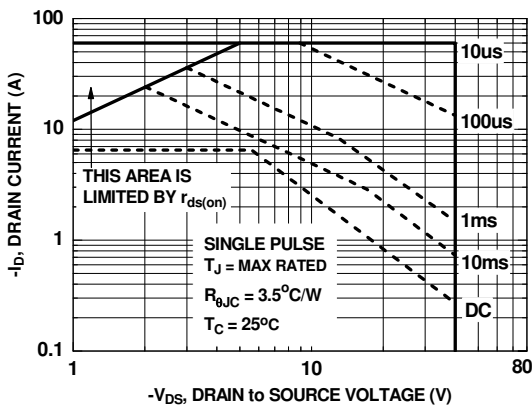
Figure 24. Forward Bias Safe Operating Area
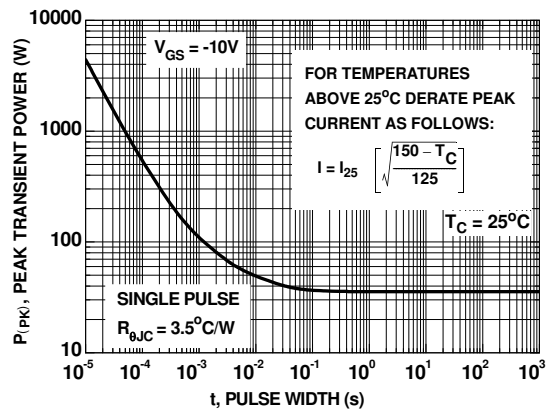
Figure 25. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 P-Channel) T_J = 25°C unless otherwise noted

Figure 26. Transient Thermal Response Curve

In the figure:

NORMALIZED THERMAL IMPEDANCE, $Z_{\theta JC}$

DUTY CYCLE-DESCENDING ORDER

D = 0.5
0.2
0.1
0.05
0.02
0.01

SINGLE PULSE

$R_{\theta JC}$ = 3.5°C/W

t, RECTANGULAR PULSE DURATION (s)

P_{DM}

t_1

t_2

NOTES:
DUTY FACTOR: D = t_1/t_2
PEAK T_J = P_{DM} x $Z_{\theta JC}$ x $R_{\theta JC}$ + T_C

6.73
6.35

A

5.46
5.21

1.25
1.15

⊕ | 0.10 Ⓜ | C | A | B

B

6.22
5.97

1.01
0.64

1

5

(0.68)

0.81
0.61 /F\

0.70
0.55

1.14

⊕ | 0.10 Ⓜ | C | A | B

4.56

6.00 MIN

6.50 MIN

(6.25)

3.00 MIN

0.80 MIN

1.14

4.56

SEE
NOTE D

4.32 MIN

5.21 MIN

5

1

2.39
2.18

C

0.61
0.46

10.41
9.40

SEE DETAIL "A"

⌓ | 0.10 | C

0.51

0.127 MAX

GAGE PLANE

SEATING PLANE

1.78
1.40

(2.82) /F\

0-10°

0.61
0.46

DETAIL A
SCALE 2:1

NOTES: UNLESS OTHERWISE SPECIFED

A. THIS PACKAGE CONFORMS TO JEDEC, TO252
   VARIATION AD.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS,
   MOLD FLASH AND TIE BAR PROTRUSIONS
D. HEATSINK TOP EDGE COULD BE IN CHAMFERED
   CORNERS OR EDGE PROTRUSION.
E. DIMENSIONS AND TOLERANCES AS PER ASME
   Y14.5-2009.
/F\ EXCEPTION TO TO-252 STANDARD.
G. FILE NAME: TO252B05REV3
H. FAIRCHILDSEMICONDUCTOR

PUBLICATION ORDERING INFORMATION