MLA-06183A

5 - 18 GHz Low-Noise MMIC Amplifier
Data Sheet

FEATURES

- **Wide Band:** 5 to 18 GHz
- **NF (ext match):** 3.4 dB @ 6 GHz
  3.0 dB @ 12 GHz
  3.7 dB @ 18 GHz
- **P-1dB:** 21 dBm
- **OIP3:** 29 dBm
- **Gain:** 19 db
- **Bias Condition:** VDD = 4.5V
  IDD = 135 mA
- **50-Ohm On-chip Matching**
- **Unconditionally Stable from 50 MHz to 20 GHz**

APPLICATIONS

- **Microwave Radios**
- **Satellite Communications**
- **EW Systems**
- **Commercial Wireless Systems**

DESCRIPTION

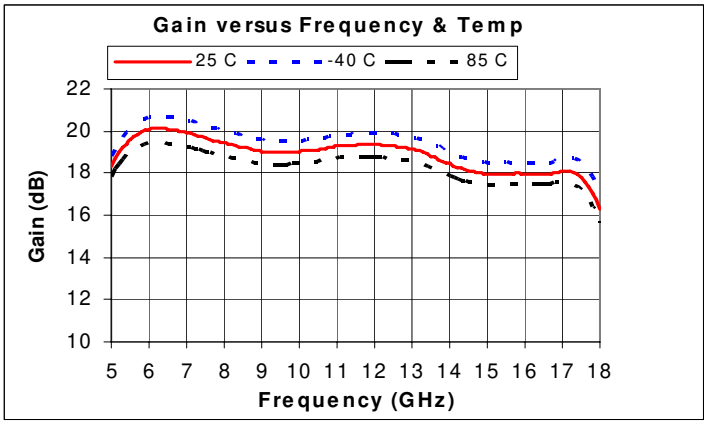
The MLA-06183A is a fully-matched 2-stage broadband low-noise MMIC amplifier utilizing high-reliability low-noise GaAs PHEMT technology. This MMIC is suited for microwave radios, wideband EW, satellite communications, instrumentation, and commercial communication systems, where low-noise figure and high-gain are desirable. It has excellent gain of 19 dB and Noise Figure of 3 dB @ 12 GHz. Typical P-1dB is 21 dBm and OIP3 is + 29 dBm @ 12 GHz. It has on-chip bias circuit, choke, and DC blocking to provide bias stability and ease of use.

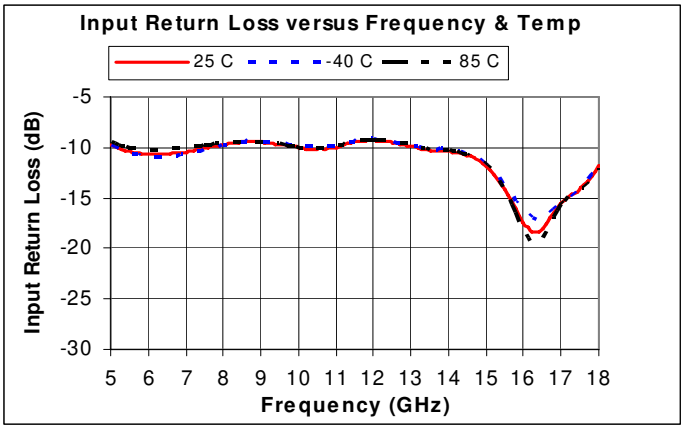
ELECTRICAL SPECIFICATIONS: *VDD1, VDD2=+4.5V,VG2/VG2=-0.025 (2), IDD=135mA, Ta=25 C, ZO=50 ohm (1)*

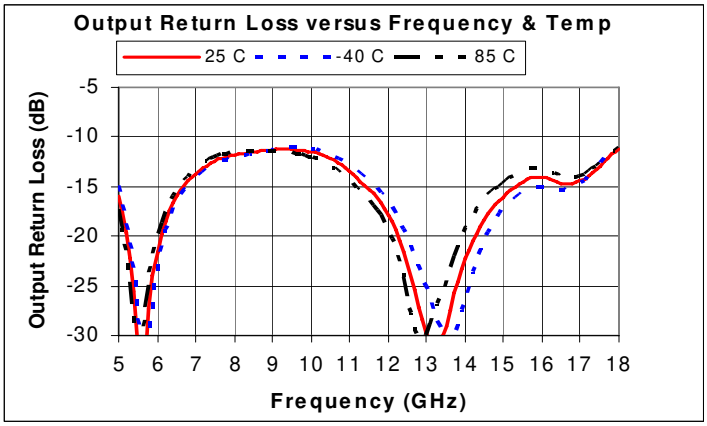
PARAMETER	TEST CONDITIONS	TYPICAL DATA	UNITS
Frequency Range		5-18	GHz
Gain	6 - 8 GHz 8 - 14 GHz 14 - 17.5 GHz 18 GHz	20 19 18 16	dB
Gain Flatness	6 - 14 GHz 14 - 18 GHz	0.75 1.25	+/-dB
Input Return Loss	6 - 14 GHz 14 - 18 GHz	9 12	dB
Output Return Loss		12	dB
Output P1dB	6 GHz 12 GHz 18 GHz	17 21 22	dBm
Output IP3 @ 0 dBm/tone, 1 MHz separation	6 GHz 12 GHz 18 GHz	29 29 27	dBm
Noise Figure	6 GHz 12 GHz 18 GHz	3.4 3.0 3.7	dB
Operating Bias Conditions: VDD1, VDD2 IDD	VG1,VG2=-0.025V, typical	+ 4.5 135	V mA
Stability Factor K	0.05 to 20 GHz	> 1	

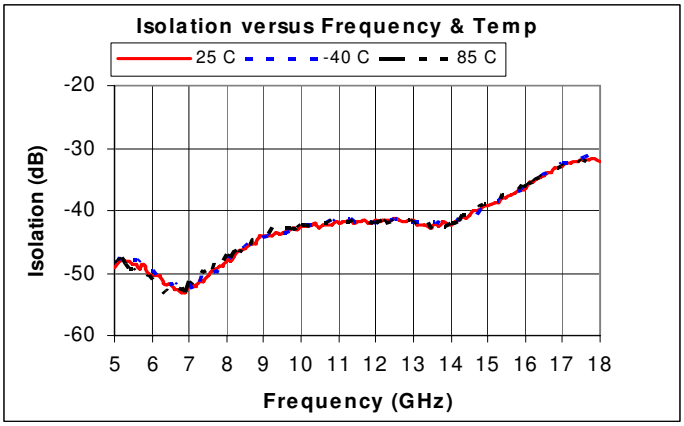
(1) All data is measured on 50 Ohm carrier, with Dual-Bias Supply and stub tuning shown in the datasheet assembly diagram.
(2) Since the VG bias setting has typical range of -0.1 to +0.1V, VG1, VG2 bias inputs may be directly grounded/bonded to DC ground to convert to single +ve supply operation such that VG = 0V. The bias current will then be fixed and cannot be controlled or shut down by VG input.

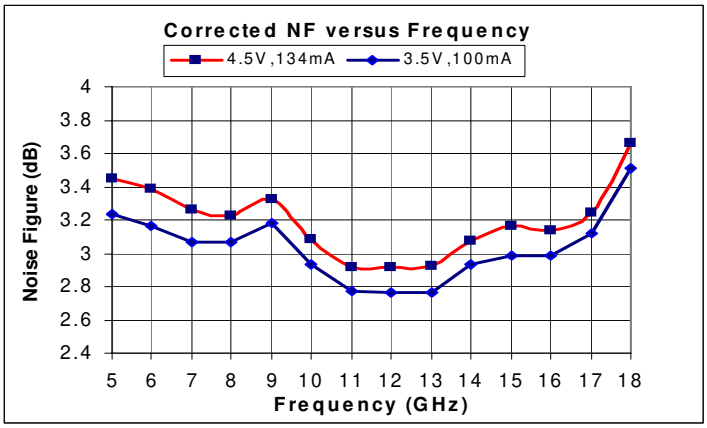
TYPICAL RF PERFORMANCE: *VDD1, VDD2=+4.5V,VG2/VG2=-0.025 (2), IDD=135mA, Ta=25 C, ZO=50 ohm (1)*

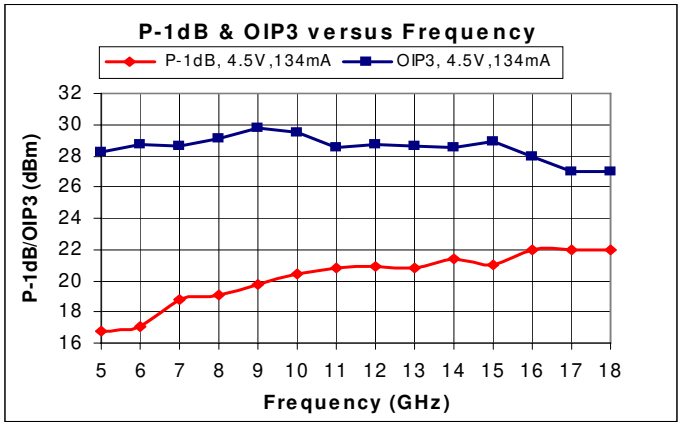












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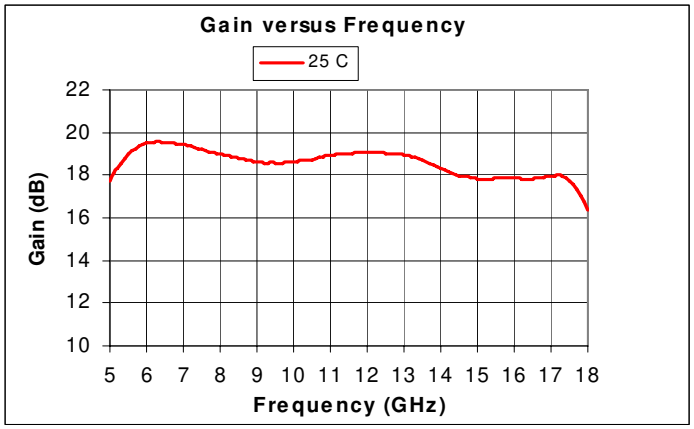
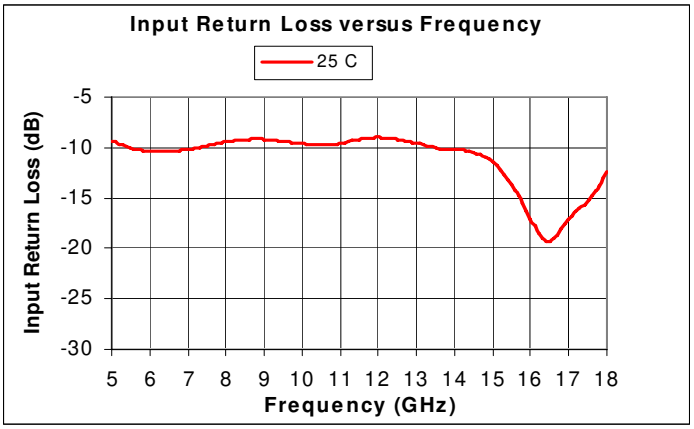
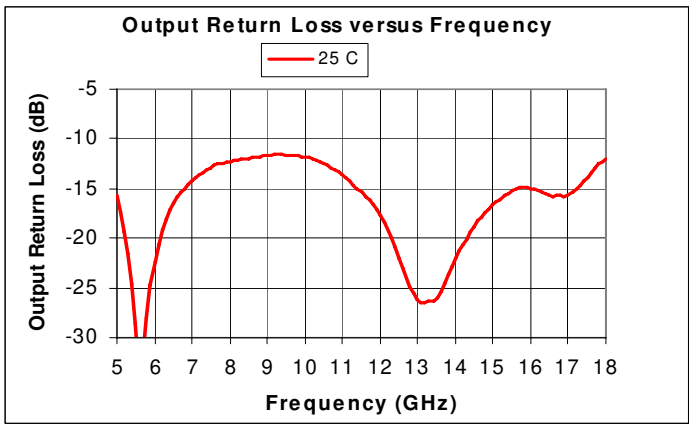
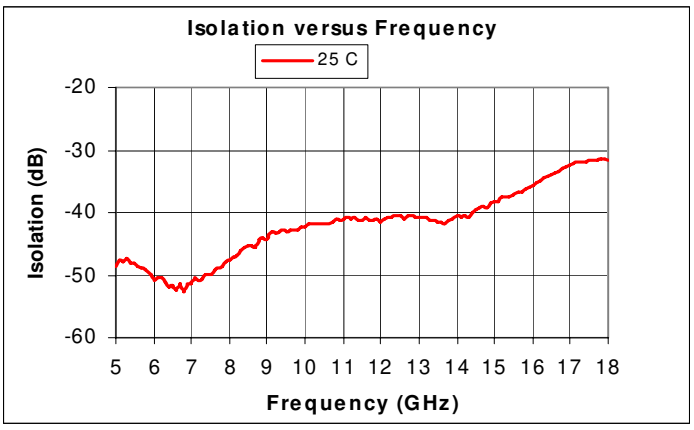
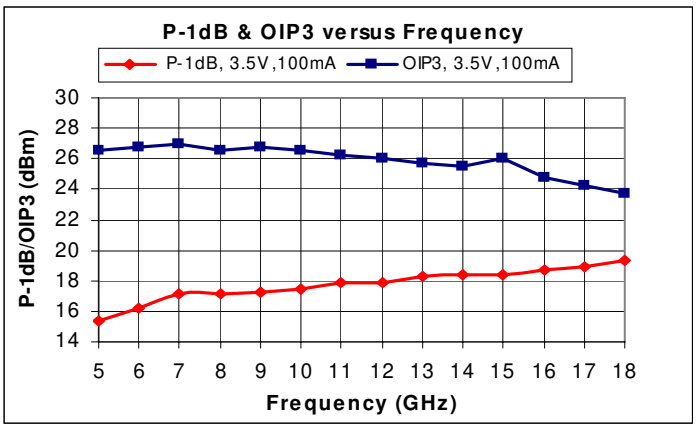








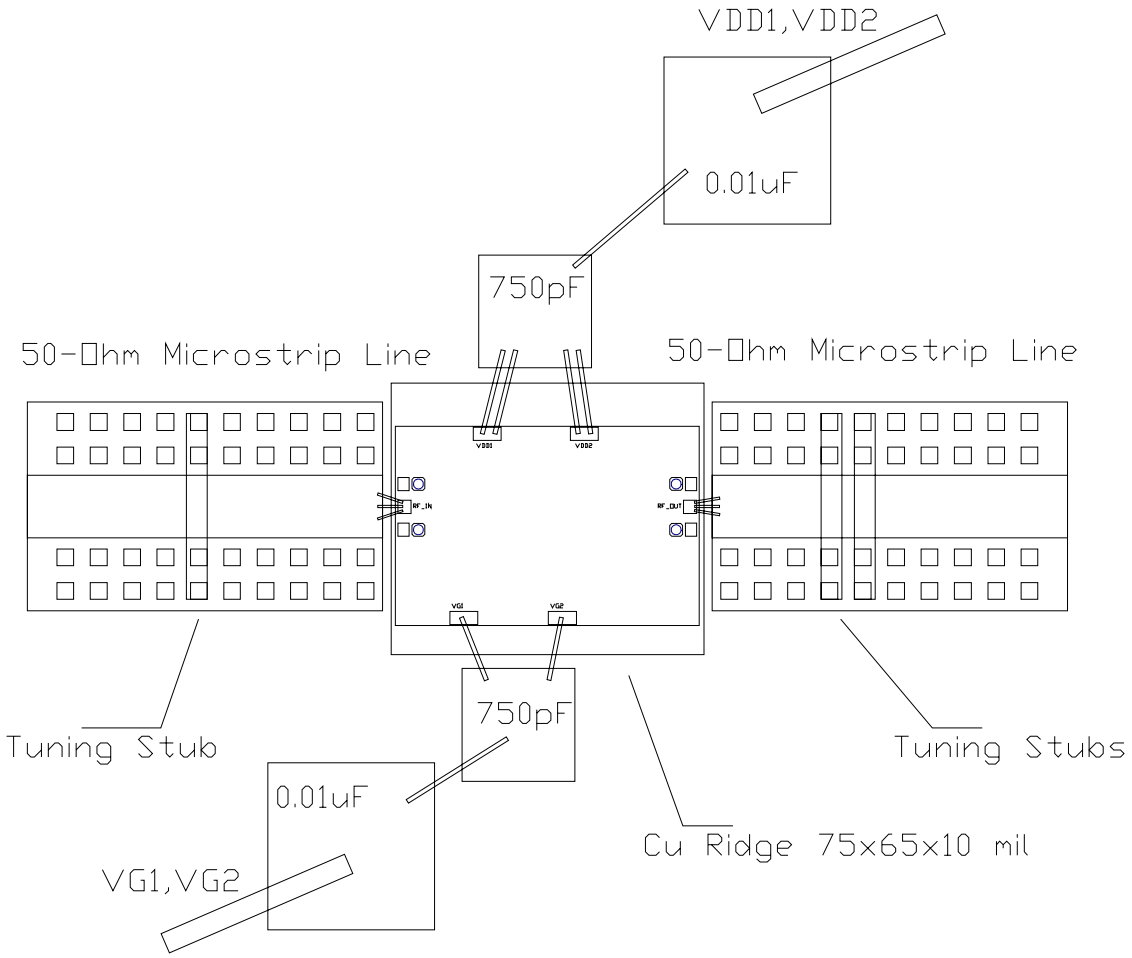


ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETERS	UNITS	MAX
VDD	Drain Voltage	V	5.5
IDD	Drain Current	mA	200
Pdiss	DC Power Dissipation	W	0.7
Pin max	RF Input Power	dBm	+13
Toper	Operating Case/Lead Temp Range	ºC	-40 to +85
Tch	Channel Temperature	ºC	150
Tstg	Storage Temperature	ºC	-60 to 150

Exceeding any on of these limits may cause permanent damage.

ASSEMBLY DIAGRAM

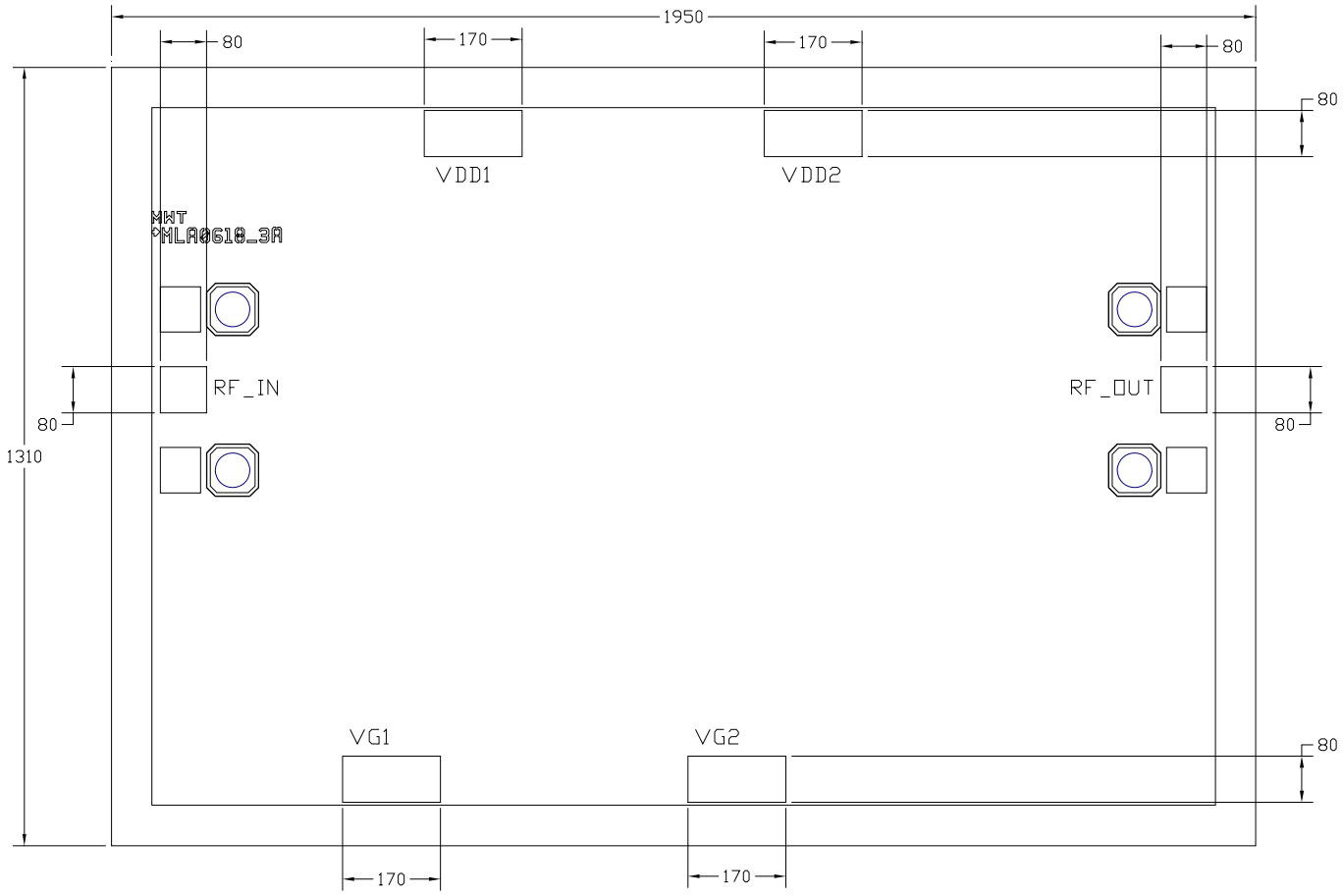


Notes:

1) 1st Close-in Bypass cap values must be at least 100pF and placed < 30mil from chip edge. The large bypass cap 0.01uF is also recommended to be as close to chip as possible.
2) RF IN/OUT Bonds must be 3 wires of length < 10 mil & 0.7 mil diameter for best RF performance.
3) 2 Tuning stubs (5 x 50 mil each) on the 50 ohm line are required on output side about 25 mil from bond edge for good output return loss especially at frequencies > 15 GHz . Stub size & location may be tuned for best RF performance . All data shown include the tuning stubs.
4) 1 Tuning stub (5 x 40 mil) on the 50 ohm line is required on input side about 40 mil from bond edge for good input return loss over the full band. Stub size & location may be tuned for best RF performance . All data shown includes the tuning stubs.

MECHANICAL INFORMATION

Outline Drawing



Notes:

1) Die Size: 1.95 x 1.31 x 0.1 mm.
2) RFIN, RFOUT Bond Pad Size is: 80 x 80 micron.
   VDD1, VDD2, VG1 and VG2 Bond Pad Size is: 80 x 170 micron.
3) Backside of chip is metalized and provides DC and RF Ground with on-chip vias.
4) Bond Pad and Backside metallization: Gold.

Functional Diagram