ANALOG DEVICES

Circuit Note
CN-0535

Circuits from the Lab® reference designs are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit https://www.analog.com/CN0535.

Circuits from the Lab®
Reference Designs

Devices Connected/Referenced

AD7768-1	DC to 204 kHz, Dynamic Signal Analysis, Precision 24-bit ADC with Power Scaling	AD8628	Zero-Drift, Single-Supply, Rail-to-Rail Input/Output Op Amp
LTC6373	36 V, Fully Differential, Programmable Gain, Instrumentation Amplifier	LT3095	Dual-Channel, Low Noise, Bias Generators
ADA4945-1	High Speed, ±0.1 µV Offset Drift, Fully Differential Amplifier	ADP2300	1.2 A, 20 V, 700 kHz, Nonsynchronous Step-Down Regulator
ADR444	Ultralow Noise, LDO XFET® 4.096 V Voltage Reference with Current Sink and Source	ADP7182	−28 V, −200 mA, Low Noise, Linear Regulator

High Performance, Alias Free Measurement Platform for Flexible Data Acquisition System

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards
   CN0535 Circuit Evaluation Board (EVAL-CN0535-FMCZ)
   System Demonstration Platform Board (EVAL-SDP-CH1Z)
Design and Integration Files
   Schematics, Layout Files, Bill of Materials, Software

CIRCUIT FUNCTION AND BENEFITS

A data acquisition (DAQ) system measures real-world physical phenomenon, such as temperature, force, acceleration, or vibration, converting measurements into digital values for data processing, storage, or transmission to a remote location. A typical DAQ system is comprised of a sensor, analog filtering and signal conditioning circuitry, an analog-to-digital converter (ADC), and a digital controller. Components for a DAQ solution are selected on a per application basis. Some DAQ systems are designed to minimize the overall system dc error from the sensor, with fast settling filters for control loop or multiplexed applications. Others are designed to provide superior ac performance, with low distortion and flat frequency response.

The DAQ system shown in Figure 1 has simplified many of these design challenges into a single, flexible DAQ platform that can be used across a wide range of ac and dc applications.

The wide input voltage range, high input impedance, and high input common-mode voltage allows most sensors and signal sources to be connected directly to the input, without additional signal conditioning. The system has a programmable gain block for attenuation or amplification of the input signal to optimally utilize the input range of the ADC.
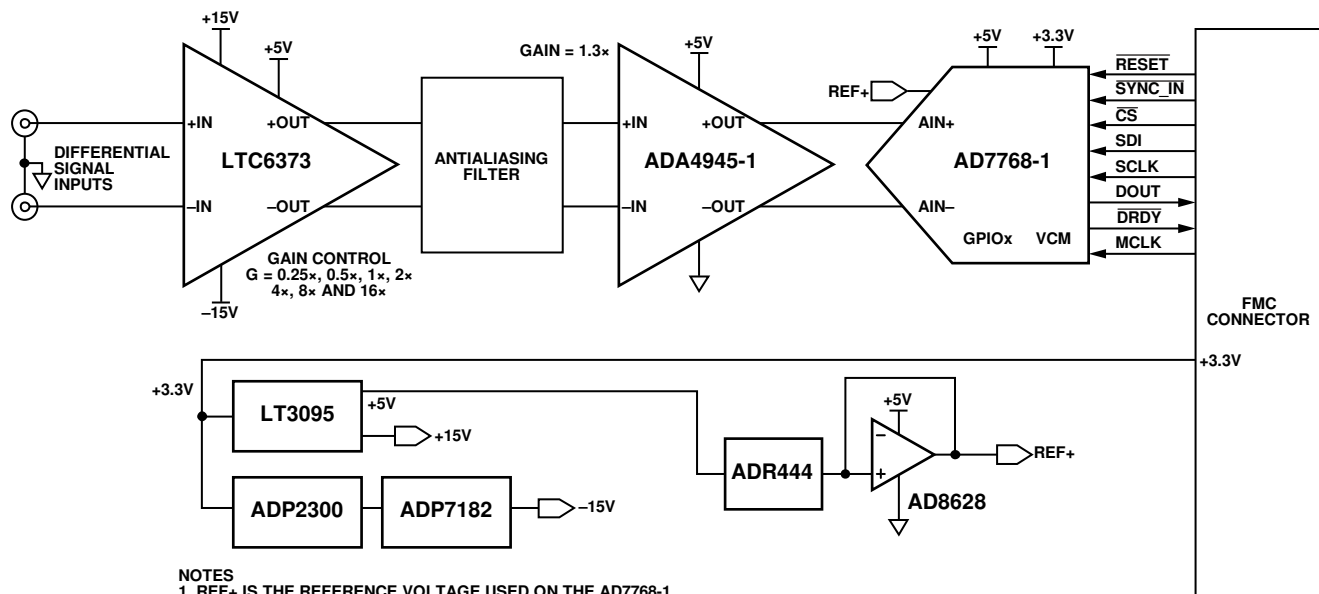
The dc and ac performance of this system have been optimized to provide exceptional performance across the entire analog input bandwidth. The low input bias current minimizes the dc error due to the output impedance of the sensor, and the high common-mode rejection ratio (CMRR) minimizes the impact of the common-mode noise pickup from the environment, especially when the sensor is located far from the DAQ system, which keeps the dc errors to a minimum, while not making sacrifices to the ac performance of the converter.

The ADC has fully programmable digital filters with adjustable bandwidth and data rate that can be tailor fit to specific system requirements. The analog filter of the system rejects frequencies at multiples of the sampling frequency, eliminating aliasing concerns.

SIMPLIFIED CIRCUIT DIAGRAM

Figure 1. Simplified Circuit Diagram (All Connection and Decoupling Capacitors Are Not Shown)

CIRCUIT DESCRIPTION

ADC

The heart of the solution is the AD7768-1, which is a low power, high performance, Σ-Δ ADC, with a Σ-Δ modulator and digital filter for precision conversion of both ac and dc signals. The AD7768-1 offers the user flexibility to configure and optimize for input bandwidth vs. output data rate (ODR) vs. power dissipation.

The ODR can be programmed on a per application requirement. Use the following equation to calculate the ODR of the AD7768-1:

$$ODR = (FMOD/DEC\ RATE)$$

where:
FMOD is the AD7768-1 modulator frequency.
DEC_RATE is the decimation rate.

Use the following equation to calculate FMOD:

$$FMOD = (MCLK/MCLK\ DIV)$$

where:
MCLK is the master clock frequency.
MCLK_DIV is the ratio between MCLK applied and the clock used by the ADC modulator.

The AD7768-1 offers extensive digital filtering capabilities that meet a wide range of system requirements. The filter options allow configuration for frequency domain measurements with tight gain error over frequency, linear phase response requirements (a wideband, low ripple, finite impulse response (FIR) filter), a low latency path (sinc5 or sinc3) for use in control loop applications, and measuring dc inputs with the ability to configure the sinc3 filter to reject a line frequency of either 50 Hz or 60 Hz. All filters offer programmable decimation.

The digital filter dictates the overall system bandwidth. For typical digital filter settings, see Table 1 for the input signal bandwidth. The −3 dB bandwidth for a selected digital filter can also be calculated by using the following:

$$Wideband\ Low\ Ripple\ FIR\ Filter = 0.433 \times ODR$$

$$Sinc5\ Low\ Latency\ Filter = 0.204 \times ODR$$

$$Sinc3\ Low\ Latency\ Filter = 0.2617 \times ODR$$

Table 1. Maximum Input Signal Bandwidth vs. Digital Filter

Digital Filter	Decimation Rate	ODR (kSPS)	Input Signal Bandwidth (kHz)
Low Ripple FIR	32	250	108.2
Sinc5	8	1000	204
Sinc3	32	250	65.425

If the application filter requirements are outside of the default filter options, the user has the option of designing and uploading a custom digital filter to memory. This upload overwrites the default low ripple FIR filter coefficients.

The AD7768-1 has internal calibration registers that can be programmed to provide offset and gain correction for the full input path from the sensor to the input signal conditioning to the ADC.

Table 2 shows an example of the errors before and after writing to the calibration registers.

Table 2. System Offset and Gain Error Using Calibration Registers

Error	Before Calibration	After Calibration
Offset	−420.3 µV	2.319 µV
Gain	3010 ppm	10 ppm

Input Signal Conditioning

The input signal needs some conditioning before it enters the ADC to maximize the input range of the ADC and to remove unwanted information. The signal conditioning is two stages. First, a programmable gain instrumentation amplifier (PGIA) can attenuate or amplify the signal, and then an antialiasing filter (AAF) can remove artifacts that can compromise signal integrity.

PGIA

The LTC6373 is a fully differential PGIA that offers signal attenuation and amplification for different input signal amplitudes ranging from 0.25× to 16×. Table 3 shows the gain pin configuration settings for the LTC6373 and its corresponding gain.

Table 3. LTC6373 Gain Setting

A2	A1	A0	Gain
Logic High	Logic high	Logic high	Shutdown
Logic High	Logic high	Logic low	0.25
Logic High	Logic low	Logic high	0.5
Logic High	Logic low	Logic low	1
Logic Low	Logic High	Logic high	2
Logic Low	Logic High	Logic low	4
Logic Low	Logic low	Logic high	8
Logic Low	Logic low	Logic low	16

The low 20 pA maximum input bias current and high (1000 GΩ) input impedance of the LTC6373 enables the solution to be easily driven by sensors and H-bridge circuits.

The LTC6373 helps protect the ADC and the ADC driver from overvoltage by limiting its output voltage to the same supply rail used for the ADC driver and the ADC input. This feature can be achieved by using the same supply for the V^+_{OUT} pin of the LTC6373, for the $+V_S$ pin of ADA4945-1, and for the AVDD1 pin of AD7768-1.

The gain bandwidth product (GBP) of the LTC6373 increases at higher gains, which allows for higher bandwidth and minimum phase variation across gain settings. This feature is difficult to implement for discrete PGIA designs because it requires dedicated frequency compensation for each gain setting. Figure 2 shows the gain vs. frequency performance of the LTC6373.
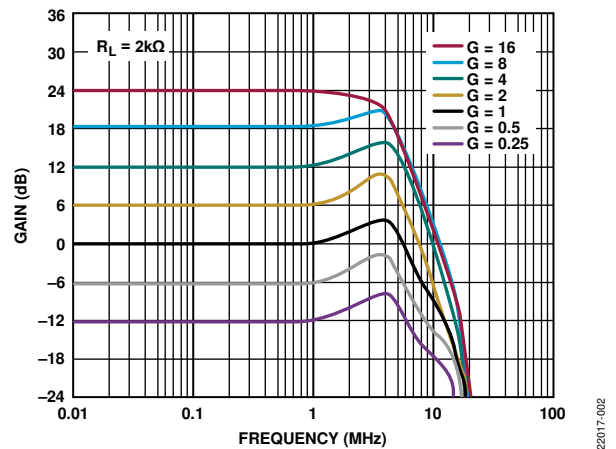

Figure 2. Gain vs. Frequency for the LTC6373, R_L = 2 kΩ

AAF

The AFF is designed to attenuate frequencies at filter images centered around the modulator sample rate (F_S), which is 8 MHz in fast mode, 4 MHz in medium speed mode, and 1 MHz in low speed mode. The AAF is a fourth-order low-pass filter (LPF) with a cutoff frequency set to 330 kHz, maintaining a flat response over the signal bandwidth of 125 kHz. This cutoff frequency results in an attenuation of 105 dB at the 8 MHz sample rate in fast mode. For lower modulator sample rates, the AAF cutoff frequency must be reduced accordingly.
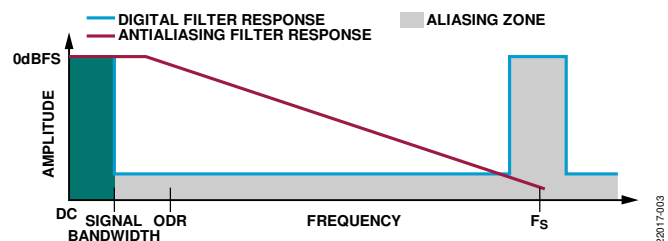

Figure 3. AAF and ADC Digital Filter Frequency Response

Aside from being part of the AAF, the ADA4945-1 serves as the driver for the AD7768-1 ADC. The ADA4945-1 is a fully differential amplifier that has excellent dc and ac performance. The pass band of the AAF has a gain of 1.3×, which is set by the ratio of the 1.3 kΩ feedback resistors and the summation of the 249 Ω, 249 Ω, and 499 Ω resistors.
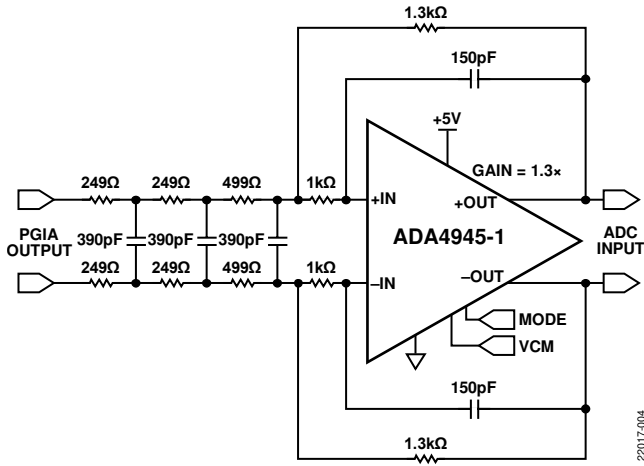

Figure 4. Fourth-Order AAF Circuitry

Noise Contributions

Analysis of a mixed-mode signal chain is complex because noise from the analog signal chain may not necessarily be flat, and the total response of the analog and digital filters must be solved numerically. The Precision ADC Driver Tool was used to assess the simulated noise contribution of the ADC driver, filter, and ADC front end, greatly simplifying the design process.

The ADC, driver, RC filter, and input signal settings on the Precision ADC Driver Tool follow:

- For the ADC, MCLK = 16.38 MHz, MCLK_DIV = divide by 2, power mode = fast, filter type = FIR, decimation = 32, reference voltage (V_{REF}) = 4.096 V, and the precharge mode is enabled.
- For the ADC driver, it is an inverting configuration, gain = 1.3 V/V, R_F = 1.3 kΩ, $+V_S$ = 5 V, and $-V_S$ = 0 V.
- For the RC filter, external resistor (R_{EXT}) = 82 Ω and external capacitor (C_{EXT}) = 100 pF.
- For the input signal, it is a differential input type, frequency = 1 kHz, and the common-mode output voltage (V_{OCM}) = 2.5 V.

The noise contribution of each section is derived from the specifications on the data sheet of the ADC and the ADC driver. The ADC total noise is derived from the signal-to-noise ratio (SNR) specification, and the total noise of the ADC driver is derived from the voltage and current noise density specifications multiplied by the equivalent noise bandwidth of the ADC filter.

The total rms noise is the square root of the sum of the squares (RSS) for each noise contributor. Use the following equation to calculate the total rms noise:

$$Total\ RMS\ Noise = \sqrt{(Driver^2 + RC\ Filter^2 + ADC^2)}$$

The Precision ADC Driver Tool calculates the system SNR (SNS_{SYS}) as follows:

$$SNR_{SYS} = 20\log\frac{FS_{INPUT_{RMS}}}{Total\ RMS\ Noise}$$

where $FS_{INPUT_{RMS}}$ is 4.096 V/√2.

Table 4 details the calculated noise contribution of the ADC and the ADC driver as well as the overall system SNR.

Table 4. Precision ADC Driver Tool Noise Results

Section	Noise (V rms)	Noise (%)	SNR (dB)
ADC Driver	7.15 µ	27	112.2
Voltage Noise of the Amplifier (V_N)	2.45 µ		
Positive Bias Current (I_{B+})	866 n		
Negative Bias Current (I_{B-})	866 n		
Feedback Resistor (R_F)	4.35 µ		
Gain Resistor (R_G)	4.96 µ		
RC Filter	1.09 µ	1	
ADC	11.7 µ	72	107.9
Total	13.7 µ	Not applicable	106.5

The ADA4945-1 also has a high bandwidth and slew rate that helps to suppress the charge kickback from the ADC during sampling and that allows the input to fully settle before the next conversion cycle. Figure 5 shows that the input has fully settled for a sampling period of 61 ns.
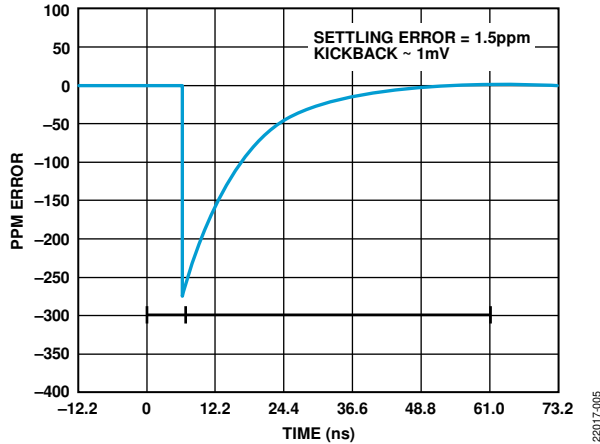

Figure 5. Input Settling Time

Table 5 shows the overall system gain and the corresponding input voltage range of the solution.

Table 5. System Gain and Input Voltage Range

PGIA Gain	AAF + ADC Driver Gain	Overall System Gain	Input Voltage Range (V)
0.25	1.3	0.325	±12.603
0.5	1.3	0.65	±6.302
1	1.3	1.3	±3.151
2	1.3	2.6	±1.575
4	1.3	5.2	±0.788
8	1.3	10.4	±0.394
16	1.3	20.8	±0.197

AC Performance Results

Figure 6 and Figure 7 show the CN-0535 SNR measurements of a 1 kHz input signal, which is comparable to the total SNR Precision ADC Driver Tool results in Table 4. Note that the measured results slightly vary from the Precision ADC Driver Tool because the results of the CN-0535 board encompass the overall performance of the system, which include the PGIA, voltage reference, and power components.
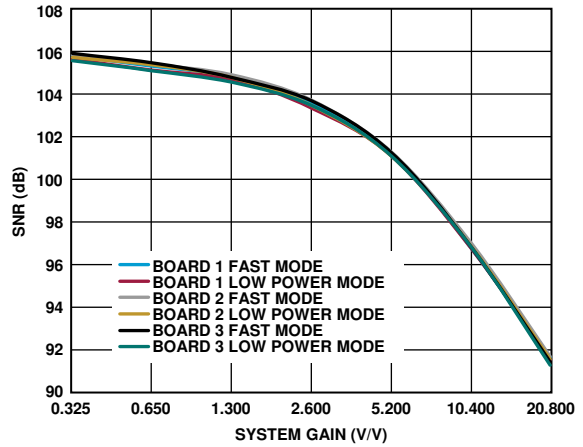
Figure 6. SNR vs. System Gain, Input = 0.5 dBFS
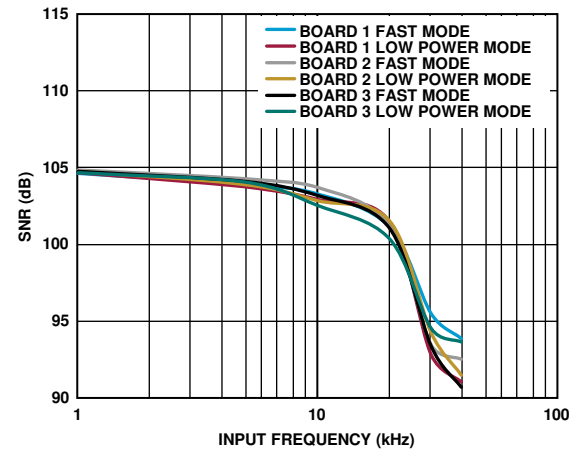
Figure 7. SNR vs. Input Frequency, Input = 0.5 dBFS

Figure 8 and Figure 9 show the CN0535 signal-to-noise-and-distortion ratio (SINAD) measurements.
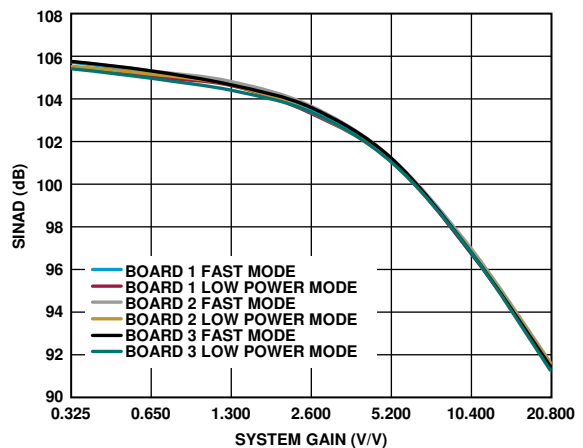

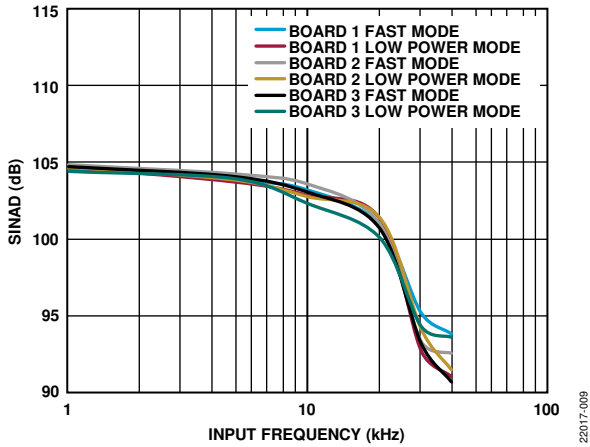*Figure 8. SINAD vs. System Gain, Input = 0.5 dBFS*

Figure 9. SINAD vs. Input Frequency, Input = 0.5 dBFS

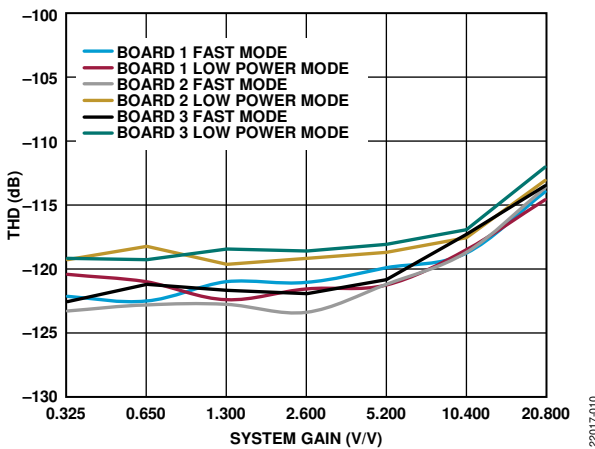Figure 10 and Figure 11 show the CN0535 total harmonic distortion (THD) results.

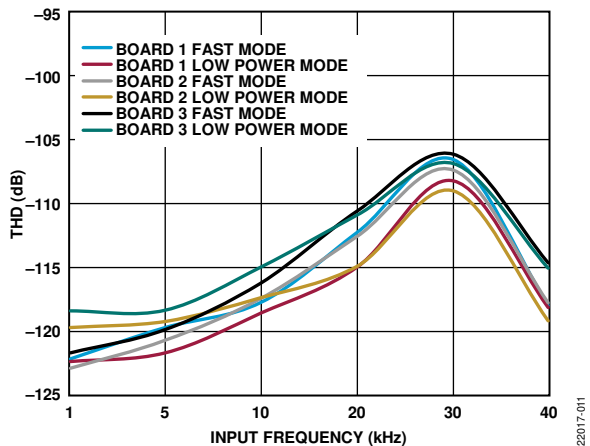Figure 10. THD vs. System Gain, Input = 0.5 dBFS

Figure 11. THD vs. Input Frequency, Input = 0.5 dBFS

DC Performance Results

For DAQ systems, linearity is an important factor in accurately converting the input signal to an ADC output equivalent code. Linear errors, such as offset error and gain error, can be easily calibrated in a measurement system by using the calibration registers in the ADC or the look-up tables in a microcontroller. Figure 12 and Figure 13 show how the offset voltage and a dc input voltage moves across the ambient temperature. These measured values can be used to calibrate the offset and gain errors of the system as previously mentioned in the calibration section of the ADC.
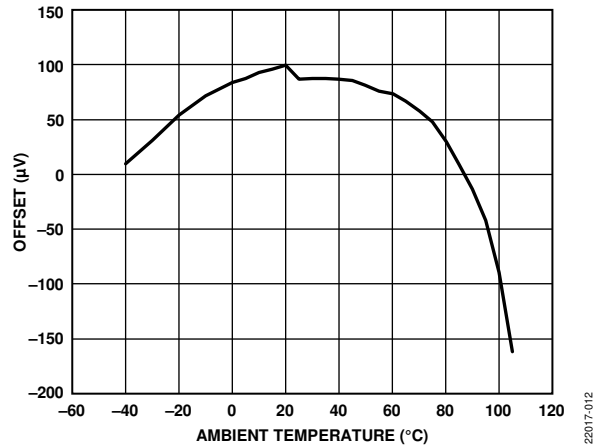
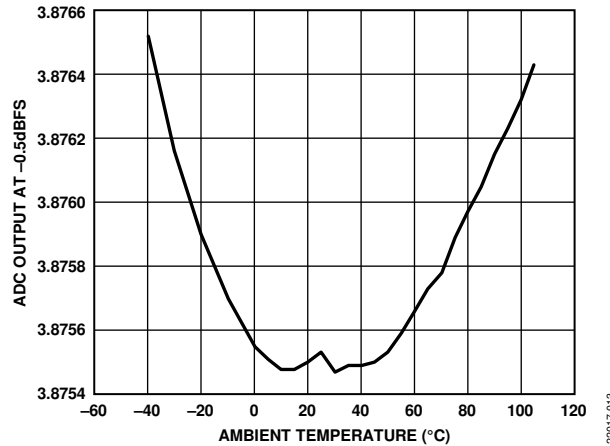Figure 12. Offset vs. Ambient Temperature, G = 1.3

Figure 13. ADC Output at −0.5 dBFS vs. Ambient Temperature, G = 1.3

By using the box method, the offset drift and gain drift of the system are 1.8 μV/°C and 7 μV/°C, respectively. The formula for the offset drift and gain drift follow:

$$Offset\ Drift = (V_{OSMAX} - V_{OSMIN})/(T_{MAX} - T_{MIN})$$

$$Gain\ Drift = (V_{OSMAX} - V_{OSMIN})/(T_{MAX} - T_{MIN})$$

The same cannot be said for nonlinear errors, such as integral nonlinearity (INL), because it is challenging to predict these errors. It is best to design a system that has a minimum nonlinearity error to reduce the calibration required for the system.

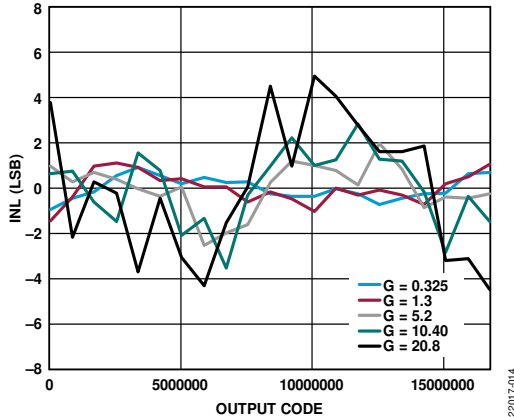Figure 14 shows the typical INL error of the signal chain that is within ±5 LSB.

Figure 14. INL vs. Output Code Across System Gain

Voltage Reference and Buffer

The ADR444 and AD8628 compose the reference voltage for the ADC. The ADR444 is an ultralow noise, 4.096 V voltage reference, and the AD8628 is a zero drift amplifier, which can both operate using the same single supply as the analog part of the ADC. This configuration simplifies the design of the power tree because there are less power rails to generate while still having enough headroom for both the reference chip and the reference buffer.

The reference input current of the ADC scales linearly with the modulator clock rate. The reference input draws 80 µA/V unbuffered and 4 µA/V when the precharge buffers are enabled. The reference block must be able to drive on both of these conditions. Therefore, with a 4.096 V reference, the ADC reference draws the following:

- With precharge buffers off, drawn current (I_{DRAWN}) = 4.096 V × 80 µA/V = 328.68 µA

- With precharge buffers on, I_{DRAWN} = 4.096 V × 4 µA/V = 16.384 µA

With these approximate values, the AD8628 can easily drive the reference input pin because it has a 10 mA capability.

Power Architecture

As shown in Figure 15, the entire power architecture of the CN-0535 is designed in such a way that the whole signal chain can be powered from a single 3.3 V supply.
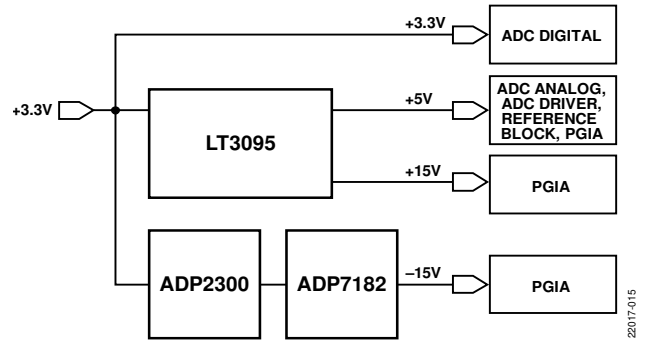

Figure 15. Simplified Block Diagram of the Power Solution

The 3.3 V is supplied from the host board through the FMC connector. Ensure that the field-programmable gate array (FPGA) mezzanine card (FMC) host platform can supply the necessary 250 mA required by the inrush current on the capacitors during startup of the CN0535. If not, an external power supply can be used to power the CN0535.

From the 3.3 V supply, the LT3095 generates the positive 15 V and the 5 V rails for the system. The LT3095 is a compact power solution that features independent, dual, dc to dc boost regulators with two linear regulators at each output in a single chip.

The combination of the ADP2300 and the ADP7182 regulators generates the negative supply rail. The ADP2300 is configured as a buck-boost regulator to generate a −16 V output that is then connected to the ADP7182 linear regulator to generate the −15 V.

The 3.3 V for the digital supply of the ADC is connected directly from the 3.3 V supply because this rail is not critical when it comes to noise.

The analog supply pins of the signal chain require careful attention with regards to noise because the supply noise can greatly affect the performance of the system. The power supply rejection of the low dropout (LDO) regulators help suppress the switching noise coming from the boost and buck-boost regulators before it goes into the system.

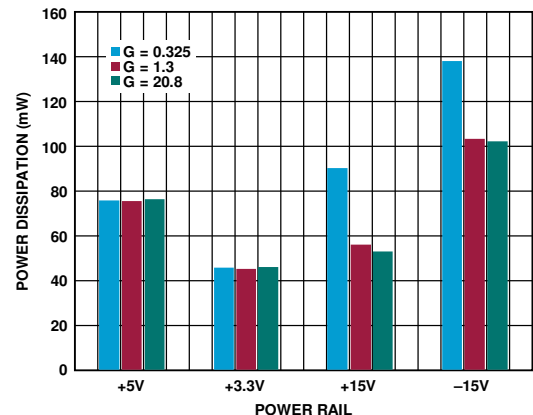Figure 16 shows the power consumption required from each supply rail in the signal chain.

Figure 16. Power Consumption on Each Power Rail

COMMON VARIATIONS

For higher channel count systems, the multichannel AD7768 and AD7768-4 are suitable alternatives to the AD7768-1. The ADC noise and linearity are like that of the AD7768-1, but these devices have the advantage of providing up to eight simultaneous channels in a single chip, which may simplify the implementation of a multichannel DAQ design.

Other ADCs that can be considered for DAQ signal chains include the AD4000, AD4002, and AD7380.

The ADAQ7768-1 is 24-bit, single channel, precision μModule® DAQ system that integrate the ADC, the ADC driver stage, and the PGIA stages, as well as the most critical passive components into a system in package (SiP) design. This option is recommended where size or simplicity of implementation is more critical.

CIRCUIT EVALUATION AND TEST

The following section outlines testing procedures and the gathering of the results for the CN-0535 circuit design. For complete details on the hardware and software setup, see the CN-0535 User Guide.

Equipment Needed

The following equipment is needed:

- A EVAL-CN0535-FMCZ reference design board
- A EVAL-SDP-CH1Z (SDP-H1) system demonstration platform board
- An Audio Precision AP2700 or equivalent.
- A coaxial cable with Bayonet Neill–Concelman (BNC) and Subminiature Version B (SMB) terminations

Getting Started

Figure 17 shows the hardware setup.

To use the reference design board, take the following steps:

1. Ensure that the EVAL-SDP-CH1Z is disconnected from the PC. Install the AD7768-1 evaluation board software, and restart the PC after the software installation is complete.
2. Connect the EVAL-SDP-CH1Z to the EVAL-CN0535-FMCZ reference design board. The J4 connector of the EVAL-SDP-CH1Z connects to the receiving socket, P1, on the EVAL-CN0535-FMCZ.
3. Ensure that the EVAL-SDP-CH1Z and the EVAL-CN0535-FMCZ are connected firmly together by screwing these boards together.
4. Connect a 12 V dc supply to the EVAL-SDP-CH1Z and then connect the EVAL-SDP-CH1Z to the PC using the supplied USB cable. Choose to automatically search for the drivers for the EVAL-SDP-CH1Z if prompted by the operating system.
5. Launch the AD7768-1 evaluation board software from the **Analog Devices** subfolder in the **Programs** menu.
6. Power-on the sine or arbitrary waveform generator as follows:
    a. Connect the differential ac source to the EVAL-CN0535-FMCZ inputs (J3 and J4).
    b. Set the signal type to sine wave and set the level to 5.9 V p-p at 1 kHz.
    c. Enable the output.
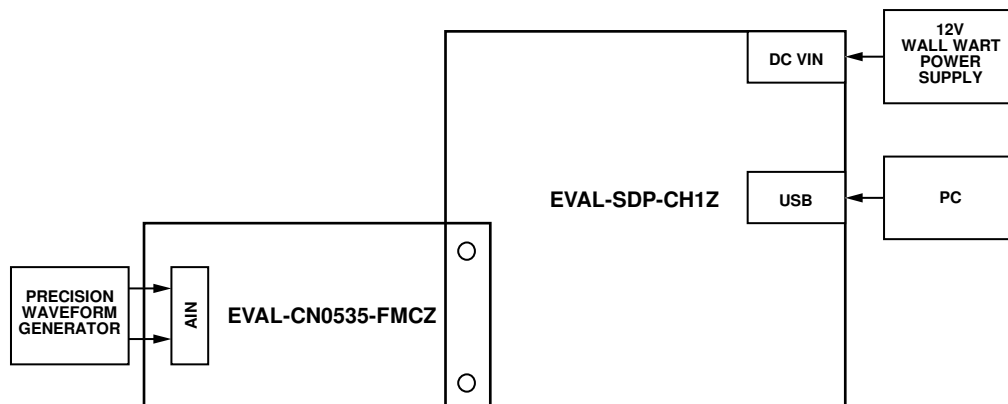7. Run the software and capture the resulting ADC data and FFT data.

Figure 17. Hardware Setup

The plots in Figure 18 and Figure 19 show the typical captures that are expected from the EVAL-CN0535-FMCZ when configured using the previous step. Figure 18 shows the time domain view of the ADC capture data, illustrating the expected ADC output codes over a number of samples.
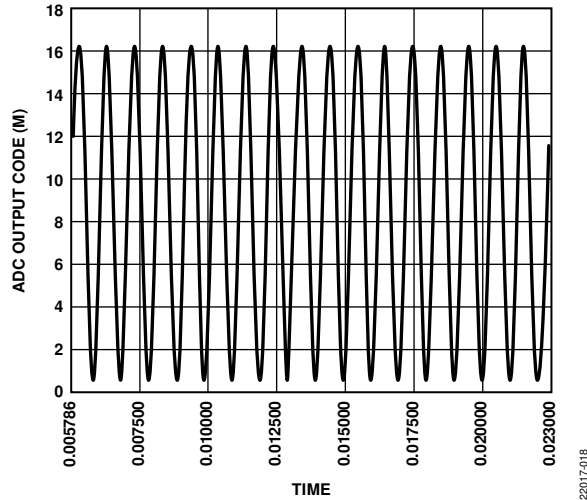

Figure 18. ADC Output Code vs. Time, Input = 1 kHz

Figure 19 shows the same data processed and displayed as a frequency domain FFT plot. The AD7768-1 software user interface is set to have 32,768 samples and uses 7-term Blackman-Harris for its windowing.
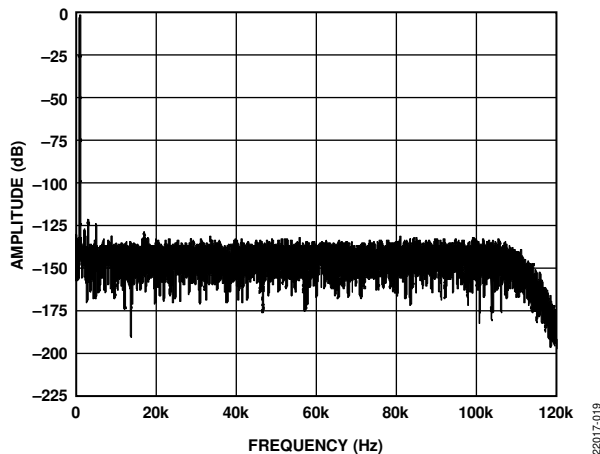
Figure 19. FFT of 1 kHz Input Signal

LEARN MORE

CN0535 Design Support Package:
https://www.analog.com/CN0535-DesignSupport

CN0535 User Guide

Precision ADC Driver Tool

Data Sheets and Evaluation Boards

CN-0535 Circuit Evaluation Board (EVAL-CN0535-FMCZ)

LT3095 Data Sheet

ADP2300 Data Sheet

ADP7182 Data Sheet

ADR444 Data Sheet

AD8628 Data Sheet

ADA4945-1 Data Sheet

AD7768-1 Data Sheet

REVISION HISTORY

1/2021—Revision 0: Initial Version

**ANALOG
DEVICES**