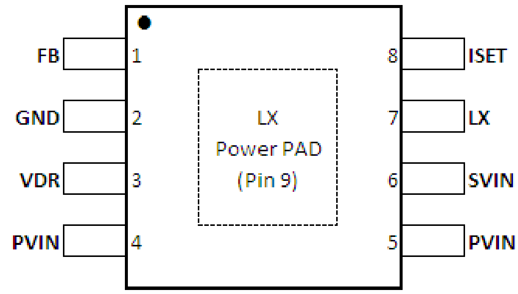
SP7656 PowerBlox

3A, 29V Non-Synchronous Buck Converter

FEATURES

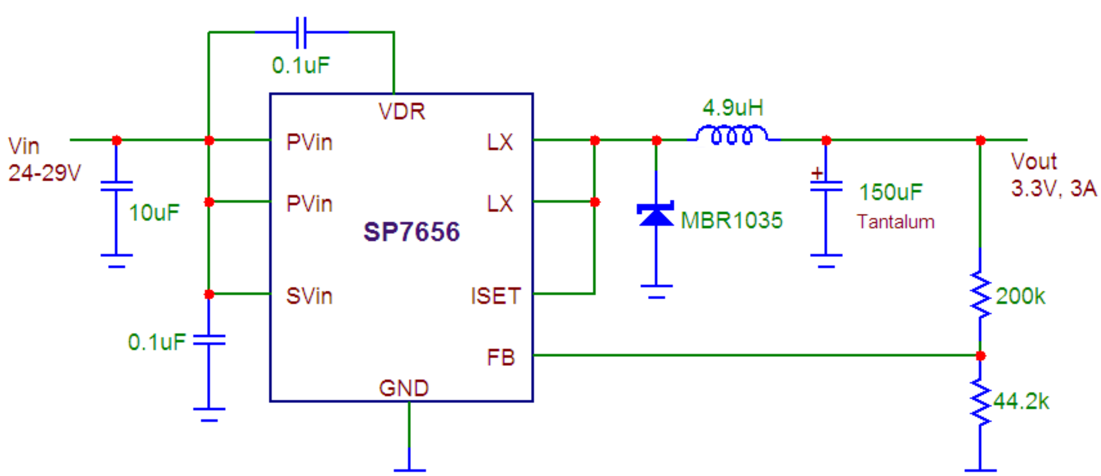
- Wide Input Voltage Range 4.5V – 29V
- 3 Amps Continuous 4 Amps Peak Output Current
- Internal Compensation
- Input Feedforward Control improves Transient and Regulation
- 600kHz Constant Frequency Operation
- Low 0.6V Reference Voltage
- High output setpoint accuracy of 1%
- Internal Soft Start
- Small SO8-EP Thermally Enhanced Package
- Adjustable Overcurrent Protection
- Lead Free, RoHS Compliant Package



DESCRIPTION

The SP7656 is a PWM controlled step down (buck) voltage mode regulator co-packaged with a P-Channel FET. It operates from 4.5V to 29V making it suitable for 5V, 12V and 24V applications. The programmable overcurrent protection is based on internal FET resistance sensing and allows setting the overcurrent protection value up to a 300mV threshold (measured between VIN-LX). The SP7656 is packaged in a thermally enhanced 8-pin SO8 package making it one of the smallest converters available capable of operating from 5, 9, 12, 18 and 24VDC supplies.

TYPICAL APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

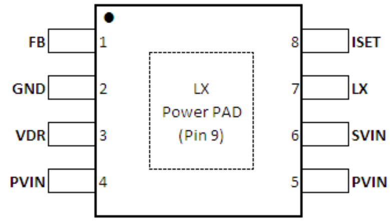
PVIN…... -0.3V to 30V
SVIN…………………………………………..….. -0.3V to 30V
Lx……………………………….…………………..-2V to 30V
ISET……………………………….………………-2V to 30V

FB……………...-0.3V to 5.5V
Storage Temperature..…………………..….-65 °C to 150 °C
Junction Temperature.................................-40°C to 125°C
Lead Temperature (Soldering, 10 sec).....……………..300 °C

ELECTRICAL SPECIFICATIONS

Specifications are for T_{AMB}=T_J=25°C, and those denoted by ♦ apply over the full operating range, -40°C< T_j <85°C.
Unless otherwise specified: V_{IN} =4.5V to 29V, C_{IN} = 4.7µF.

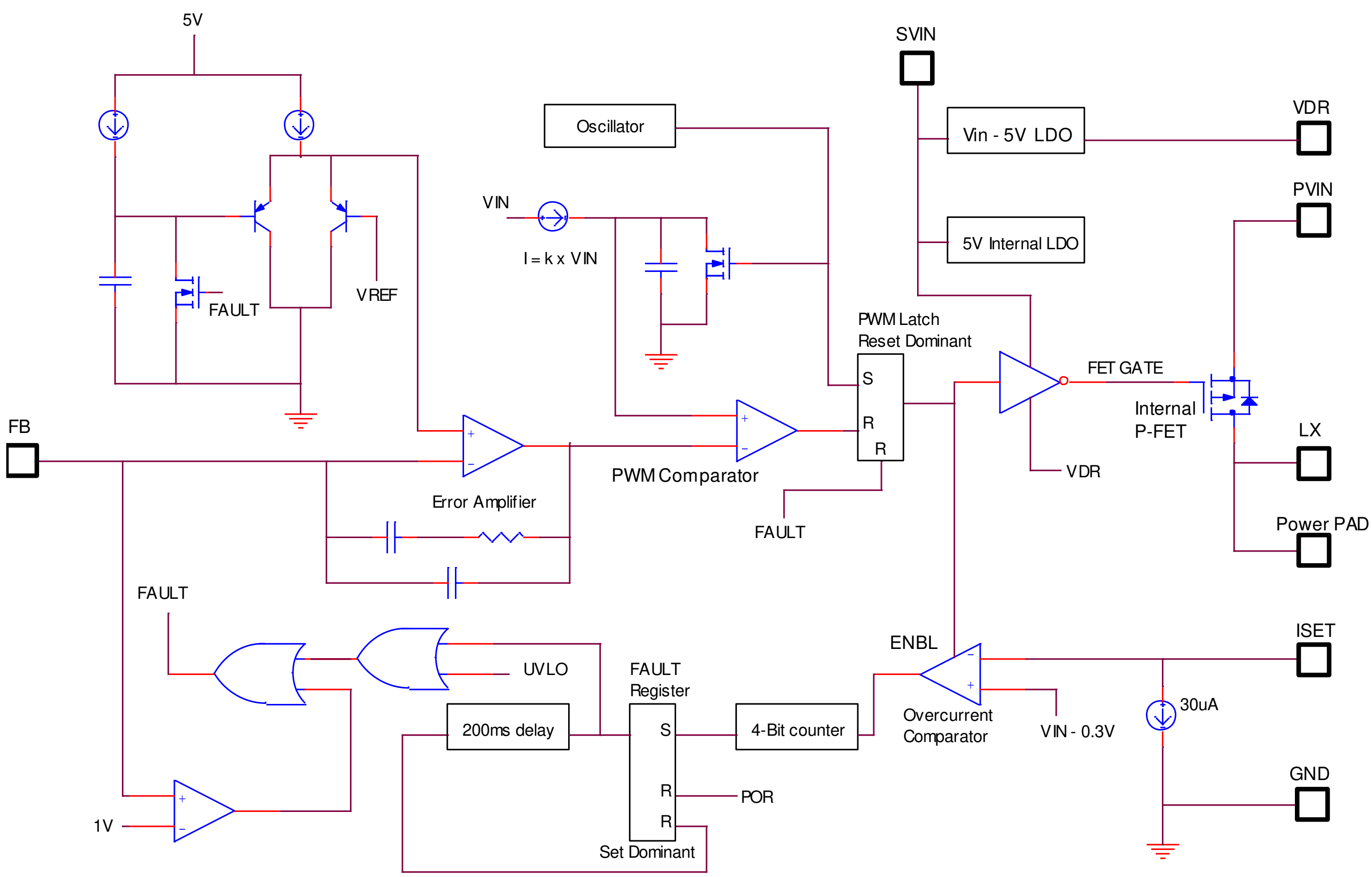
PARAMETER	MIN	TYP	MAX	UNITS	♦	CONDITIONS
UVLO Turn-On Threshold	4.2	4.35	4.5	V		0°C< T_j <85°C
UVLO Turn-Off Threshold	4.0	4.15	4.3	V		0°C< T_j <85°C
UVLO Hysteresis		0.2		V		
Operating Input Voltage Range	4.5		29	V		0°C< T_j <85°C
Operating Input Voltage Range	7		29	V	♦	
Operating VCC Current		0.3	3	mA		VFB=1.2V
Reference Voltage Accuracy		0.5		%		
Reference Voltage Accuracy		0.5	2	%	♦	
Reference Voltage		0.6		V		
Reference Voltage	0.588	0.6	0.612	V	♦	
Switching Frequency	510	600	690	kHz		
Minimum ON-Pulse Duration		40	100	ns	♦	
Minimum Duty Cycle			0	%		
Maximum Duty Cycle	100			%		*See Duty Cycle restriction- applications section
SVIN - VDR voltage difference	4.5		5.5	V	♦	Measure SVIN – VDR, SVIN>7V
Overcurrent Threshold	270	300	330	mV		Measure SVIN - ISET
ISET pin Input Current	25	30	35	µA		V_{ISET} = SVIN
OFF interval during hiccup		100		ms		
Soft start time	3	5	9	ms		VFB=0.58V, measure between VIN=4.5V and first GATE pulse
SHDN Threshold	0.8	1.0	1.2	V	♦	Apply voltage to FB
SHDN Threshold Hysteresis		100		mV		
P-Channel FET ON Resistance		60		mΩ		
P-Channel FET Source leakage		3	5	µA		



PIN DESCRIPTION

PIN #	PIN NAME	DESCRIPTION
1	FB	Regulator feedback input. Connect to a resistive voltage-divider network to set the output voltage. This pin can be also used for ON/OFF control. If this pin is pulled above 1V the controller resets internal soft start circuit.
2	GND	Ground pin.
3	VDR	Power supply for the internal driver. This voltage is internally regulated to about 5V below VIN. Place a 0.1uF decoupling capacitor between VDR and Vin as close as possible to the IC.
4,5	PVIN	Internal P-Channel FET Source. Connect to input voltage.
6	SVIN	Input power supply for the controller. Place input decoupling capacitor as close as possible to this pin. Connect to input voltage.
7,9	LX	Internal P-Channel FET Drain. Connect to the output inductor.
8	ISET	This pin is used as a current limit input for the internal current limit comparator. Connect to LX through an optional resistor. Internal threshold is pre-set to 300mV nominal and can be decreased by changing the external resistor based on the following formula: V_{TRSHLD} = 300mV – 30uA * R. Where R≤3kΩ

CONVERTER BLOCK DIAGRAM



SP7656 General Overview:

The SP7656 PowerBlox is a fixed frequency, voltage mode, non-synchronous PWM controller co-packaged with a P-Channel FET. SP7656 is optimized for minimum component, small form factor and cost effectiveness. It has been designed for single-supply operation ranging from 4.5V to 29V. SP7656 has Type-2 internal compensation for use with Electrolytic/Tantalum output capacitors. For ceramic capacitors Type-3 compensation can be implemented by simply adding an R and C between output and Feedback.

A precision 0.6V reference, present on the positive terminal of the internal error amplifier, permits programming of the output voltage down to 0.6V via the FB pin. The output of the Error Amplifier is internally compared to a feed-forward ($V_{IN}/5$ peak-to-peak) ramp and generates the PWM control.

Timing is governed by an internal oscillator that sets the PWM frequency at 600kHz.

SP7656 contains useful protection features. Over-current protection is based on the internal MOSFET Rds(on) and is programmable via a resistor placed between I_{SET} and LX node. Under-Voltage Lock-Out (UVLO) ensures that the controller starts functioning only when sufficient voltage exists for powering IC's internal circuitry.

SP7656 Loop Compensation

The SP7656 includes Type-2 internal compensation components for loop compensation. External compensation components are not required for systems with tantalum or aluminum electrolytic output capacitors with sufficiently high ESR. Use the condition below as a guideline to determine whether or not the internal compensation is sufficient for your design. Type-2 internal compensation is sufficient if the following condition is met:

$$f_{ESRZERO} < f_{DBPOLE}$$

where:

$$f_{ESRZERO} = \frac{1}{2\pi \; R_{ESR} C_{OUT}}$$

$$f_{DBPOLE} = \frac{1}{2\pi \sqrt{L \, C_{OUT}}}$$

Creating a Type-3 compensation Network

The above condition requires the ESR zero to be at a lower frequency than the double-pole from the LC filter. If this condition is not met, Type-3 compensation should be used and can be accomplished by placing a series RC combination in parallel with R1 as shown below. The value of CZ can be calculated as follows and RZ selected from table 1.

$$CZ = \frac{\sqrt{L \, C}}{R1}$$

$f_{ESRZERO}/f_{DBPOLE}$	RZ
1X	50K
2X	40K
3X	30K
5X	10K
>= 10X	2K

Table1- RZ Selection

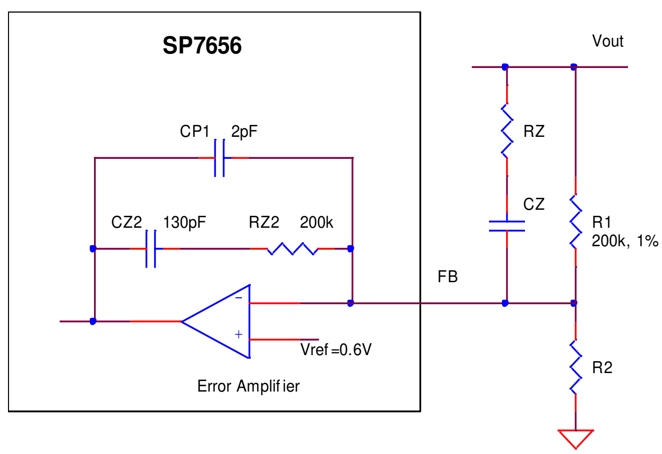


Figure 1- RZ and CZ in conjunction with internal compensation components form a Type-3 compensation

Overcurrent Protection

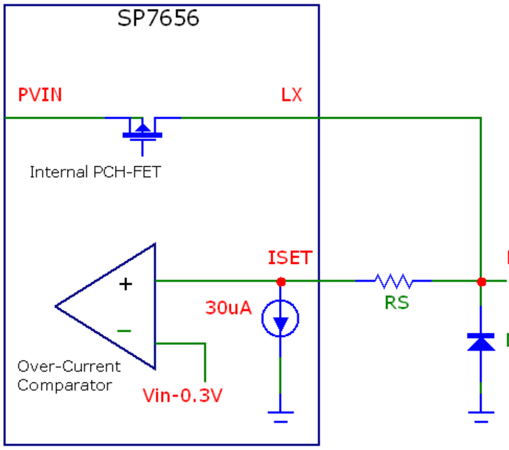


Figure 2 – Overcurrent Protection Circuit

The overcurrent protection circuit functions by monitoring the voltage across the internal P-Channel FET. When this voltage exceeds 0.3V (nominal), the overcurrent comparator triggers and the controller enters hiccup mode. Since the FET has nominal Rds(on) of 0.06Ω, assuming no temperature rise, the overcurrent will trigger at Iocp = 0.3V/0.06Ω=5A. To program a lower overcurrent use a resistor Rs between ISET and LX pins. Calculate Rs from:

$$Rs = \frac{0.3 - (1.15 \times Iocp \times 0.06\Omega \times Kt)}{30uA}$$

Where:
- 1.15 is a multiplier to calculate peak current
- Iocp is the desired overcurrent protection,
- 0.06Ω is nominal FET Rsd(on) at 25°C
- Kt is a multiplier that calculates increase in Rds(on) for a given temperature

Kt is 1.0 and 1.4 for the FET operating at 25°C and 150°C respectively. This accounts for 40% increase in FET Rds(on) as temperature is increased from 25°C to 150°C.

Example: Calculate Rs for Iocp of 3.5A. FET operating temperature is 88°C.

$$Rs = \frac{0.3 - (1.15 \times 3.5A \times 0.06\Omega \times 1.2)}{30uA}$$

Rs=340Ω

Using the above equation there is good agreement between calculated and test results for Rs up to 3k. For Rs larger than 3k test results are lower than those predicted by the Rs equation due to circuit parasitics. Therefore the maximum value of Rs should be limited to 3kΩ.

Using the ON/OFF Function via VFB

The feedback pin serves a dual role of On/Off control. The MOSFET driver is disabled when a voltage greater than 1V is applied at FB pin. Maximum voltage rating of this pin is 5.5V. The controlling signal should be applied through a small signal diode to FB pin. *Please note that an optional 10k bleeding resistor across the output helps keep the output capacitor discharged under no load condition.*

Programming the Output Voltage

To program the output voltage, calculate R2 using the following equation:

$$R2 = \frac{200k}{\left(\frac{Vout}{0.6} - 1\right)}$$

0.6 is used as it is the reference voltage of the SP7656. 200k is a fixed-value and is the top resistor in the output set point resistor pair. In addition to being part of the voltage divider, it is part of the compensation network. R1 of the output voltage divider should always be 200kΩ.

Soft Start

Soft Start is preset internally to 5ms (nominal). Internal Soft Start eliminates the need for the external capacitor CSS that is commonly used to program this function.

Input Capacitance Selection

Select the input capacitor for Voltage, Capacitance, ripple current, ESR and ESL. Voltage rating is nominally selected to be approximately twice the input voltage. The RMS value of input capacitor current, assuming a low inductor ripple current (I_{RIP}), can be calculated from:

$$Icin = Iout\sqrt{D\ (1 - D)}$$

In general total input voltage ripple should be maintained below 1.5% of V_{IN} (not to exceed 180mV).
Input voltage ripple has three components: ESR and ESL cause a step voltage drop upon turn on of the MOSFET. During the on time

the capacitor discharges linearly as it supplies I_{OUT}-I_{in}. The contribution to Input voltage ripple by each term can be calculated from:

$$\Delta V, Cin = \frac{Iout\ \ Vout\ \ (Vin - Vout)}{fs\ \ Cin\ \ Vin^2}$$

$$\Delta V, ESR = ESR\ \ (Iout - 0.5\ \ Irip)$$

$$\Delta V, ESL = ESL\ \ \frac{(Iout - 0.5\ \ Irip)}{Trise}$$

Where Trise is the rise time of current through Capacitor. The total input voltage ripple is sum of the above:

$$\Delta V, Tot = \Delta V, Cin + \Delta V, ESR + \Delta V, ESL$$

Output Capacitor Selection

Select the output capacitor for voltage rating, capacitance and Equivalent Series Resistance (ESR).

Nominally the voltage rating is selected to be twice as large as the output voltage. Select the capacitance to satisfy the specification for output voltage overshoot/undershoot caused by current step load. A steady-state output current I_{OUT} corresponds to inductor stored energy of ½ L I_{OUT}^2.

A sudden decrease in I_{OUT} forces the energy surplus in L to be absorbed by C_{OUT}. This causes an overshoot in output voltage that is corrected by the power switch reducing in duty cycle. Use the following equation to calculate C_{OUT}:

$$Cout = L\left(\frac{I_2^{\ 2} - I_1^{\ 2}}{Vos^2 - Vout^2}\right)$$

Where:
L is the output inductance
I2 is the step load high current
I1 is the step load low current
V_{os} is output voltage including overshoot
V_{OUT} is steady state output voltage

Output voltage undershoot calculation is more complicated. Test results for SP7656 buck circuits show that undershoot is approximately equal to overshoot. Therefore above equation provides a satisfactory method for calculating C_{OUT}. Select ESR such that output voltage ripple (V_{RIP}) specification is met. There are two components to the output ripple voltage: The first component arises from charge transferred to and from C_{OUT} during each cycle. The second component is due to inductor ripple current flowing through the output capacitor's ESR. It can be calculated from:

$$Vrip = Irip\ \ \sqrt{ESR^2 + \left(\frac{1}{8\ \ Cout\ \ fs}\right)^2}$$

Where:
I_{RIP} is inductor ripple current
fs is switching frequency
C_{OUT} is output capacitor calculated above

Note that a smaller inductor results in a higher inductor ripple current, therefore requiring a larger C_{OUT} and/or lower ESR in order to meet the output voltage ripple requirement.

Schottky Rectifier Selection

Select the Schottky based on the voltage rating VR, Forward voltage V_f, and thermal resistance R_{thja}. For a low duty cycle application the Schottky is conducting most of the time and its conduction losses are the largest component of losses in the converter. Conduction losses can be estimated from:

$$Pc = Vf\ \ Iout\ \left(1 - \frac{Vout}{Vin}\right)$$

where:
V_f is diode forward voltage at I_{OUT}

The AC losses from the switching capacitance of a Schottky are negligible and can be ignored.

Inductor Selection

Select the Inductor for inductance L and saturation current I_{SAT}. Make sure to select an inductor with I_{SAT} higher than the programmed overcurrent level.

The inductance can be calculated from:

$$L = (Vin - Vout)\left(\frac{Vout}{Vin}\right)\left(\frac{1}{f}\right)\left(\frac{1}{Irip}\right)$$

where:
V_{IN} is converter input voltage
V_{OUT} is converter output voltage
f is the switching frequency (300kHz)
I_{RIP} is inductor peak-to-peak current ripple (nominally set to 30% of I_{OUT})

Keep in mind that a higher inductor ripple current results in a smaller inductance – and smaller inductor. A smaller inductor has the advantages of small size, low DC equivalent resistance DCR, high saturation current and allows the use of a lower output capacitance to meet a given step load transient. A higher inductor ripple current level also has disadvantages. It increases the output voltage ripple and increases the current at which converter enters Discontinuous Conduction Mode. The output current at which converter enters DCM is ½ of I_{RIP}. Note that a negative current step load that drives the converter into DCM will result in a large output voltage transient. Therefore the lowest current for a step load should be larger than ½ of I_{RIP}.

Restriction on high duty cycle operation

The SP7656 is optimized to provide superior performance for low duty cycle applications. For applications with output voltages below 9V, the device will operate normally at the expected 600kHz switching frequency for conversions with less than 50% duty cycle. For applications with output voltages below 9V and greater than 50% duty cycle, the device will enter into a pulse skipping mode. This is due to the FB voltage to internal ramp voltage ratio of the device, and is an intended behavior from an architecture optimized for superior performance in low duty cycle conversion applications and results in a small increase in output ripple voltage for any given circuit. For output voltages above 9V, the device will operate at a constant 600kHz switching frequency across the specified duty cycle range up to 100%.

Layout Suggestions

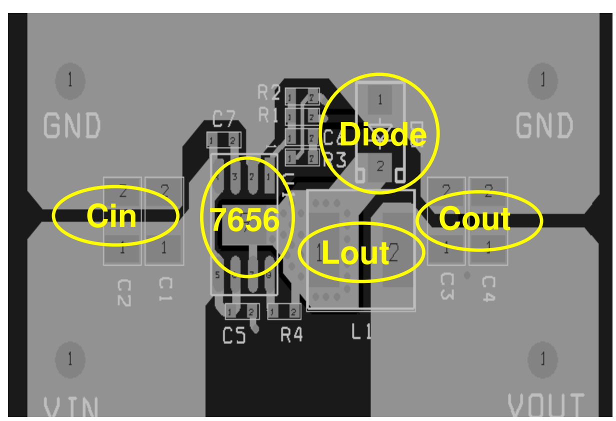
i) Place the input capacitor(s) as close as possible to the 7656 IC.

ii) Create a pad under the IC that connects the power pad (pin 9) to the inductor. Duplicate this pad through the pcb layers if present, and on the bottom side of the PCB. Use multiple vias to connect these layers to aid in heat dissipation. Do not oversize this pad - since the LX node is subjected to very high dv/dt voltages, the stray capacitance formed between these islands and the surrounding circuitry will tend to couple switching noise

iii) Connect the Schottky diode cathode as close as possible to the LX node and inductor input side. Connect the anode to a large diameter trace or a copper area that connects the input ground to the output ground.

iv) The output capacitors should be placed as close to the load as possible. Use short wide copper regions to connect output capacitors to load to avoid inductance and resistances.

v) Keep other sensitive circuits and traces away from the LX node in particular and away from the power supply completely if possible.



For more detail on the SP7656 layout see the SP7656EVB (Evaluation Board) Manual available on our web site. Each layer is shown in detail as well as a complete bill of materials and performance characterization.

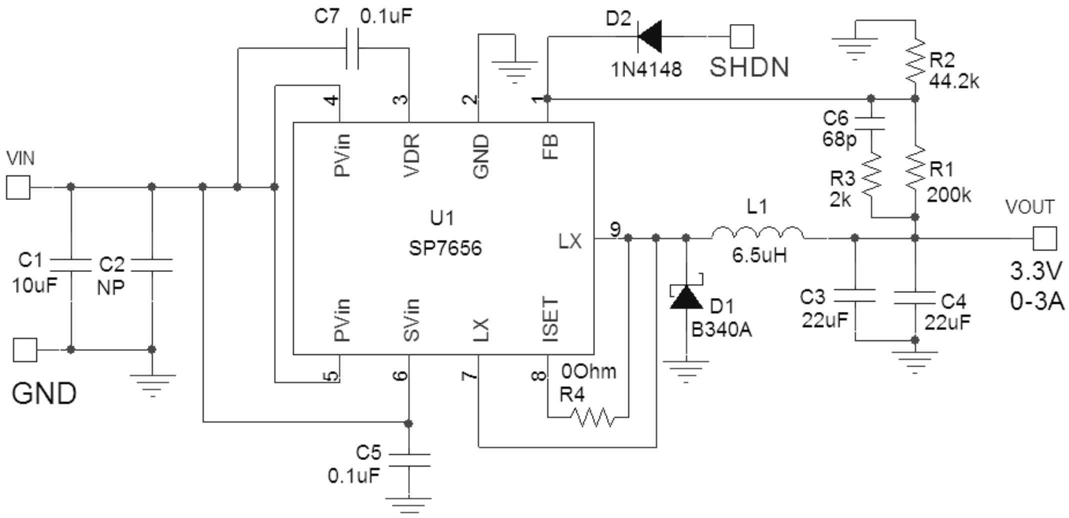


Figure 2- Typical application circuit

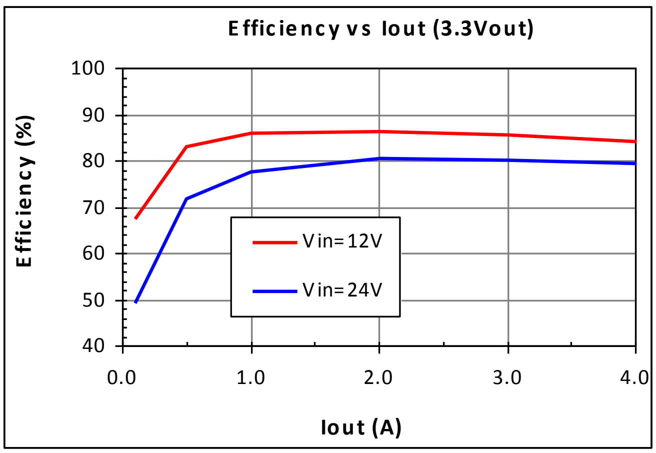


Figure 3- Efficiency, Natural convection at Vout=3.3V, Ta= 25°C

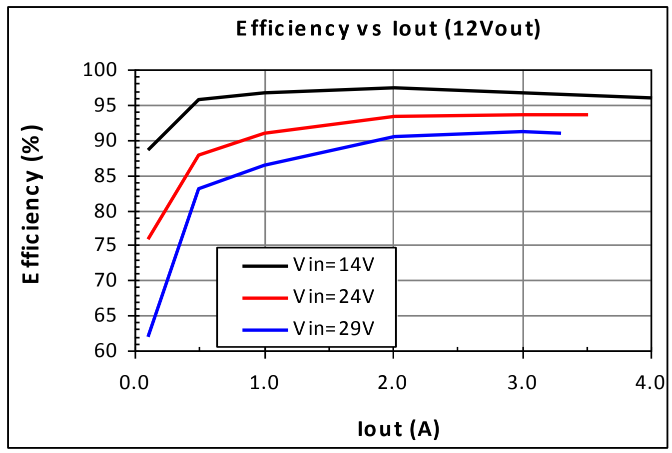


Figure 4- Efficiency Natural convection at Vout=12V, Ta= 25°C,

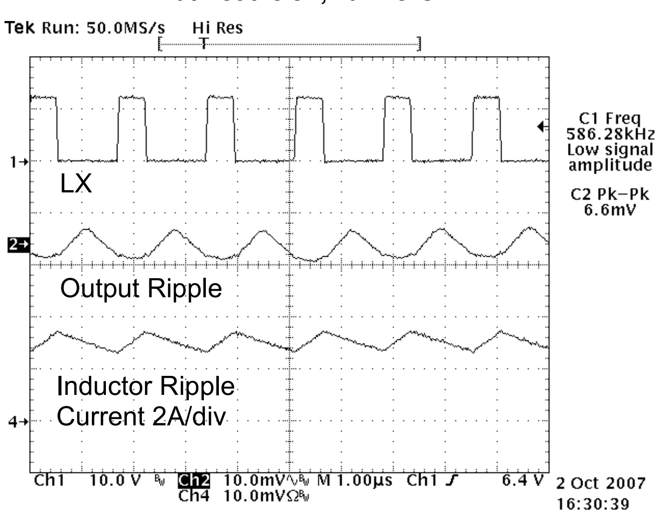


Figure 5- Output Ripple Vout=3.3V, Ta= 25°C

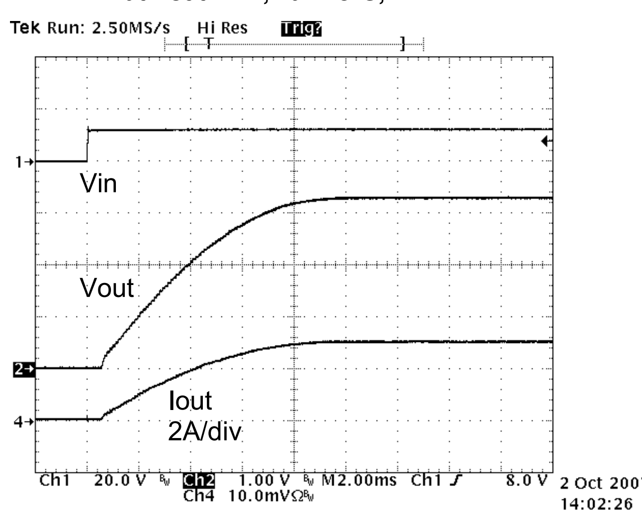
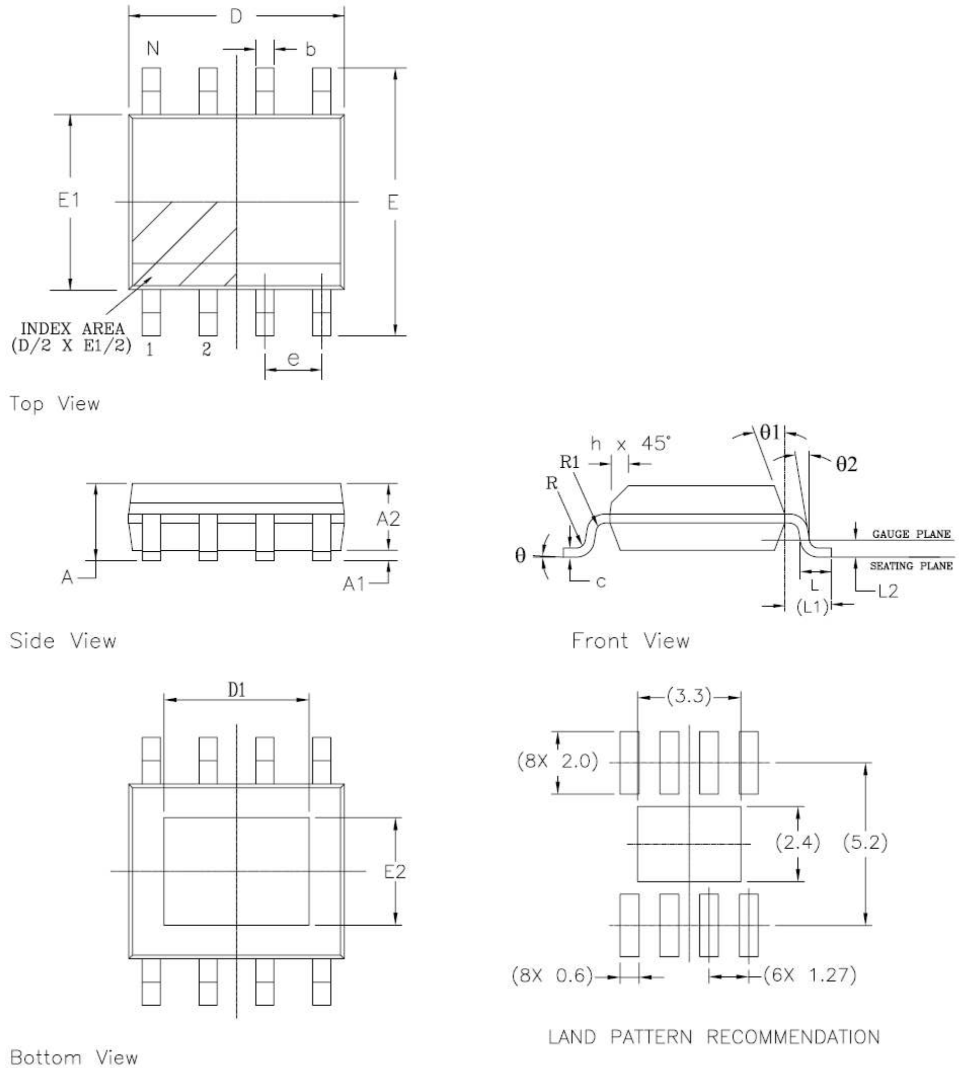


Figure 6- Start-up Vout=3.3V, Ta= 25°C



REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	06/08/07	JL
B	CHANGE DRAWING LOGO AND COMPANY NAME	11/21/07	JL

8 Pin HSOICN JEDEC MS-012 Variation BA						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	—	1.70	0.053	—	0.067
A1	0.00	—	0.15	0.000	—	0.006
A2	1.25	—	1.65	0.049	—	0.065
b	0.31	—	0.51	0.012	—	0.020
c	0.17	—	0.25	0.007	—	0.010
D	4.90 BSC			0.193 BSC		
D1	3.30 REF			0.130 REF		
E	6.00 BSC			0.236 BSC		
E1	3.90 BSC			0.154 BSC		
E2	2.41 REF			0.095 REF		
e	1.27 BSC			0.050 BSC		
h	0.25	—	0.50	0.010	—	0.020
L	0.40	—	1.27	0.016	—	0.050
L1	1.04 REF			0.041 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
θ	0°	—	8°	0°	—	8°
θ1	5°	—	15°	5°	—	15°
θ2	0°	—	—	0°	—	—
N	8			8		

EXAR Powering Connectivity		EXAR CORPORATION	
		8 PIN HSOICN PACKAGE OUTLINE	
Packaging Approval:		Drawing No: 8-PIN HSOICN	
By: JL	Date: 11/21/07	Revision: B	Sheet: 1 OF 1

Ordering Information

Part Number	Temperature Range	Package
SP7656EN2-L	- 40°C to 125°C	(Lead Free) 8-pin HSOICN
SP7656EN2-L/TR	- 40°C to 125°C	(Lead Free) 8-pin HSOICN

/TR = Tape and Reel
Pack Quantity for Tape and Reel is 2500

Revision History

DATE	REVISION	DESCRIPTION
February 2008	A	- Original Release
July 2008	B	- Block Diagram Update to include FET - Formatting changes

For further assistance:

Email: customersupport@exar.com
EXAR Technical Documentation: http://www.exar.com/TechDoc/default.aspx?

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