

Automotive Grade AUIRS44261S DUAL LOW SIDE DRIVER

Features

- Gate drive supply range from 4.8 V to 20 V
- CMOS Schmitt-triggered inputs
- Matched propagation delay for both channels
- Outputs out of phase with inputs
- Automotive Qualified[†]
- Leadfree, RoHS compliant

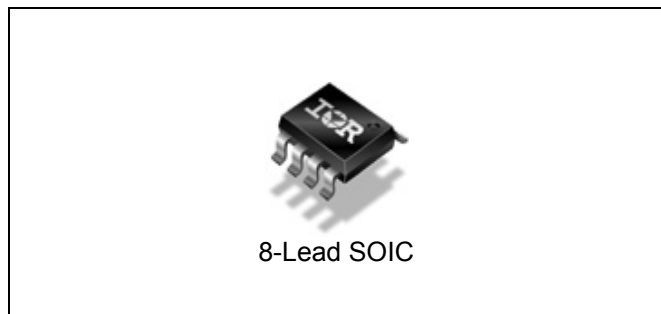
Typical Applications

- Automotive General Purpose Dual Low Side Driver
- Automotive DC-DC converters
- Hybrid Power Train Drives
- Direct Fuel Injection

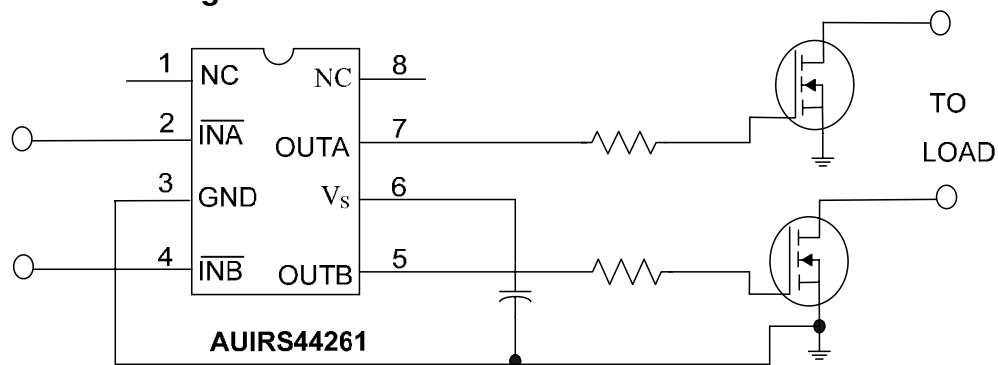
Product Summary

Topology	Dual Low Side Driver
V _{OUT}	4.8 V – 20 V
I _{o+} & I _{o-} (typical)	2.3 A & 3.3 A
t _{ON} & t _{OFF} (typical)	70 ns & 65 ns

Package



Typical Connection Diagram



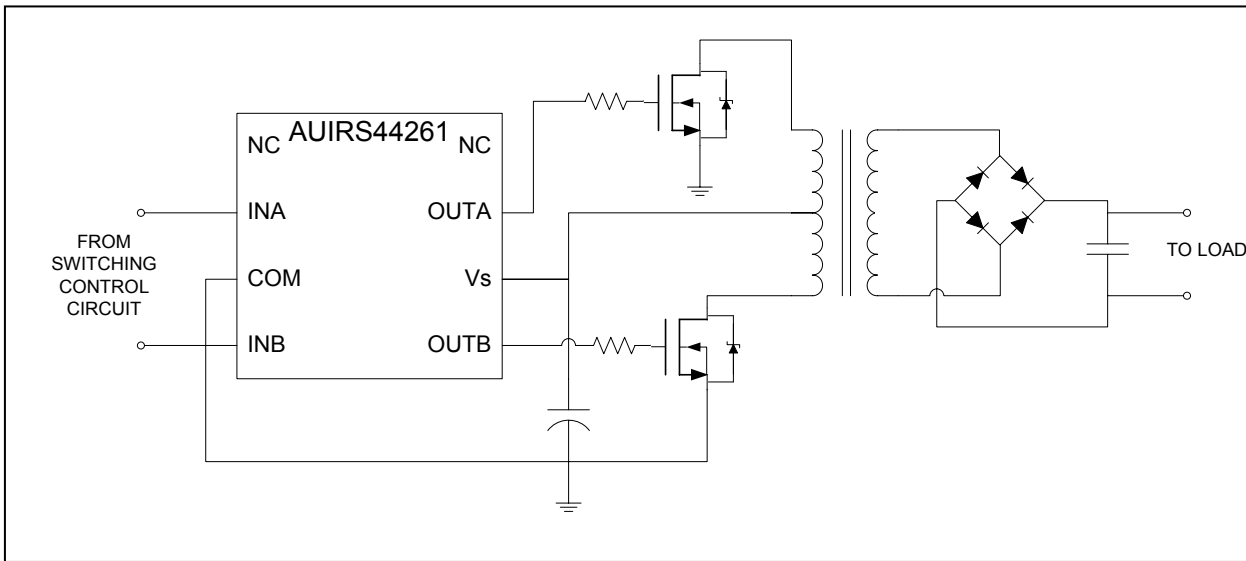
(Please refer to our Application Notes and Design Tips for proper circuit board layout)

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Description

The AUIRS44261 is a low voltage, high speed power MOSFET and IGBT driver. Proprietary latch immune CMOS technologies enable ruggedized monolithic construction. The logic inputs thresholds are proportional to V_s supply voltage.. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays between two channels are matched.

Diagram for push-pull forward DC-DC converter application



Qualification Information[†]

Qualification Level		Automotive (per AEC-Q100 ^{††})	
		Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		SOIC8N	MSL3 ^{†††} 260°C (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class M2 (+/-200V) (per AEC-Q100-003)	
	Human Body Model	Class H2 (+/-4000V) (per AEC-Q100-002)	
	Charged Device Model	Class C4 (+/-1000V) (per AEC-Q100-011)	
IC Latch-Up Test		Class II Level B ^{††††} (per AEC-Q100-004)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

†† Exceptions (if any) to AEC-Q100 requirements are noted in the qualification report.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

†††† INA and INB stressed to +/-40mA

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND lead. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

Symbol	Definition	Min.	Max.	Units
V_S	Fixed supply voltage	-0.3	25	V
V_O	Output voltage	-0.3	$V_S + 0.3$	
V_{IN}	Logic input voltage	-0.3	$V_S + 0.3$	
P_D	Package power dissipation @ $T_A \leq 25^\circ\text{C}$	—	0.625	W
R_{thJA}	Thermal resistance, junction to ambient	—	200	$^\circ\text{C}/\text{W}$
T_J	Junction temperature	—	150	$^\circ\text{C}$
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltage referenced to GND.

Symbol	Definition	Min.	Max.	Units
V_S	Fixed supply voltage	4.8	20	V
V_O	Output voltage	0	V_S	
V_{IN}	Logic input voltage	0	V_S	
T_A	Ambient temperature	-40	125	$^\circ\text{C}$

Static Electrical Characteristics

Unless otherwise noted, these specifications apply for an operating junction temperature range of $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$ with bias conditions of $V_{\text{BIAS}} (V_S) = 15\text{ V}$. The V_{IN} and I_{IN} parameters are referenced to GND and are applicable to input leads: INA and INB. The V_{O} and I_{O} parameters are referenced to GND and are applicable to the output leads: OUTA and OUTB.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{IH}	Logic "0" input voltage	$0.5 * V_S + 0.3\text{V}$	—	—	V	$4.8\text{V} < V_S < 20\text{V}$
V_{IL}	Logic "1" input voltage	—	—	$0.15 * V_S + 0.08\text{V}$		
V_{OH}	High level output voltage, $V_{\text{BIAS}} - V_{\text{O}}$	—	—	1.4		$I_{\text{O}} = 0\text{ mA}$
V_{OL}	Low level output voltage, V_{O}	—	—	0.1		
$I_{\text{IN}+}$	Logic "1" input bias current (OUT = HI)	—	15	25	μA	$V_{\text{IN}} = 0\text{ V}$
$I_{\text{IN}-}$	Logic "0" input bias current (OUT = LO)	—	0	1		$V_{\text{IN}} = V_S$
I_{QB}	Quiescent V_S supply current	—	70	220		$V_{\text{IN}} = 0\text{ V or } V_S$
$I_{\text{O}+}$	Output high short circuit pulsed current ^(†)	1.5	2.3	—	A	$V_{\text{O}} = 0\text{ V}, V_{\text{IN}} = 0$ $\text{PW} \leq 10\ \mu\text{s}$
$I_{\text{O}-}$	Output high short circuit pulsed current ^(†)	1.5	3.3	—		$V_{\text{O}} = 15\text{ V}, V_{\text{IN}} = V_S$ $\text{PW} \leq 10\ \mu\text{s}$

(†) Guaranteed by design

Dynamic Electrical Characteristics

Unless otherwise noted, these specifications apply for an operating junction temperature range of $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$ with bias conditions of $V_{\text{BIAS}} (V_S) = 15\text{ V}$, $\text{CL} = 1000\text{pF}$. The dynamic electrical characteristics are measured using the test circuit shown in Fig. 3.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Propagation delay characteristics						
t_{d1}	Turn-on propagation delay	—	70	150	ns	Figure 2
t_{d2}	Turn-off propagation delay	—	65	150		
t_{r}	Turn-on rise time	—	15	35		
t_{f}	Turn-off fall time	—	25	50		

Static Electrical Characteristics Vs=4.8V

Unless otherwise noted, these specifications apply for an operating junction temperature range of $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$ with bias conditions of $V_{\text{BIAS}} (V_S) = 4.8 \text{ V}$. The V_{IN} and I_{IN} parameters are referenced to GND and are applicable to input leads: INA and INB. The V_{O} and I_{O} parameters are referenced to GND and are applicable to the output leads: OUTA and OUTB.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{IH}	Logic "0" input voltage	2.7	—	—	V	
V_{IL}	Logic "1" input voltage	—	—	0.8	V	
$V_{\text{OH}25}$	High level output voltage, $V_{\text{BIAS}} - V_{\text{O}}$	—	—	1.6	V	$I_{\text{O}} = 2 \text{ mA}$, $T_j = 25^{\circ}\text{C}$
$V_{\text{OH}40}$	High level output voltage, $V_{\text{BIAS}} - V_{\text{O}}$	—	—	2.2	V	$I_{\text{O}} = 2 \text{ mA}$, $T_j = -40^{\circ}\text{C}$
$V_{\text{OH}125}$	High level output voltage, $V_{\text{BIAS}} - V_{\text{O}}$	—	—	1.6	V	$I_{\text{O}} = 2 \text{ mA}$, $T_j = 125^{\circ}\text{C}$
V_{OL}	Low level output voltage, V_{O}	—	—	0.1	V	$I_{\text{O}} = 2 \text{ mA}$
$I_{\text{IN}+}$	Logic "1" input bias current (OUT = HI)	—	5	10	μA	$V_{\text{IN}} = 0 \text{ V}$
$I_{\text{IN}-}$	Logic "0" input bias current (OUT = LO)	—	0	1		$V_{\text{IN}} = V_S$
I_{QB}	Quiescent V_S supply current	—	25	45		$V_{\text{IN}} = 0 \text{ V}$ or V_S
$I_{\text{O}+}$	Output high short circuit pulsed current ^(†)	430	640	—	mA	$V_{\text{O}} = 0 \text{ V}$, $V_{\text{IN}} = 0$ $\text{PW} \leq 10 \mu\text{s}$
$I_{\text{O}-}$	Output high short circuit pulsed current ^(†)	530	850	—		$V_{\text{O}} = 4.8 \text{ V}$, $V_{\text{IN}} = V_S$ $\text{PW} \leq 10 \mu\text{s}$

(†) Guaranteed by design

Dynamic Electrical Characteristics Vs=4.8V

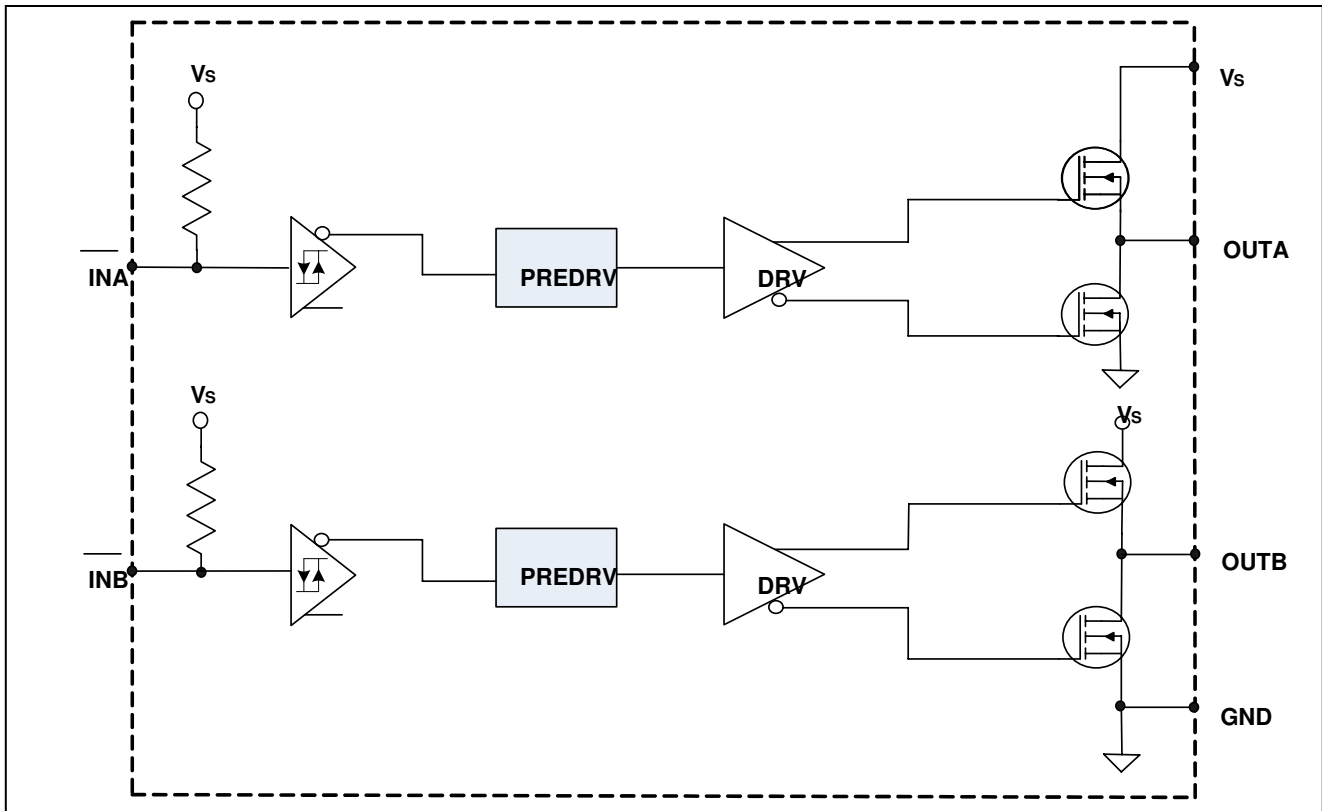
Unless otherwise noted, these specifications apply for an operating junction temperature range of $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$ with bias conditions of $V_{\text{BIAS}} (V_S) = 4.8 \text{ V}$, $\text{CL} = 1000\text{pF}$. The dynamic electrical characteristics are measured using the test circuit shown in Fig. 3.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Propagation delay characteristics						
$t_{\text{d}1}$	Turn-on propagation delay (note 1)	—	130	220	ns	Figure 2
$t_{\text{d}2}$	Turn-off propagation delay (note 2)	—	150	250		
t_{r}	Turn-on rise time (note 3)	—	40	75		
t_{f}	Turn-off fall time (note 4)	—	50	75		

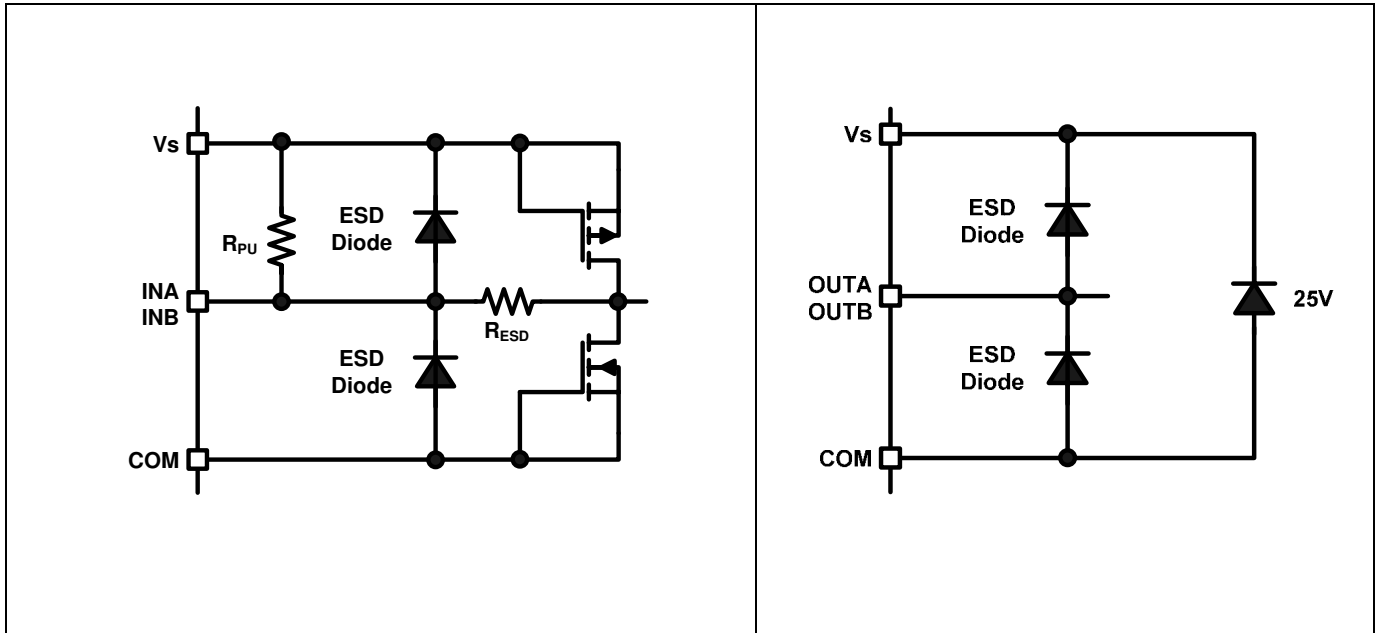
(note 1) from 50% input to 25% output
 (note2) from 50% input to 75% output
 (note3) from 10% to 65%

(note4) from 65% to 10%

Functional Block Diagram: AUIRS44261



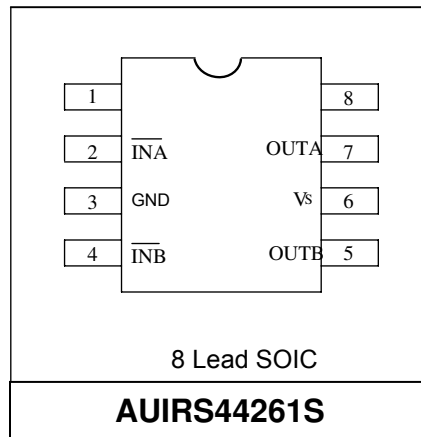
Input/Output Pin Equivalent Circuit Diagrams:



Lead Definitions

Symbol	Description
V_s	Supply voltage
GND	Ground
$\overline{\text{INA}}$	Logic input for gate driver output (OUTA), out of phase
$\overline{\text{INB}}$	Logic input for gate driver output (OUTB), out of phase
OUTA	Gate drive output A
OUTB	Gate drive output B

Lead Assignments



Application Information and Additional Details

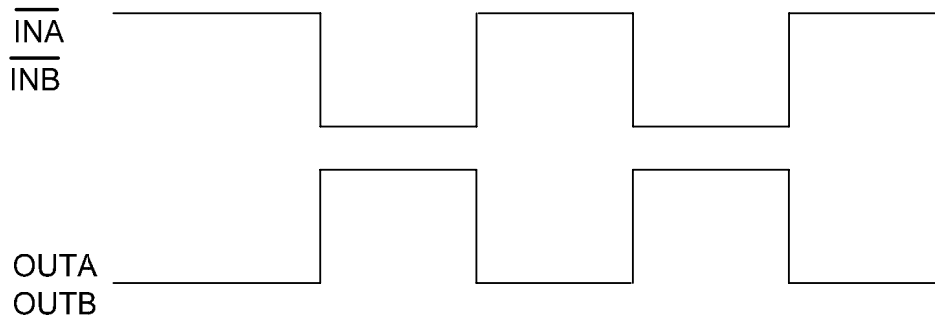


Figure 1: Input/output Timing Diagram

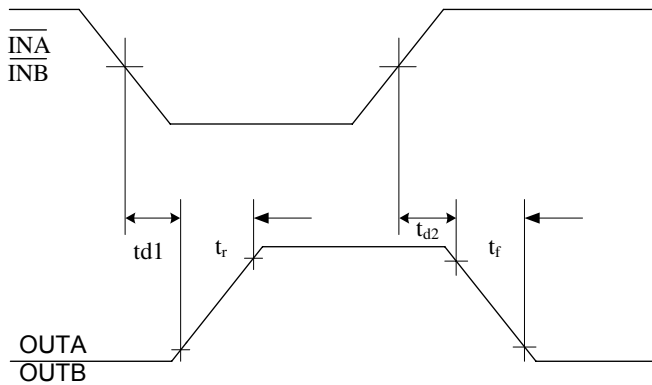


Figure 2: Switching Time Waveform Definitions

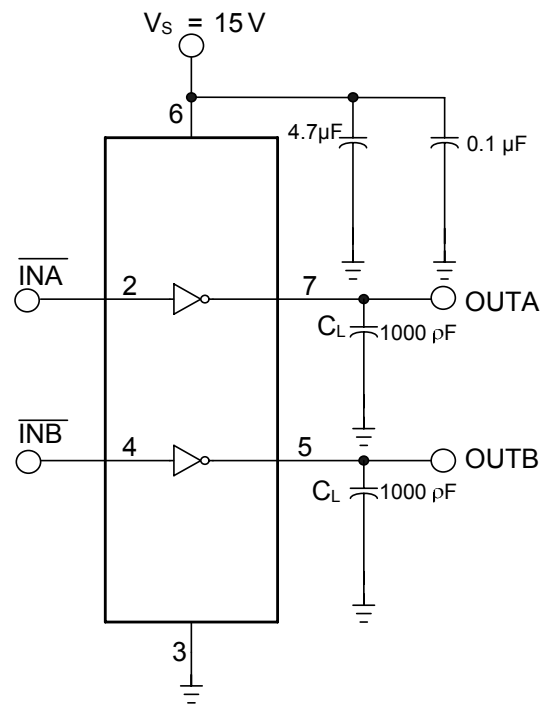


Figure 3: Advance Configuration

Parameter Trends vs. Temperature

Figures illustrated in this chapter provide information on the experimental performance of the AUIRS44261S HVIC. The line plotted in each figure is generated from actual lab data. A large number of individual samples were tested at three temperatures (-40 °C, 25 °C, and 125 °C) with supply voltage of 15V in order to generate the experimental curve. The line consists of three data points (one data point at each of the tested temperatures) that have been connected together to illustrate the understood trend. The individual data points on the Typ. curve were determined by calculating the averaged experimental value of the parameter (for a given temperature).

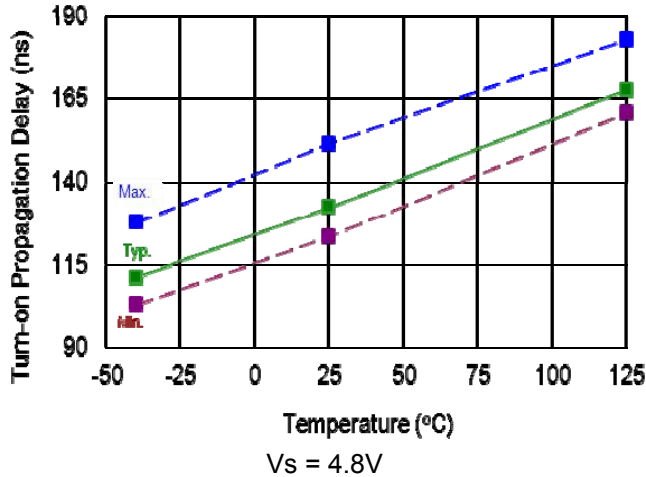


Figure 4. Turn-On Propagation Delay vs. Temperature

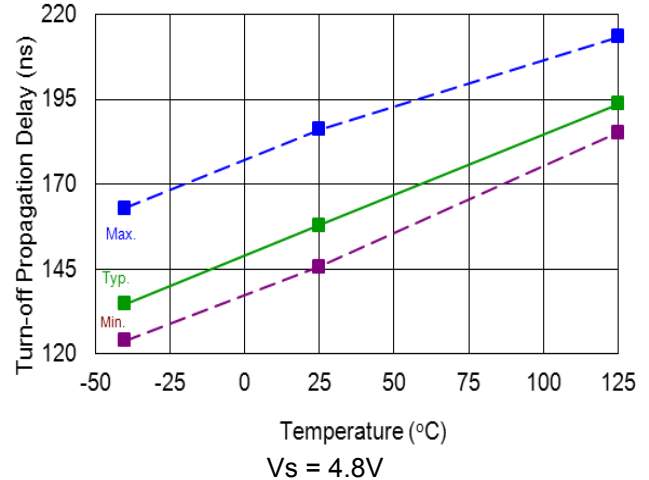


Figure 5. Turn-Off Propagation Delay vs. Temperature

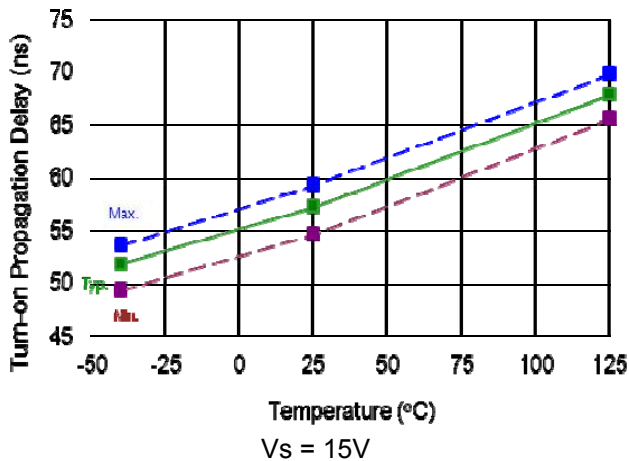


Figure 6. Turn-On Propagation Delay vs. Temperature

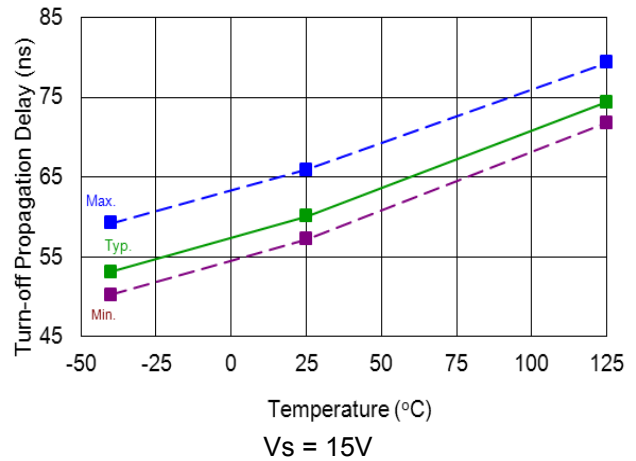


Figure 7. Turn-Off Propagation Delay vs. Temperature

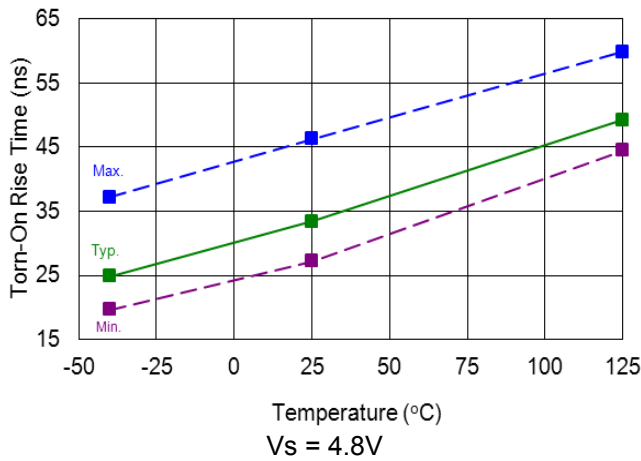


Figure 8. Turn-On Rise Time vs. Temperature

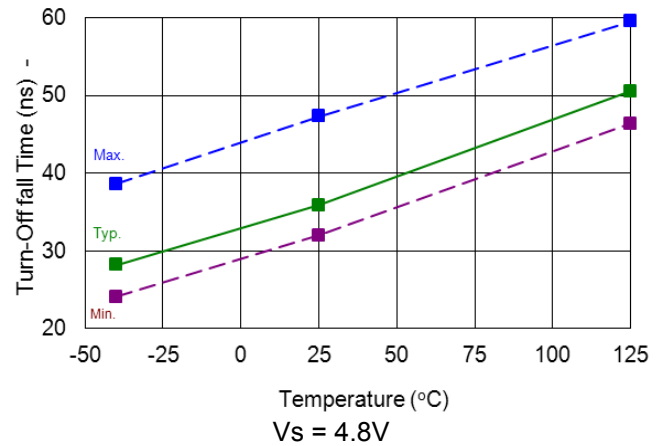


Figure 9. Turn-Off Fall Time vs. Temperature

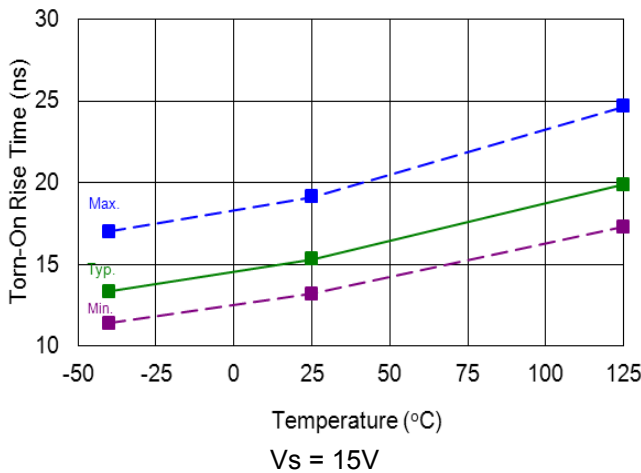


Figure 10. Turn-On Rise Time vs. Temperature

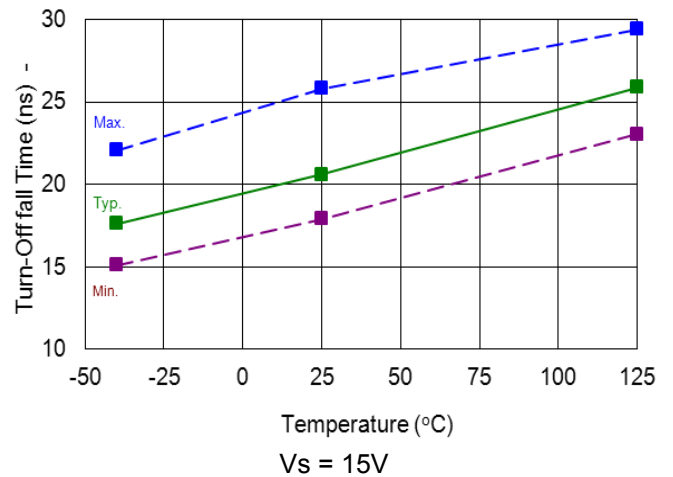


Figure 11. Turn-Off Fall Time vs. Temperature

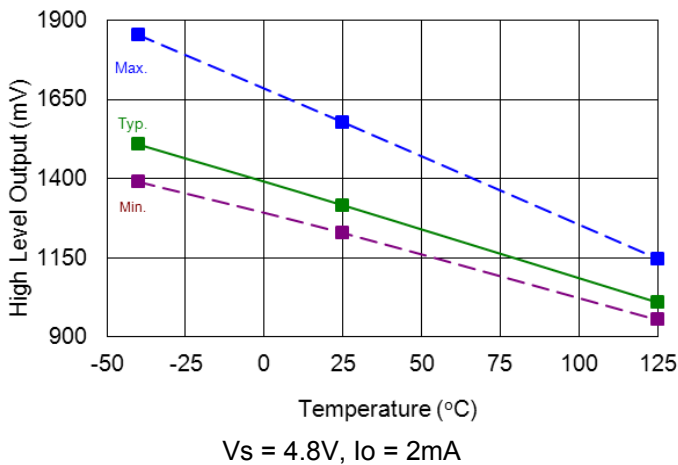


Figure 12. High Level Output Voltage vs. Temperature

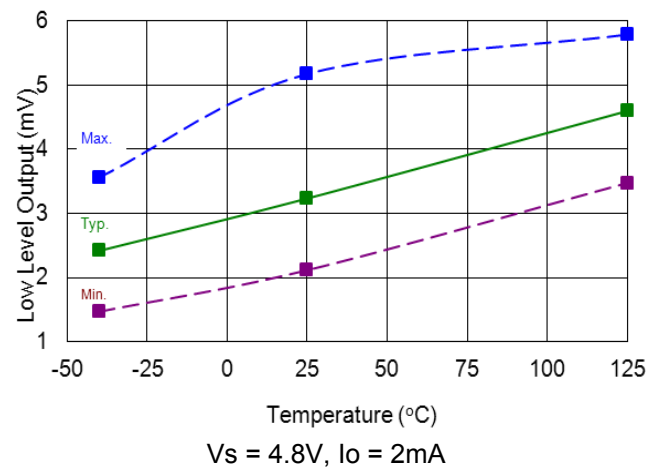
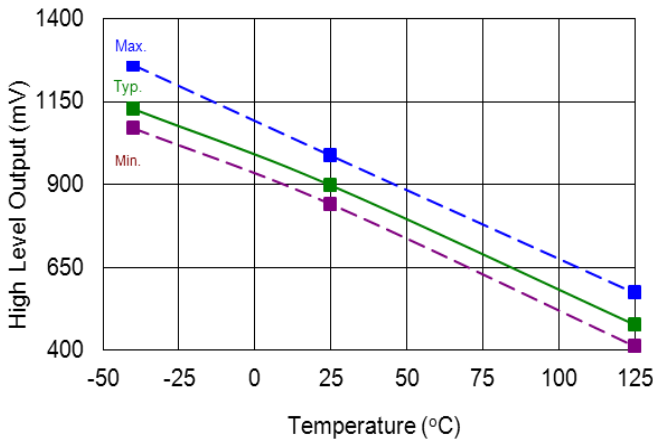
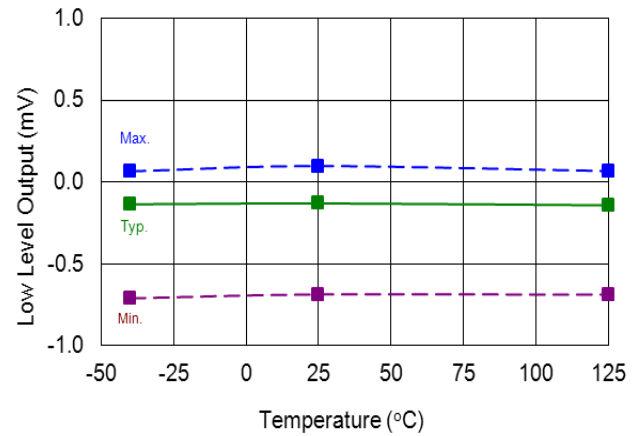


Figure 13. Low Level Output Voltage vs. Temperature



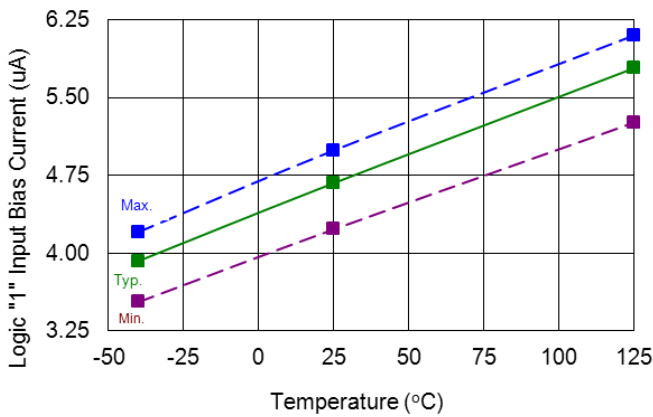
$V_s = 15V, I_o = 0mA$

Figure 14. High Level Output Voltage vs. Temperature



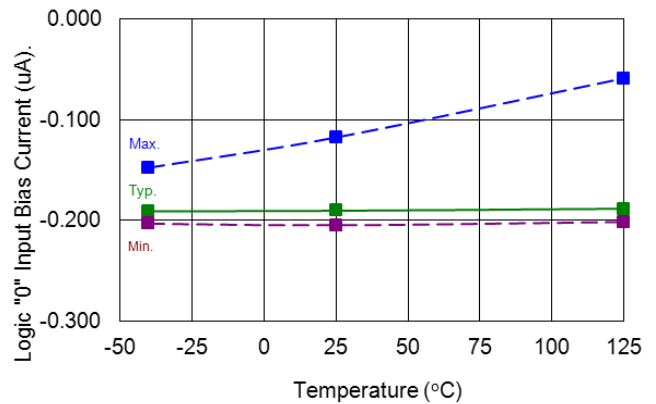
$V_s = 15V, I_o = 0mA$

Figure 15. Low Level Output Voltage vs. Temperature



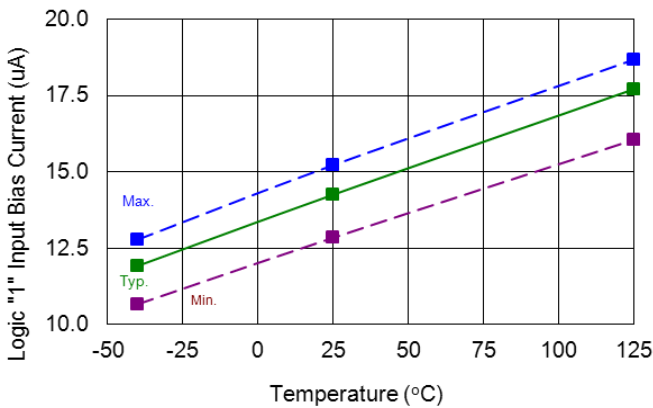
$V_s = 4.8V$

Figure 16. Logic "1" Input Bias Current vs. Temperature



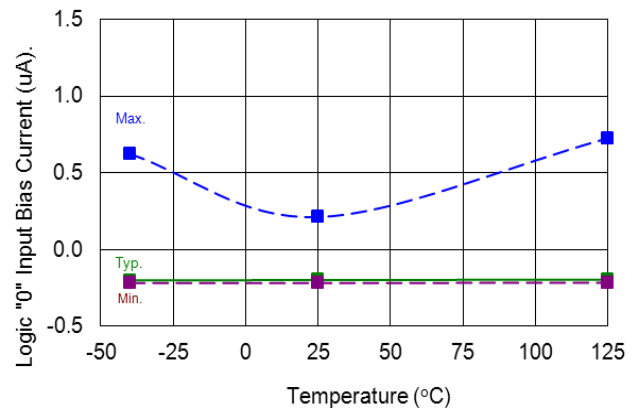
$V_s = 4.8V$

Figure 17. Logic "0" Input Bias Current vs. Temperature



$V_s = 15V$

Figure 18. Logic "1" Input Bias Current vs. Temperature



$V_s = 15V$

Figure 19. Logic "0" Input Bias Current vs. Temperature

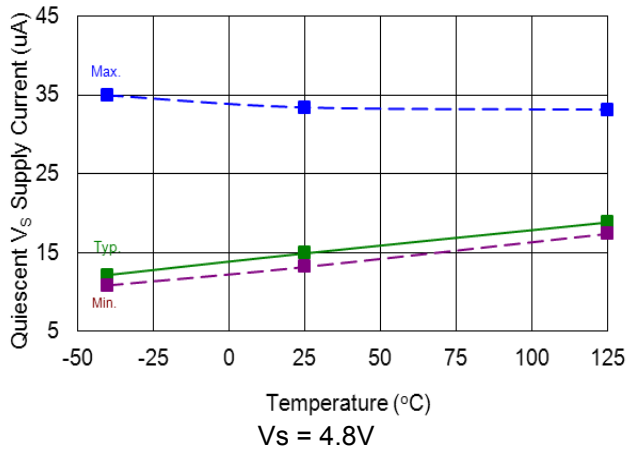


Figure 20. Quiescent V_S Supply Current vs. Temperature

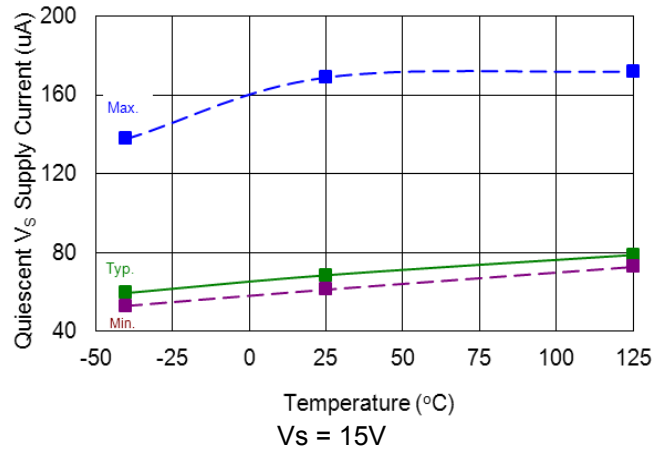
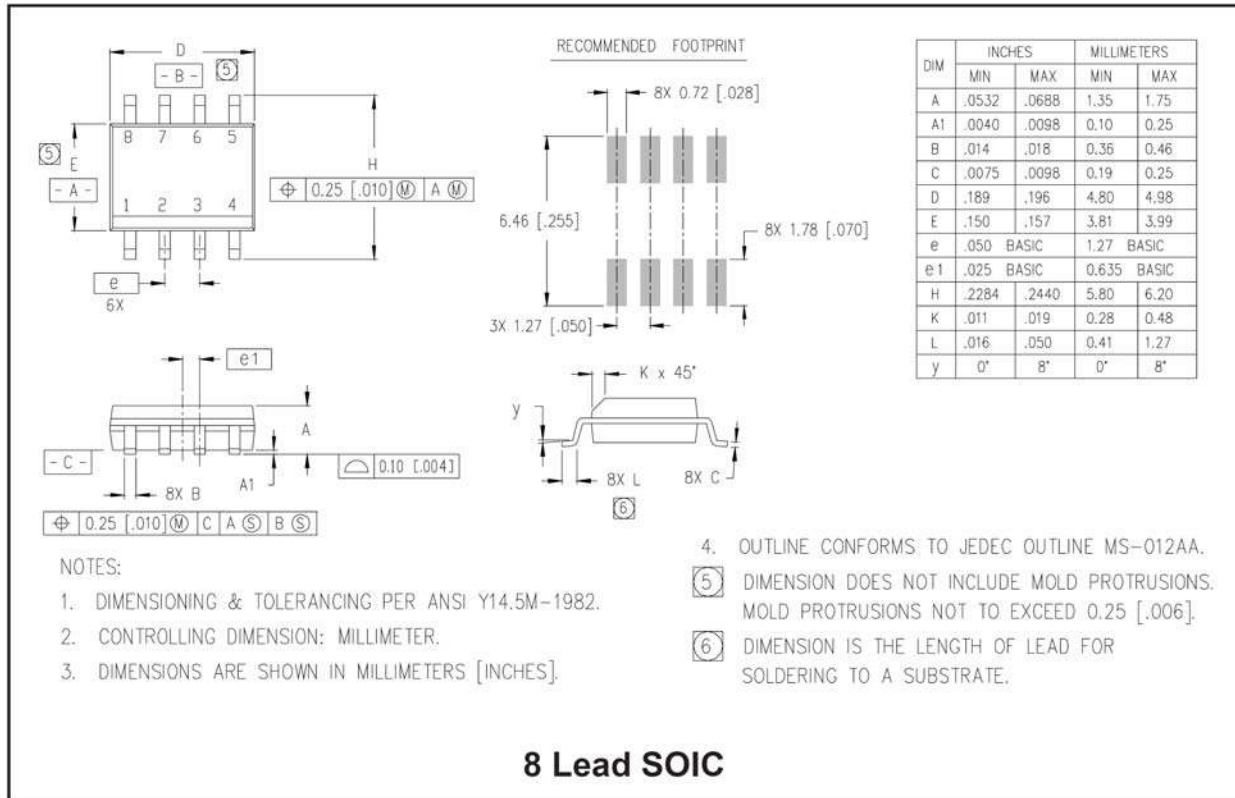
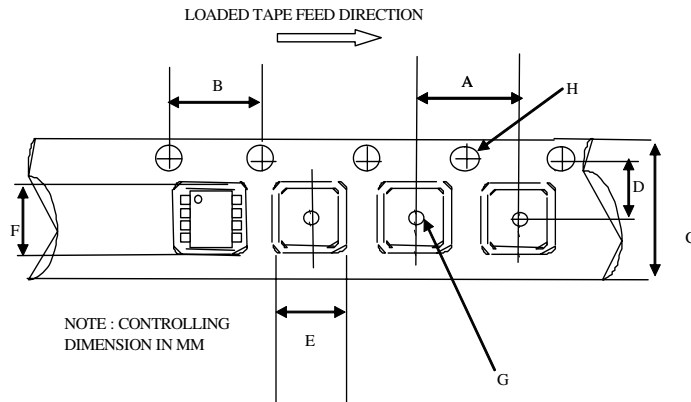


Figure 21. Quiescent V_S Supply Current vs. Temperature

Package Details: SOIC8

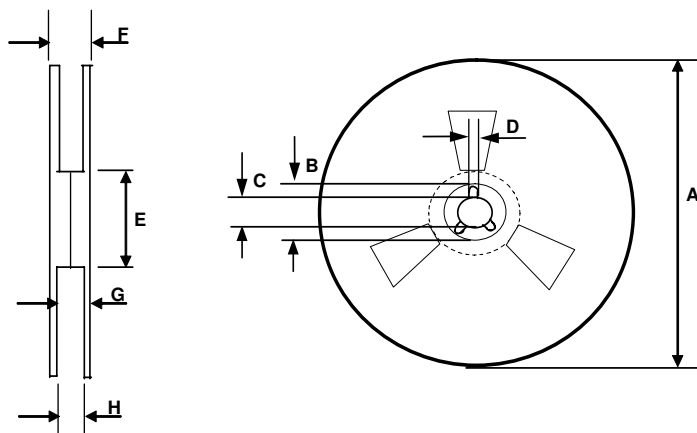


Tape and Reel Details: SOIC8



CARRIER TAPE DIMENSION FOR 8SOICN

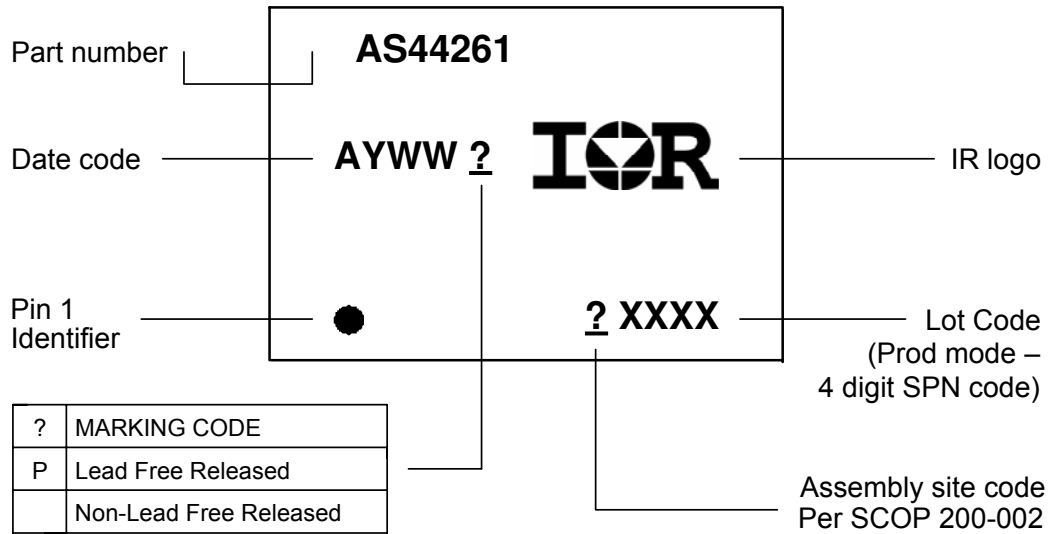
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

Part Marking Information



Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRS44261	SOIC8	Tube/Bulk	95	AUIRS44261S
		Tape and Reel	2500	AUIRS44261STR

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Revision History

Date	Comment
04/29/08	Draft
03/13/09	Front page Typ Application and diagram.
07/07/09	Removed PDIP8 and AUIRS4427, AUIRS4428
09/30/09	Reformatted entire data sheet, added part marking
01/06/09	Updated Td1 typ.=70ns & max=150ns; tf typ.=25ns & max= 50ns; VOH max.=1.4V; added note on IO+/- as guaranteed by design, added Input/Output Pin Equivalent Circuit Diagrams, added Important Notice, added ESD level in Qual Info Page, modified disclaimer under Absolute Max. Ratings; modified conditions under Dynamic Elec. Char.;
01/12/2010	Added parameter vs. temperature graphs; removed Preliminary; removed Latch Up rating in qualification info page
01/13/2010	Added passing voltage level for ESD on Qual Info Page.
01/31/2010	Removed passing voltage level for ESD on Qual Info Page.
03/12/2010	Front page: added unit (A) to IO+ & (ns) for ton; add "direct fuel injection" to application list. Page3: changed from Vcc to Vs in diagram, removed "cross-conduction" from description statement. Updated Parameter Trends vs temp statement with "supply voltage of 15V".
03/15/2010	Page 8: changed from Vcc to Vs in schematics; put back "driver cross-conduction" in description statement.
03/19/2010	Corrected Tf spec. typ=15nS, max=50nS.
07/30/2010	Part number changed to 44261; Min Vs=4.8V; Input thresholds spec changed into values proportional to Vs; Iqbmax consumption increased from 200uA to 220uA ; I _{IN+} increased to 15Vtyp and 25Vmax; I _{IN-} changed to 0uA _{typ} , 1uA _{max} ; input pullup resistor connected to Vs.
10/21/2010	Test condition corrected for Io- (Vo=4.8V instead of 15V) and for V _{OH} and V _{OL} (I=2mA instead of 20mA).
11/18/2010	AUIR4426 name corrected in AUIR44261 page2 and header
01/17/2011	Table with Vs=4.8V: VOH max limit changed to 1.9V; Tr to 65ns and td2 to 220ns
02/22/2011	Removed tri-temp graphs
03/02/2011	Inserted tri-temp graphs, based on 3 sigma and Vs = 4.8V & 15V
03/04/2011	Added "Preliminary Data Sheet" in front page titles.
5/17/2011	Updated tri-temp graphs, important notice. Change Iqs_15V typ. To 70; Voh(4.8) max to 2.2; Tr, Tf (4.8) max to 75; Ton(4.8) max to 220; Toff(4.8) max to 250.
5/30/2011	VIH and VIL parameter exchange; VOH specified at cold and at hot.
6/30/11	Updated part marking & world headquarters address