BLC9G15LS-400AVT

Power LDMOS transistor

Rev. 3 — 24 November 2017

AMPLEON

Product data sheet

1. Product profile

1.1 General description

400 W LDMOS packaged asymmetric Doherty power transistor for base station applications at frequencies from 1452 MHz to 1511 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in an asymmetrical Doherty production test circuit. V_{DS} = 32 V; I_{Dq} = 810 mA (main); $V_{GS(amp)peak}$ = 0.5 V, unless otherwise specified.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
1-carrier W-CDMA	1452 to 1511	32	93	16.5	48	–35 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.6 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

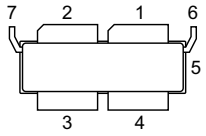
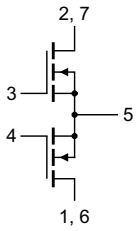
- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion capability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 1452 MHz to 1511 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain2 (peak)		
2	drain1 (main)		
3	gate1 (main)		
4	gate2 (peak)		
5	source [1]		
6	video decoupling (peak)		
7	video decoupling (main)		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLC9G15LS-400AVT	-	air cavity plastic earless flanged package; 6 leads	SOT1258-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		–6	+13	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		–6	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C
T_{case}	case temperature	operating [1]	–40	+125	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	V_{DS} = 32 V; I_{Dq} = 980 mA (main); $V_{GS(amp)peak}$ = 0,4 V; T_{case} = 80 °C		
		P_L = 93 W	0.31	k/W
		P_L = 117 W	0.29	k/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 1.62 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 162 mA	1.5	2.0	2.5	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 32 V; I_D = 810 mA	1.65	2.15	2.65	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	2.8	µA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V	-	32	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 8.1 A	-	11.5	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 5.67 A	-	85	149	mΩ
Peak device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 3.0 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 300 mA	1.5	2.0	2.5	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 32 V; I_D = 1500 mA	1.65	2.15	2.65	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	2.8	µA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V	-	52	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 15 A	-	20.5	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 10.5 A	-	46	85	mΩ

Table 7. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH; f_1 = 1455 MHz; f_2 = 1508.5 MHz; RF performance at V_{DS} = 32 V; I_{Dq} = 810 mA (main); $V_{GS(amp)peak}$ = 0.5 V; T_{case} = 25 °C; unless otherwise specified; in an asymmetrical Doherty production test circuit at frequencies from 1452 MHz to 1511 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 93 W	15	16.2	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 93 W	-	−15	−10	dB
η_D	drain efficiency	$P_{L(AV)}$ = 93 W	46.5	51	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 93 W	-	−34	−29	dBc

Table 8. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH; f = 1508.5 MHz; RF performance at V_{DS} = 32 V; I_{Dq} = 810 mA (main); $V_{GS(amp)peak}$ = 0.5 V; T_{case} = 25 °C; unless otherwise specified; in an asymmetrical Doherty production test circuit at a frequency of 1511 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PAR_O	output peak-to-average ratio	$P_{L(AV)}$ = 110 W	6.3	6.9	-	dB
$P_{L(M)}$	peak output power	$P_{L(AV)}$ = 110 W	460	540	-	W

7. Test information

7.1 Ruggedness in Doherty operation

The BLC9G15LS-400AVT is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 32 V; I_{Dq} = 810 mA; $V_{GS(amp)peak}$ = 0.5 V; f = 1454.5 MHz; P_L = 126 W (5 dB OBO); 1-carrier W-CDMA; 100 % clipping.

7.2 Impedance information

Table 9. Typical impedance of main device

Measured load-pull data of main device; I_{Dq} = 810 mA (main); V_{DS} = 30 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
1440	1.0 – j4.8	0.9 – j3.4	245	53.5	18.0
1480	1.4 – j5.3	0.9 – j3.7	245	55.6	18.3
1510	1.5 – j5.7	1.0 – j4.0	245	57.1	18.7
Maximum drain efficiency load					
1440	1.0 – j4.8	2.5 – j3.1	170	71.8	21.4
1480	1.4 – j5.3	2.5 – j2.9	153	72.3	21.8
1510	1.5 – j5.7	2.5 – j3.0	153	71.2	21.9

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

Table 10. Typical impedance of peak device

Measured load-pull data of peak device; I_{Dq} = 1800 mA (peak); V_{DS} = 30 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
1440	2.0 – j7.6	1.5 – j3.4	390	54.3	19.4
1480	3.0 – j8.0	1.6 – j3.4	400	57.0	19.7
1510	2.8 – j9.2	1.8 – j3.6	390	55.4	19.8
Maximum drain efficiency load					
1440	2.0 – j7.6	3.1 – j1.4	255	67.3	22.4
1480	3.0 – j8.0	2.5 – j1.7	271	68.3	22.3
1510	2.8 – j9.2	2.2 – j1.9	283	67.2	22.4

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

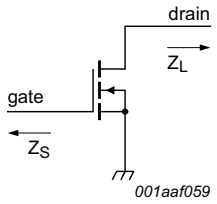


Fig 1. Definition of transistor impedance

7.3 Recommended impedances for Doherty design

Table 11. Typical impedance of main at 1 : 1 load

Measured load-pull data of main device; I_{Dq} = 810 mA (main); V_{DS} = 30 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	$P_{L(3dB)}$ [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
1440	1.0 – j4.8	1.50 – j4.2	220	45	19.5
1480	1.4 – j5.3	1.40 – j3.7	230	46	19.6
1510	1.5 – j5.7	1.38 – j3.5	220	47	20.4

[1] Z_S and Z_L defined in Figure 1.

[2] At $P_{L(AV)}$ = 93 W.

Table 12. Typical impedance of main device at 1 : 2.5 load

Measured load-pull data of main device; I_{Dq} = 810 mA (main); V_{DS} = 30 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	$P_{L(3dB)}$ [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
1440	1.0 – j4.8	3.4 – j3.5	140	65	22.0
1480	1.4 – j5.3	3.3 – j3.2	125	65	22.4
1510	1.5 – j5.7	3.3 – j3.0	120	64	23.2

[1] Z_S and Z_L defined in Figure 1.

[2] At $P_{L(AV)}$ = 93 W.

Table 13. Typical impedance of peak device at 1 : 1 load

Measured load-pull data of peak device; I_{Dq} = 1500 mA (peak); V_{DS} = 30 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	$P_{L(3dB)}$ [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
1410	2.0 – j7.6	2.0 – j4.2	380	31	19.0
1480	3.0 – j8.0	1.9 – j3.6	390	32.5	19.6
1520	2.8 – j9.2	1.9 – j3.3	380	33	20.3

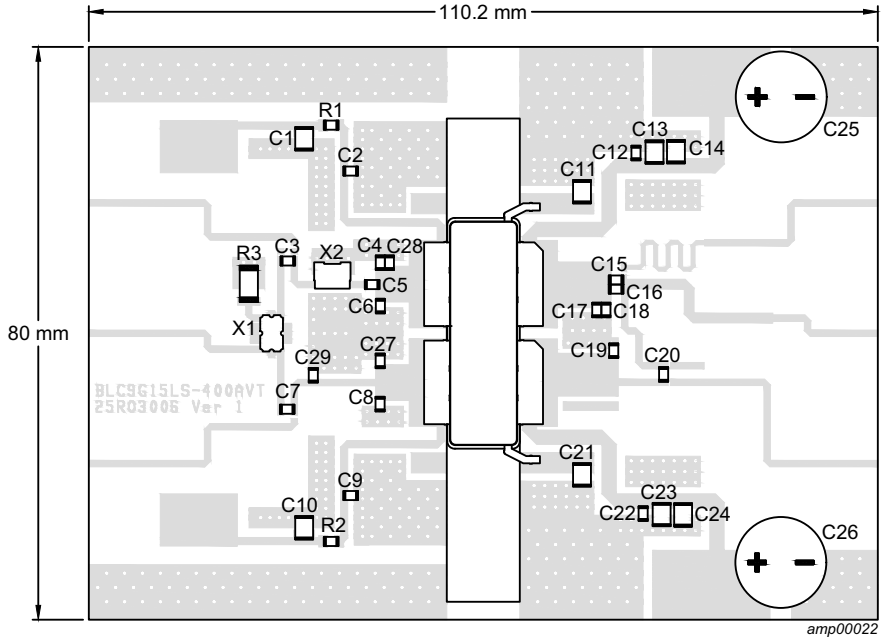
[1] Z_S and Z_L defined in Figure 1.

[2] At $P_{L(AV)}$ = 93 W.

Table 14. Off-state impedances of peak device

f	Z_{off}
(MHz)	(Ω)
1410	1.22 – j3.50
1480	0.57 – j1.30
1520	0.43 – j0.63

7.4 Test circuit



Printed-Circuit Board (PCB): Rogers 3006: ε_r = 6.15; thickness = 0.635 mm; thickness copper plating = 35 μm. See Table 15 for a list of components.

Fig 2. Component layout

Table 15. List of components

See Figure 2 for component layout.

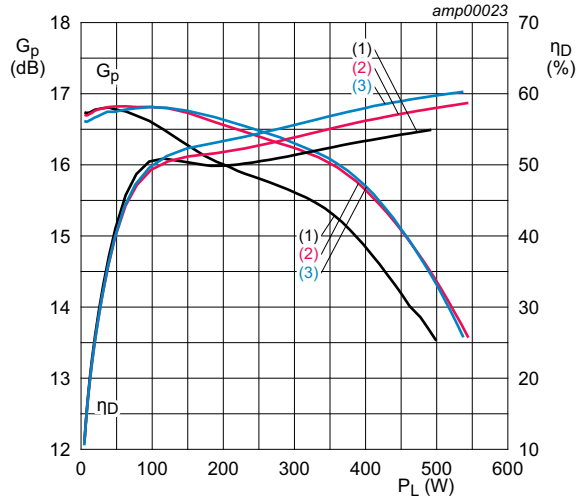
Component	Description	Value	Remarks
C1, C10, C11, C13, C14, C21, C23, C24	multilayer ceramic chip capacitor	4.7 μF	Murata GRM32ER71H475KA88L
C2, C3, C5, C7, C9, C12, C15, C16, C20, C22	multilayer ceramic chip capacitor	18 pF	Murata Hi-Q 0805
C4,C6, C27, C28	multilayer ceramic chip capacitor	2.0 pF	Murata Hi-Q 0805
C8,C17, C18	multilayer ceramic chip capacitor	1.8 pF	Murata Hi-Q 0805
C19	multilayer ceramic chip capacitor	2.7 pF	Murata Hi-Q 0805
C25, C26	electrolytic capacitor	470 μF	63 V
C29	multilayer ceramic chip capacitor	0.3 pF	ATC 100A 0805
R1, R2	SMD resistor	4.7 Ω, 1 %	0805

Table 15. List of components *…continued*
See Figure 2 for component layout.

Component	Description	Value	Remarks
R3	SMD resistor	50 Ω, 25 W	Anaren C16A50Z4
X1	hybrid coupler	2 dB, 90°	Anaren X3C20F1-02S
X2	attenuator	1 dB	Anaren D10AAXXZ4

7.5 Graphical data

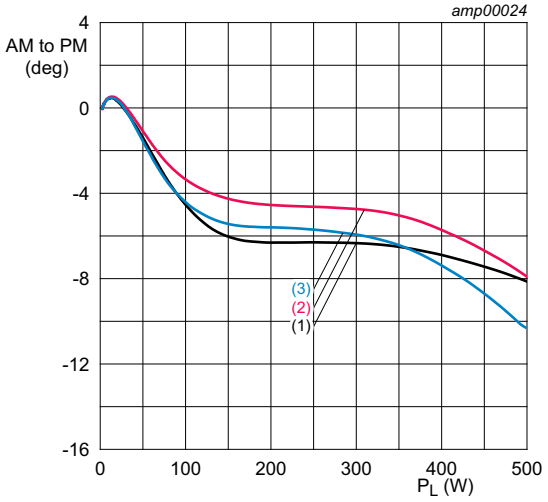
7.5.1 Pulsed CW



V_{DS} = 32 V; I_{Dq} = 810 mA; $V_{GS(amp)peak}$ = 0.5 V; t_p = 100 μs; δ = 10 %.

(1) f = 1452 MHz
(2) f = 1492 MHz
(3) f = 1511 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values



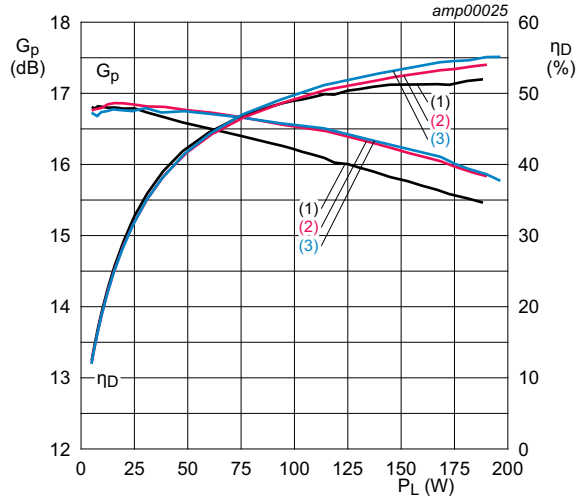
V_{DS} = 32 V; I_{Dq} = 810 mA; $V_{GS(amp)peak}$ = 0.5 V.

(1) f = 1452 MHz
(2) f = 1492 MHz
(3) f = 1511 MHz

Fig 4. AM to PM as a function of output power; typical values

7.5.2 1-Carrier W-CDMA

PAR = 9.6 dB per carrier at 0.01 % probability on the CCDF; 3GPP test model 1 with 64 DPCH (100 % clipping).



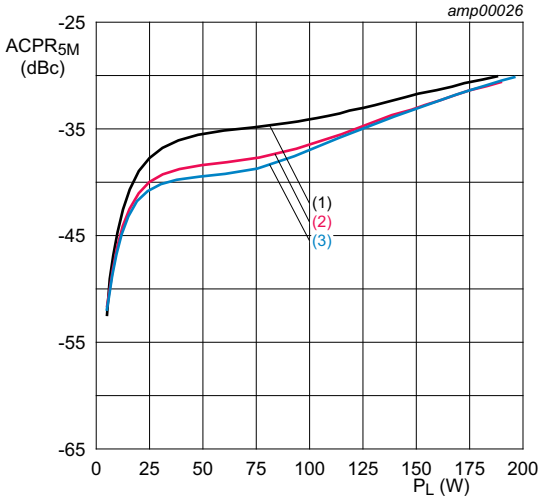
V_{DS} = 32 V; I_{Dq} = 810 mA; $V_{GS(amp)peak}$ = 0.5 V.

(1) f = 1454.5 MHz

(2) f = 1489.5 MHz

(3) f = 1508.5 MHz

Fig 5. Power gain and drain efficiency as function of output power; typical values



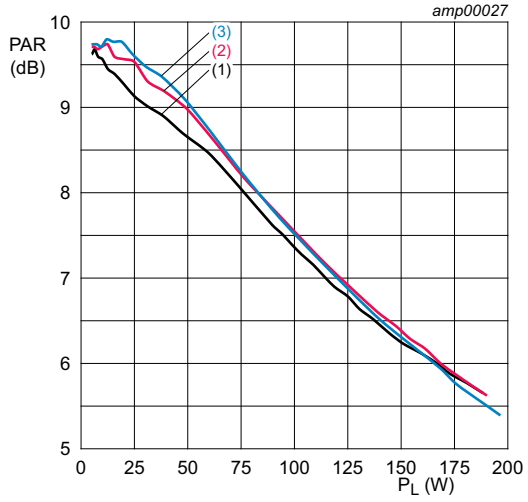
V_{DS} = 32 V; I_{Dq} = 810 mA; $V_{GS(amp)peak}$ = 0.5 V.

(1) f = 1454.5 MHz

(2) f = 1489.5 MHz

(3) f = 1508.5 MHz

Fig 6. Adjacent channel power ratio (5 MHz) and adjacent channel power ratio (10 MHz) as function of output power; typical values



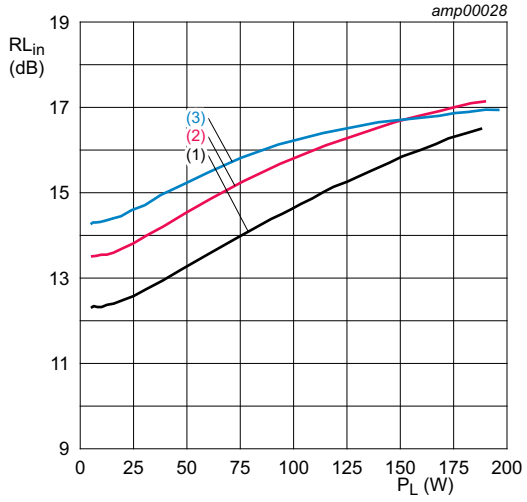
V_{DS} = 32 V; I_{Dq} = 810 mA; $V_{GS(amp)peak}$ = 0.5 V.

(1) f = 1454.5 MHz

(2) f = 1489.5 MHz

(3) f = 1508.5 MHz

Fig 7. Peak-to-average power ratio as a function of output power; typical values



V_{DS} = 32 V; I_{Dq} = 810 mA; $V_{GS(amp)peak}$ = 0.5 V.

(1) f = 1454.5 MHz

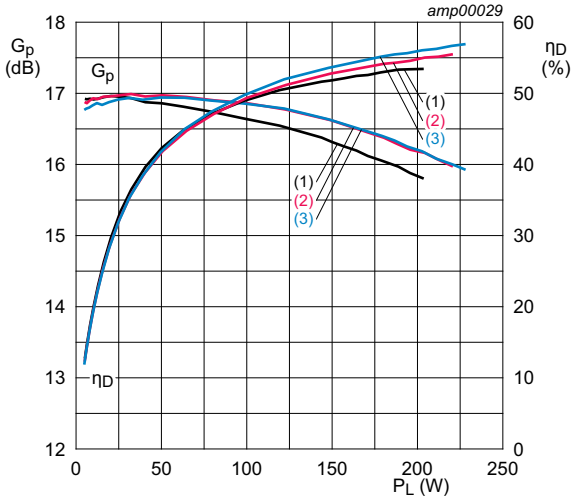
(2) f = 1489.5 MHz

(3) f = 1508.5 MHz

Fig 8. Input return loss as a function of output power; typical values

7.5.3 2-Carrier W-CDMA

PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1 with 64 DPCH (46 % clipping).



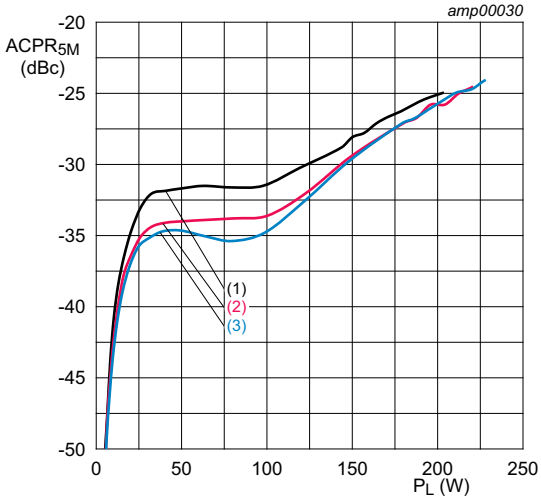
V_{DS} = 32 V; I_{Dq} = 810 mA; $V_{GS(amp)peak}$ = 0.5 V.

(1) f = 1457 MHz

(2) f = 1487 MHz

(3) f = 1506 MHz

Fig 9. Power gain and drain efficiency as function of output power; typical values



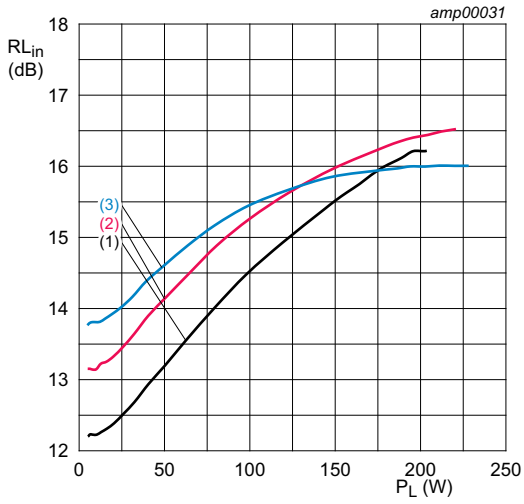
V_{DS} = 32 V; I_{Dq} = 810 mA; $V_{GS(amp)peak}$ = 0.5 V.

(1) f = 1457 MHz

(2) f = 1487 MHz

(3) f = 1506 MHz

Fig 10. Adjacent channel power ratio (5 MHz) and adjacent channel power ratio (10 MHz) as function of output power; typical values



V_{DS} = 32 V; I_{Dq} = 810 mA; $V_{GS(amp)peak}$ = 0.5 V.

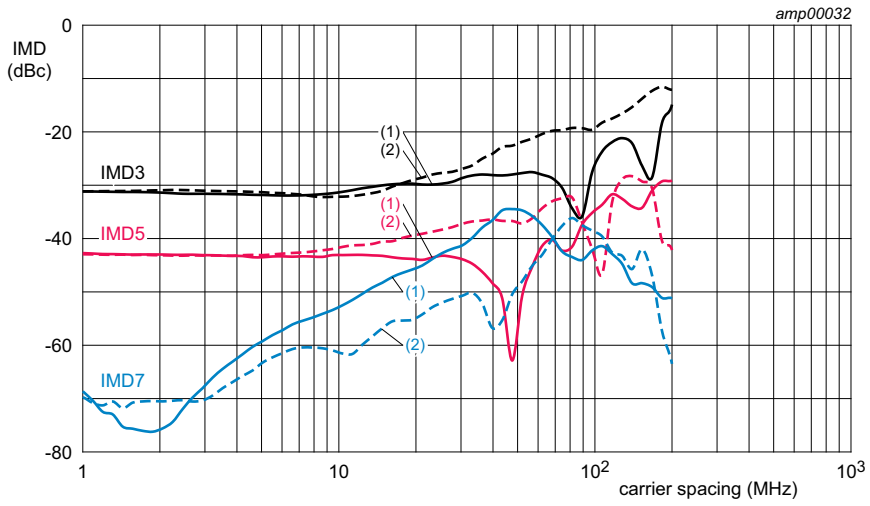
(1) f = 1457 MHz

(2) f = 1487 MHz

(3) f = 1506 MHz

Fig 11. Input return loss as a function of output power; typical values

7.5.4 2-Tone VBW



V_{DS} = 32 V; I_{Dq} = 810 mA; $V_{GS(amp)peak}$ = 0.5 V.

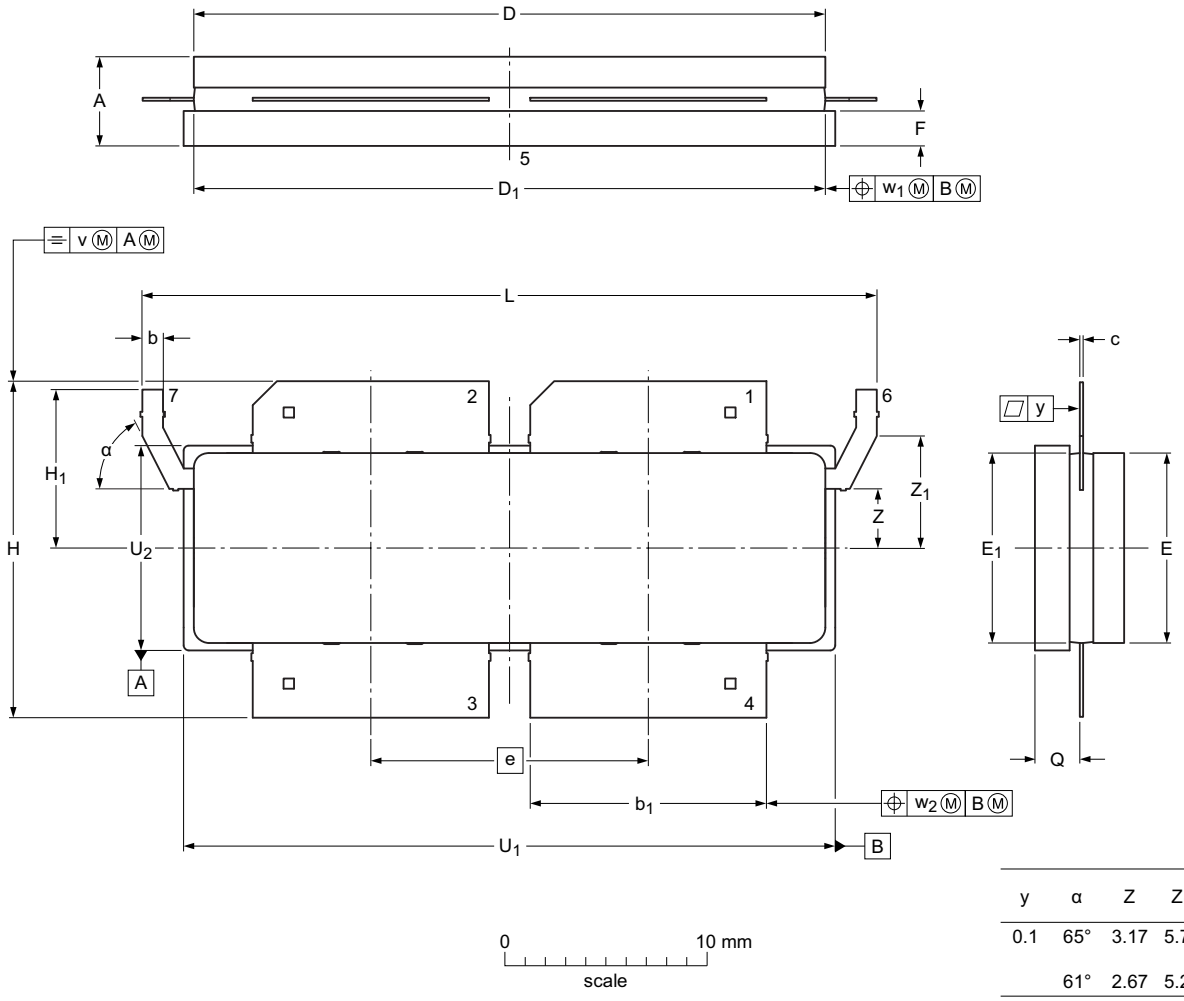
(1) IMD low

(2) IMD high

Fig 12. VBW capability

8. Package outline

Air cavity plastic earless flanged package; 6 leads **SOT1258-1**



y	α	Z	Z_1
0.1	65°	3.17	5.79
	61°	2.67	5.29

Dimensions

Unit		A	b	b_1	c	D	D_1	E	E_1	e	L	F	H	H_1	Q(1)	U_1	U_2	v	w_1	w_2
mm	max	4.65	1.12	11.78	0.2	31.44	31.34	9.60	9.50	13.72	36.42	1.83	16.71	8.12	2.33	32.33	10.23	0.5	0.5	0.5
	nom																			
	min	4.18	0.91	11.58	0.1	31.04	31.14	9.20	9.30		36.22	1.63	16.51	7.62	2.13	32.13	10.03			

Note
1. Dimension Q is measured 0.1 mm away from the flange.
2. Ringframe and/or ringframe glue shall not overhang at the side of the flange.

sot1258-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1258-1						~~14-02-24~~ 17-08-31

Fig 13. Package outline SOT1258-1

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 16. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V, but fails after exposure to an ESD pulse of 750 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V, but fails after exposure to an ESD pulse of 4000 V.

10. Abbreviations

Table 17. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
AM	Amplitude Modulation
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
OBO	Output Back Off
PAR	Peak-to-Average Ratio
PM	Phase Modulation
SMD	Surface Mounted Device
VBW	Video Bandwidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC9G15LS-400AVT v.3	20171124	Product data sheet	-	BLC9G15LS-400AVT v.2
Modifications:	• Table 2 on page 2: changed simplified version drawing SOT1258-3 to SOT1258-1 • Table 3 on page 2: changed version SOT1258-3 to SOT1258-1 • Figure 13 on page 11: changed package outline drawing SOT1258-3 to SOT1258-1			
BLC9G15LS-400AVT v.2	20161202	Product data sheet	-	BLC9G15LS-400AVT v.1
BLC9G15LS-400AVT v.1	20160317	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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13. Contact information

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14. Contents

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